

18-BIT, 500-kHz, UNIPOLAR INPUT, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE

FEATURES

- 500-kHz Sample Rate
- 18-Bit NMC Ensured Over Temperature
- Zero Latency
- Low Power: 110 mW at 500 kHz
- Unipolar Input Range
- Onboard Reference Buffer
- High-Speed Parallel Interface
- Wide Digital Supply
- 8-/16-/18-Bit Bus Transfer
- 48-Pin TQFP Package

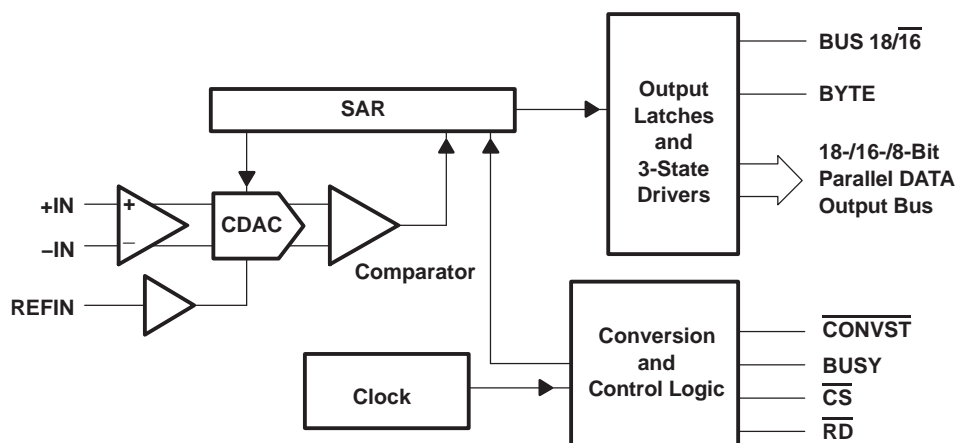
APPLICATIONS

- Medical Instruments
- Optical Networking
- Transducer Interface
- High Accuracy Data Acquisition Systems
- Magnetometers

DESCRIPTION

The ADS8383 is an 18-bit, 500 kHz A/D converter. The device includes a 18-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8383 offers a full 18-bit interface, a 16-bit option where data is read using two read cycles or an 8-bit bus option using three read cycles.

The ADS8383 is available in a 48-lead TQFP package and is characterized over the industrial -40°C to 85°C temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

| MODEL | MAXIMUM INTEGRAL LINEARITY (LSB) | MAXIMUM DIFFERENTIAL LINEARITY (LSB) | NO MISSING CODES RESOLUTION (BIT) | PACKAGE TYPE | PACKAGE DESIGNATOR | TEMPERATURE RANGE | ORDERING INFORMATION | TRANSPORT MEDIA QUANTITY |
|-----------|----------------------------------|--------------------------------------|-----------------------------------|--------------|--------------------|-------------------|----------------------|--------------------------|
| ADS8383I | ±10 | -2~7 | 17 | 48 Pin TQFP | PFB | -40°C to 85°C | ADS8383IPFBT | Tape and reel 250 |
| | | | | | | | ADS8383IPFBR | Tape and reel 1000 |
| ADS8383IB | ±7 | -1~2.5 | 18 | 48 Pin TQFP | PFB | -40°C to 85°C | ADS8383IBPFBT | Tape and reel 250 |
| | | | | | | | ADS8383IBPFBR | Tape and reel 1000 |

NOTE: For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | | UNIT |
|------------------------------------------------------|-----------------------------------|--------------------------------------------------------|
| Voltage | +IN to AGND | -0.4 V to +VA + 0.1 V |
| | -IN to AGND | -0.4 V to 0.5 V |
| Voltage | +VA to AGND | -0.3 V to 7 V |
| | +VBD to BDGND | -0.3 V to 7 V |
| | +VA to +VBD | -0.3 V to 2.5 V |
| Digital input voltage to BDGND | | -0.3 V to +VBD + 0.3 V |
| Digital output voltage to BDGND | | -0.3 V to +VBD + 0.3 V |
| Operating free-air temperature range, T _A | | -40°C to 85°C |
| Storage temperature range, T _{stg} | | -65°C to 150°C |
| Junction temperature (T _J max) | | 150°C |
| TQFP package | Power dissipation | (T _J Max - T _A)/θ _{JA} |
| | θ _{JA} thermal impedance | 86°C/W |
| Lead temperature, soldering | Vapor phase (60 sec) | 215°C |
| | Infrared (15 sec) | 220°C |

⁽¹⁾ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS
 $T_A = -40^\circ\text{C}$ to 85°C , $+V_A = 5\text{ V}$, $+V_{BD} = 3\text{ V}$ or 5 V , $V_{\text{ref}} = 4.096\text{ V}$, $f_{\text{SAMPLE}} = 500\text{ kHz}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|----------------------------------------|--|-----------------------|-----------------------------------|--------|------------------------|-----------------|-----|
| Analog Input | | | | | | | |
| Full-scale input voltage (see Note 1) | | +IN – –IN | 0 | | V_{ref} | V | |
| Absolute input voltage | | +IN | –0.2 | | $V_{\text{ref}} + 0.2$ | V | |
| | | –IN | –0.2 | | 0.2 | | |
| Input capacitance | | | | 45 | | pF | |
| Input leakage current | | | | 1 | | nA | |
| System Performance | | | | | | | |
| Resolution | | | | 18 | | Bits | |
| No missing codes | | ADS8383I | (+IN – –IN) < 0.5 FS | | 17 | Bits | |
| | | | (+IN – –IN) ≥ 0.5 FS | | 17 | | |
| | | ADS8383IB | | | 18 | | |
| Integral linearity (see Notes 2 and 3) | | ADS8383I | (+IN – –IN) < 0.125 FS | | –4 | LSB (18 bit) | |
| | | | (+IN – –IN) < 0.5 FS | | –6 | | |
| | | | (+IN – –IN) ≥ 0.5 FS | | –10 | | |
| | | ADS8383IB | –7 | –2/3 | 7 | | |
| Differential linearity | | ADS8383I | (+IN – –IN) < 0.125 FS | | –1 | LSB (18 bit) | |
| | | | (+IN – –IN) < 0.5 FS | | –1 | | |
| | | | (+IN – –IN) ≥ 0.5 FS | | –2 | | |
| | | ADS8383IB | –1 | –1/1.4 | 2.5 | | |
| Offset error (see Note 4) | | ADS8383I | –1 | ±0.5 | 1 | mV | |
| | | ADS8383IB | –0.75 | ±0.25 | 0.75 | | |
| Gain error (see Note 4) | | ADS8383I | $V_{\text{ref}} = 4.096\text{ V}$ | | –0.1 | 0.1 | %FS |
| | | ADS8383IB | $V_{\text{ref}} = 4.096\text{ V}$ | | –0.06 | 0.06 | %FS |
| Noise | | | | 60 | | μV RMS | |
| Power supply rejection ratio | | At 3FFFFh output code | | 75 | | dB | |
| Sampling Dynamics | | | | | | | |
| Conversion time | | | | | 1.52 | μs | |
| Acquisition time | | | 0.4 | | | μs | |
| Throughput rate | | | | | 500 | kHz | |
| Aperture delay | | | | 4 | | ns | |
| Aperture jitter | | | | 15 | | ps | |
| Step response | | | | 150 | | ns | |
| Over voltage recovery | | | | 150 | | ns | |

(1) Ideal input span, does not include gain or offset error.

(2) LSB means least significant bit

(3) This is endpoint INL, not best fit.

(4) Measured relative to an ideal full-scale input (+IN – –IN) of 4.096 V

SPECIFICATIONS (CONTINUED)

T_A = -40°C to 85°C, +V_A = +5 V, +V_{BD} = 3 V or 5 V, V_{ref} = 4.096 V, f_{SAMPLE} = 500 kHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------------------------|-----------|------------------------------------------------|------|-------|-----|------|
| Dynamic Characteristics | | | | | | |
| Total harmonic distortion (THD) (see Note 1) | ADS8383I | V _{IN} = 4 V _{pp} at 1 kHz | | -110 | | dB |
| | ADS8383IB | | | -112 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 10 kHz | | -98 | | |
| | ADS8383IB | | | -108 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 50 kHz | | -98 | | |
| | ADS8383IB | | | -99 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 100 kHz | | -90 | | |
| | ADS8383IB | | | -91 | | |
| Signal to noise ratio (SNR) (see Note 1) | ADS8383I | V _{IN} = 4 V _{pp} at 1 kHz | | 87 | | dB |
| | ADS8383IB | | | 88 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 10 kHz | | 87 | | |
| | ADS8383IB | | | 87 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 50 kHz | | 87 | | |
| | ADS8383IB | | | 87 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 100 kHz | | 87 | | |
| | ADS8383IB | | | 87 | | |
| Signal to noise + distortion (SINAD) (see Note 1) | ADS8383I | V _{IN} = 4 V _{pp} at 1 kHz | | 86 | | dB |
| | ADS8383IB | | | 87 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 10 kHz | | 86 | | |
| | ADS8383IB | | | 86 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 50 kHz | | 86 | | |
| | ADS8383IB | | | 86 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 100 kHz | | 85 | | |
| | ADS8383IB | | | 85 | | |
| Spurious free dynamic range (SFDR) (see Note 1) | ADS8383I | V _{IN} = 4 V _{pp} at 1 kHz | | 110 | | dB |
| | ADS8383IB | | | 112 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 10 kHz | | 98 | | |
| | ADS8383IB | | | 108 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 50 kHz | | 98 | | |
| | ADS8383IB | | | 98 | | |
| | ADS8383I | V _{IN} = 4 V _{pp} at 100 kHz | | 90 | | |
| | ADS8383IB | | | 94 | | |
| -3dB Small signal bandwidth | | | | 3 | | MHz |
| Voltage Reference Input | | | | | | |
| Reference voltage at REFIN, V _{ref} | | | 2.5 | 4.096 | 4.2 | V |
| Reference resistance (see Note 2) | | | | 500 | | kΩ |
| Reference current drain | | f _S = 500 kHz | | | 1 | mA |
| Bias Input | | | | | | |
| Bias input range | | | 2 | 2.048 | 2.1 | V |
| Bias input drift | | | | | ±5 | %FS |
| Bias input current, sink | | | -150 | -100 | | μA |

(1) Calculated on the first nine harmonics of the input frequency

(2) Can vary ±20%

SPECIFICATIONS (CONTINUED)
 $T_A = -40^\circ\text{C}$ to 85°C , $+VA = +5\text{ V}$, $+VBD = 3\text{ V}$ or 5 V , $V_{\text{ref}} = 4.096\text{ V}$, $f_{\text{SAMPLE}} = 500\text{ kHz}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------|----------------------------|-------------------------------|-----------------|--------------|------|------------------|
| Digital Input/Output | | | | | | |
| Logic family | | | CMOS | | | |
| Logic level | V_{IH} | $I_{IH} = 5\ \mu\text{A}$ | $+VBD - 1$ | $+VBD + 0.3$ | | V |
| | V_{IL} | $I_{IL} = 5\ \mu\text{A}$ | -0.3 | 0.8 | | |
| | V_{OH} | $I_{OH} = 2\text{ TTL loads}$ | $+VBD - 0.6$ | | | |
| | V_{OL} | $I_{OL} = 2\text{ TTL loads}$ | 0.4 | | | |
| Data format | | | Straight Binary | | | |
| Power Supply Requirements | | | | | | |
| Power supply voltage | $+VBD$ (see Notes 1 and 2) | | 2.95 | 3.3 | 5.25 | V |
| | $+VA$ (see Note 2) | | 4.75 | 5 | 5.25 | V |
| Supply current, 500-kHz sample rate (see Note 3) | | | | 22 | 26 | mA |
| Power dissipation, 500-kHz sample rate (see Note 3) | | | | 110 | 130 | mW |
| Temperature Range | | | | | | |
| Operating free-air | | | -40 | | 85 | $^\circ\text{C}$ |

 (1) The difference between $+VA$ and $+VBD$ should be no less than 2.3 V, i.e. if $+VA$ is 5.5 V, $+VBD$ should be at least 2.95 V.

 (2) $+VBD \geq +VA - 2.3\text{ V}$

 (3) This includes only $+VA$ current. $+VBD$ current is typical 1 mA with 5 pF load capacitance on all output pins.

TIMING CHARACTERISTICS

All specifications typical at -40°C to 85°C, +VA = +VBD = 5 V (see Notes 1, 2, and 3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----|------|------|
| t _{CONV} | Conversion time | | | 1.52 | μs |
| t _{ACQ} | Acquisition time | 0.4 | | | μs |
| t _{HOLD} | Hold time, sampling capacitor | | | 25 | ns |
| t _{pd1} | Propagation delay time, $\overline{\text{CONVST}}$ low to conversion started (BUSY high) | | | 45 | ns |
| t _{pd2} | Propagation delay time, end of conversion to BUSY low | | | 20 | ns |
| t _{pd3} | Propagation delay time, from start of CONVERT state to rising edge of BUSY | | | 20 | ns |
| t _{w1} | Pulse duration, $\overline{\text{CONVST}}$ low | 40 | | | ns |
| t _{su1} | Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low | 20 | | | ns |
| t _{w2} | Pulse duration, $\overline{\text{CONVST}}$ high | 20 | | | ns |
| | $\overline{\text{CONVST}}$ falling edge jitter | | | 10 | ps |
| t _{w3} | Pulse duration, BUSY low | Min(t _{ACQ}) | | | μs |
| t _{w4} | Pulse duration, BUSY high | | | 1.52 | μs |
| t _{h1} | Hold time, first data bus data transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS18/16 input changes) after $\overline{\text{CONVST}}$ low | 40 | | | ns |
| t _{d1} | Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low | 0 | | | ns |
| t _{su2} | Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high | 0 | | | ns |
| t _{w5} | Pulse duration, $\overline{\text{RD}}$ low | 50 | | | ns |
| t _{en} | Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid | | | 20 | ns |
| t _{d2} | Delay time, data hold from $\overline{\text{RD}}$ high | 5 | | | ns |
| t _{d3} | Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid | 10 | | 20 | ns |
| t _{w6} | Pulse duration, $\overline{\text{RD}}$ high | 20 | | | ns |
| t _{w7} | Pulse duration, $\overline{\text{CS}}$ high | 20 | | | ns |
| t _{h2} | Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge | 125 | | | ns |
| t _{pd4} | Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge | Max(t _{d5}) | | | ns |
| t _{d4} | Delay time, BYTE edge to BUS18/16 edge skew | 0 | | | ns |
| t _{su3} | Setup time, BYTE or BUS18/16 transition to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t _{h3} | Hold time, BYTE or BUS18/16 transition to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t _{d5} | Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus | | | 20 | ns |
| t _{d5} | Delay time, BUSY low to MSB data valid | | | 30 | ns |
| t _{su5} | Setup time, BYTE transition to next BYTE transition, or BUS18/16 to next BUS18/16 | 50 | | | ns |

(1) All input signals are specified with t_r = t_f = 5 ns (10% to 90% of +VBD) and timed from a voltage level of (V_{IL} + V_{IH})/2.

(2) See timing diagrams.

(3) All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

TIMING CHARACTERISTICS

All specifications typical at -40°C to 85°C, +VA = 5 V, +VBD = 3 V (see Notes 1, 2, and 3)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|-----|------|------|
| t _{CONV} | Conversion time | | | 1.52 | μs |
| t _{ACQ} | Acquisition time | 0.4 | | | μs |
| t _{HOLD} | Hold time, sampling capacitor | | | 25 | ns |
| t _{pd1} | Propagation delay time, $\overline{\text{CONVST}}$ low to conversion started (BUSY high) | | | 50 | ns |
| t _{pd2} | Propagation delay time, end of conversion to BUSY low | | | 25 | ns |
| t _{pd3} | Propagation delay time, start of CONVERT state to rising edge of BUSY | | | 25 | ns |
| t _{w1} | Pulse duration, $\overline{\text{CONVST}}$ low | 40 | | | ns |
| t _{su1} | Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low | 20 | | | ns |
| t _{w2} | Pulse duration, $\overline{\text{CONVST}}$ high | 20 | | | ns |
| | $\overline{\text{CONVST}}$ falling edge jitter | | | 10 | ps |
| t _{w3} | Pulse duration, BUSY low | Min(t _{ACQ}) | | | μs |
| t _{w4} | Pulse duration, BUSY high | | | 1.52 | μs |
| t _{h1} | Hold time, first data bus transition ($\overline{\text{RD}}$ low, or $\overline{\text{CS}}$ low for read cycle, or BYTE or BUS 18/16 input changes) after $\overline{\text{CONVST}}$ low | 40 | | | ns |
| t _{d1} | Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low | 0 | | | ns |
| t _{su2} | Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high | 0 | | | ns |
| t _{w5} | Pulse duration, $\overline{\text{RD}}$ low | 50 | | | ns |
| t _{en} | Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid | | | 30 | ns |
| t _{d2} | Delay time, data hold from $\overline{\text{RD}}$ high | 10 | | | ns |
| t _{d3} | Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid | 10 | | 30 | ns |
| t _{w6} | Pulse duration, $\overline{\text{RD}}$ high | 20 | | | ns |
| t _{w7} | Pulse duration, $\overline{\text{CS}}$ high | 20 | | | ns |
| t _{h2} | Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge | 125 | | | ns |
| t _{pd4} | Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge | Max(td5) | | | ns |
| t _{d4} | Delay time, BYTE edge to BUS18/16 edge skew | 0 | | | ns |
| t _{su3} | Setup time, BYTE or BUS18/16 rising edge to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t _{h3} | Hold time, BYTE or BUS18/16 falling edge to $\overline{\text{RD}}$ falling edge | 10 | | | ns |
| t _{dis} | Disable time, $\overline{\text{RD}}$ High ($\overline{\text{CS}}$ high for read cycle) to 3-stated data bus | | | 30 | ns |
| t _{d5} | Delay time, BUSY low to MSB data valid delay time | | | 40 | ns |
| t _{su5} | Setup time, from BYTE transition to next BYTE transition or from BUS18/16 to next BUS18/16 | 50 | | | ns |

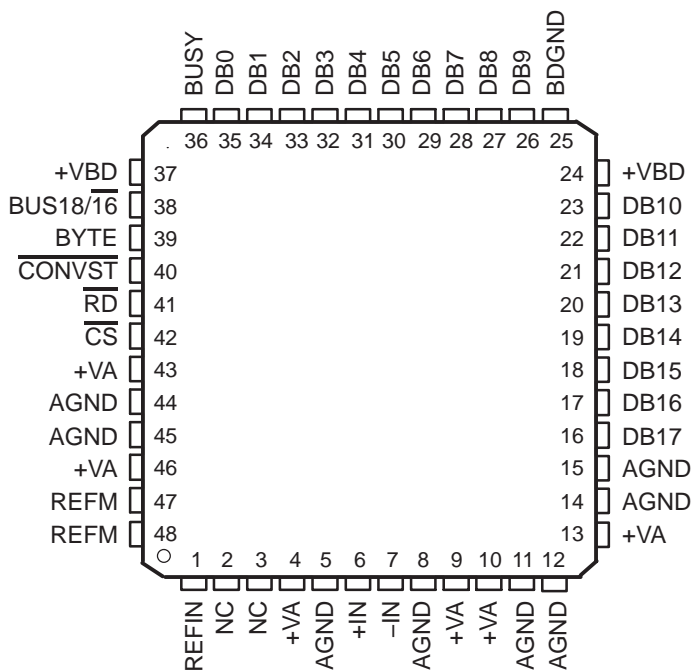
(1) All input signals are specified with t_r = t_f = 5 ns (10% to 90% of +VBD) and timed from a voltage level of (V_{IL} + V_{IH})/2.

(2) See timing diagrams.

(3) All timing are measured with 10 pF equivalent loads on all data bits and BUSY pins.

PIN ASSIGNMENTS

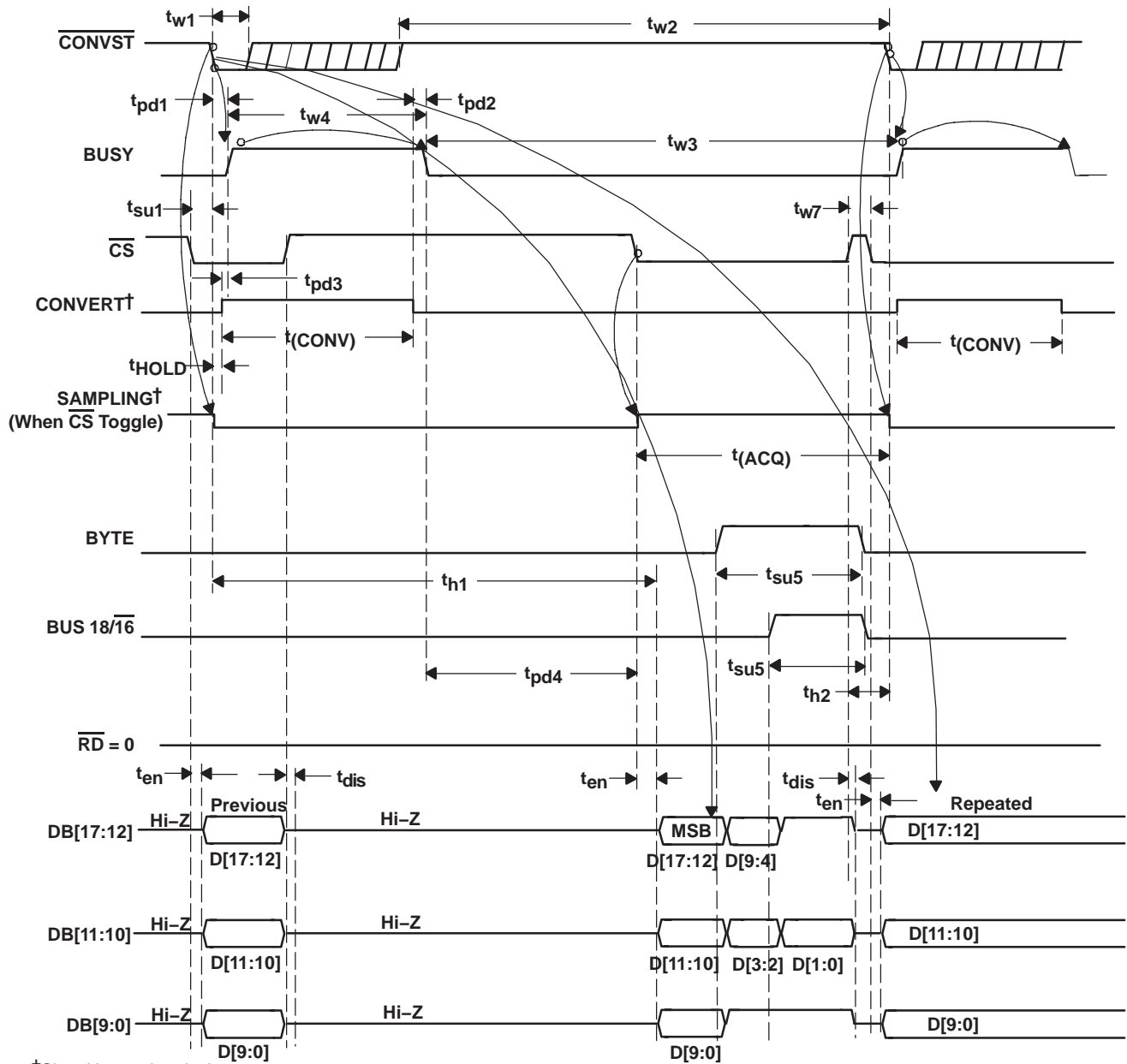
PFB PACKAGE
(TOP VIEW)



NC – No connection.

TERMINAL FUNCTIONS

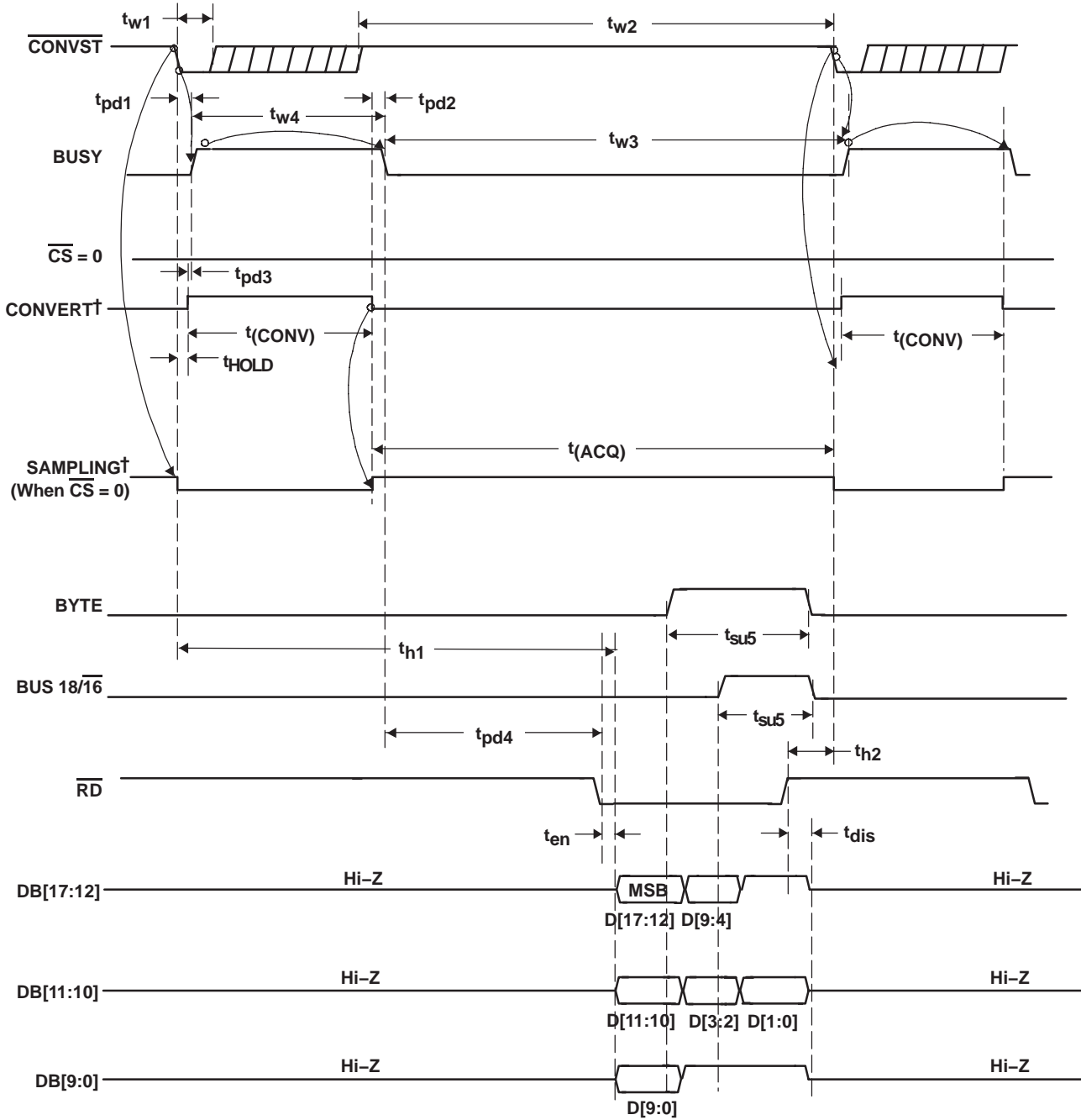
| NAME | NO. | I/O | DESCRIPTION | | | | | |
|----------|------------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|--------------|--------------|--------------|
| AGND | 5, 8, 11, 12, 14, 15, 44, 45 | – | Analog ground | | | | | |
| BDGND | 25 | – | Digital ground for bus interface digital supply | | | | | |
| BUSY | 36 | O | Status output. High when a conversion is in progress. | | | | | |
| BUS18/16 | 38 | I | Bus size select input. Used for selecting 18-bit or 16-bit wide bus transfer. 0: Data bits output on the 18-bit data bus pins DB[17:0]. 1: Last two data bits D[1:0] from 18-bit wide bus output on: a) the low byte pins DB[9:2] if BYTE = 0 b) the high byte pins DB[17:10] if BYTE = 1 | | | | | |
| BYTE | 39 | I | Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Low byte D[9:2] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[17:10]. | | | | | |
| CONVST | 40 | I | Convert start. The falling edge of this input ends the acquisition period and starts the hold period. | | | | | |
| CS | 42 | I | Chip select. The falling edge of this input starts the acquisition period | | | | | |
| Data Bus | | | 8-Bit Bus | | | 16-Bit Bus | | 18-Bit Bus |
| | | | BYTE = 0 | BYTE = 1 | BYTE = 1 | BYTE = 0 | BYTE = 0 | BYTE = 0 |
| | | | BUS18/16 = 0 | BUS18/16 = 0 | BUS18/16 = 1 | BUS18/16 = 0 | BUS18/16 = 1 | BUS18/16 = 0 |
| DB17 | 16 | O | D17 (MSB) | D9 | All ones | D17 (MSB) | All ones | D17 (MSB) |
| DB16 | 17 | O | D16 | D8 | All ones | D16 | All ones | D16 |
| DB15 | 18 | O | D15 | D7 | All ones | D15 | All ones | D15 |
| DB14 | 19 | O | D14 | D6 | All ones | D14 | All ones | D14 |
| DB13 | 20 | O | D13 | D5 | All ones | D13 | All ones | D13 |
| DB12 | 21 | O | D12 | D4 | All ones | D12 | All ones | D12 |
| DB11 | 22 | O | D11 | D3 | D1 | D11 | All ones | D11 |
| DB10 | 23 | O | D10 | D2 | D0(LSB) | D10 | All ones | D10 |
| DB9 | 26 | O | D9 | All ones | All ones | D9 | All ones | D9 |
| DB8 | 27 | O | D8 | All ones | All ones | D8 | All ones | D8 |
| DB7 | 28 | O | D7 | All ones | All ones | D7 | All ones | D7 |
| DB6 | 29 | O | D6 | All ones | All ones | D6 | All ones | D6 |
| DB5 | 30 | O | D5 | All ones | All ones | D5 | All ones | D5 |
| DB4 | 31 | O | D4 | All ones | All ones | D4 | All ones | D4 |
| DB3 | 32 | O | D3 | All ones | All ones | D3 | D1 | D3 |
| DB2 | 33 | O | D2 | All ones | All ones | D2 | D0 (LSB) | D2 |
| DB1 | 34 | O | D1 | All ones | All ones | D1 | All ones | D1 |
| DB0 | 35 | O | D0 (LSB) | All ones | All ones | D0 (LSB) | All ones | D0 (LSB) |
| –IN | 7 | I | Inverting input channel | | | | | |
| +IN | 6 | I | Noninverting input channel | | | | | |
| NC | 2, 3 | – | No connection | | | | | |
| REFIN | 1 | I | Reference input. | | | | | |
| REFM | 47, 48 | I | Reference ground. | | | | | |
| RD | 41 | I | Synchronization pulse for the parallel output. When CS is low this serves as output enable. | | | | | |
| +VA | 4, 9, 10, 13, 43, 46 | – | Analog power supplies, 5-V dc | | | | | |
| +VBD | 24, 37 | – | Digital power supply for bus | | | | | |



†Signal internal to device

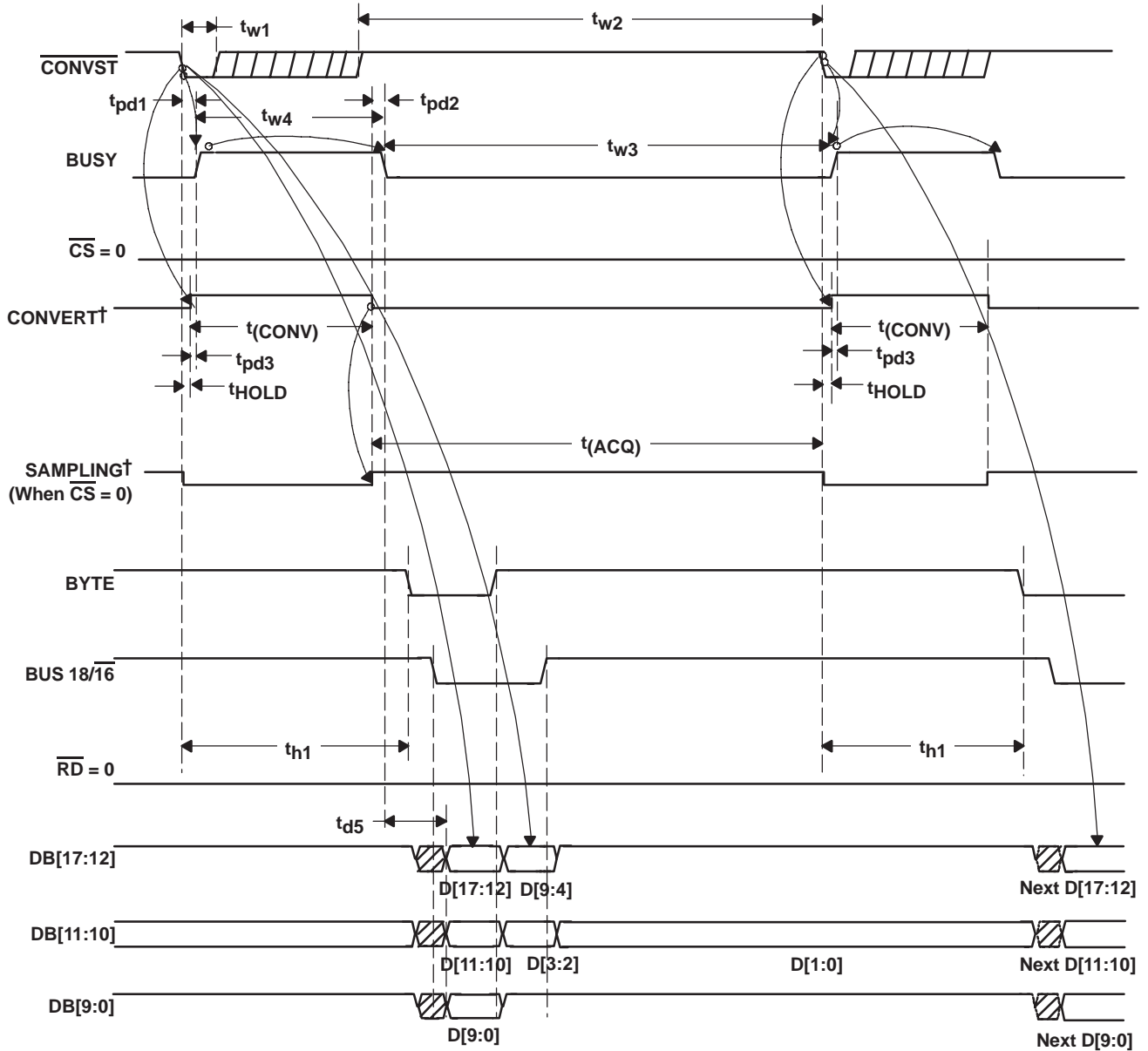
NOTE: $\overline{\text{RD}}$ cannot be tied to BDGND. Three read cycles are required at power on.

Figure 2. Timing for Conversion and Acquisition Cycles With $\overline{\text{CS}}$ Toggling, $\overline{\text{RD}}$ Held at BDGND After Power-On Initialization



† Signal internal to device

Figure 3. Timing for Conversion and Acquisition Cycles With $\overline{\text{CS}}$ Tied to BDGND , $\overline{\text{RD}}$ Toggling



†Signal internal to device

NOTE: \overline{RD} cannot be tied to BDGND. Three read cycles are required at power on.

Figure 4. Timing for Conversion and Acquisition Cycles With \overline{CS} and \overline{RD} Held at BDGND After Power-On Initialization - Auto Read

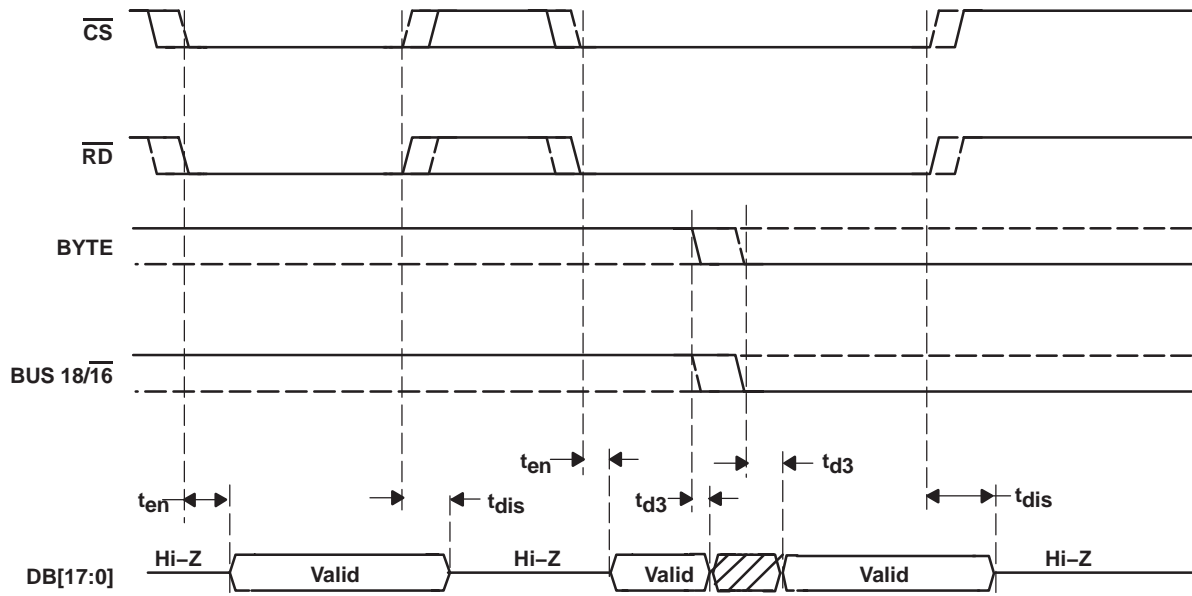


Figure 5. Detailed Timing for Read Cycles

TYPICAL CHARACTERISTICS†

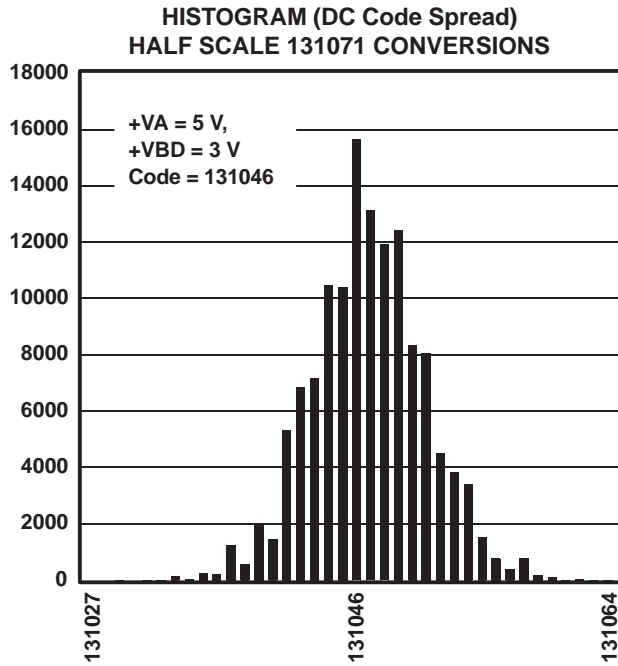


Figure 6

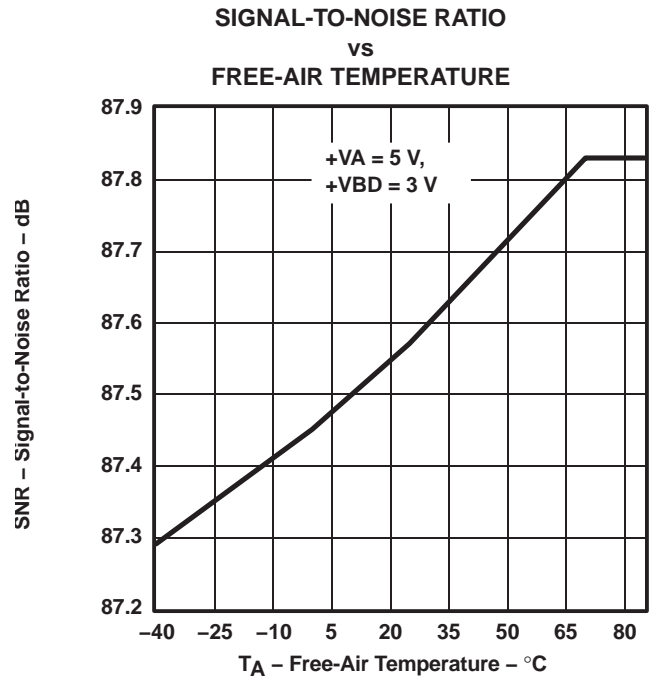


Figure 7

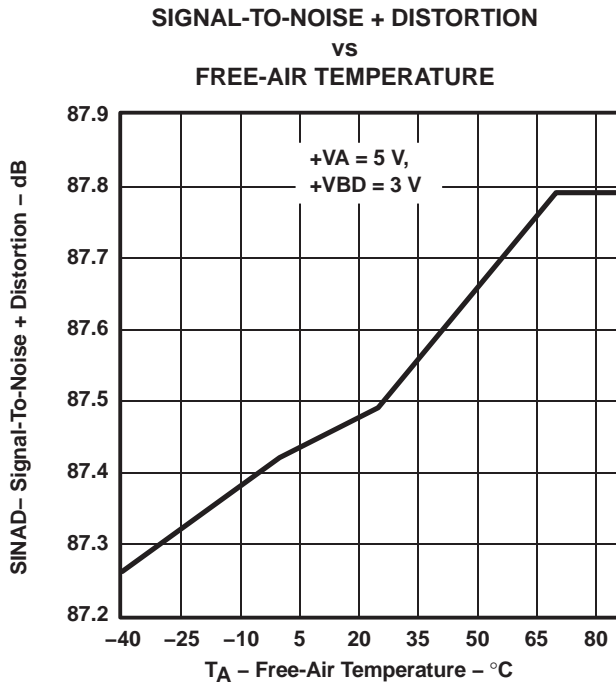


Figure 8

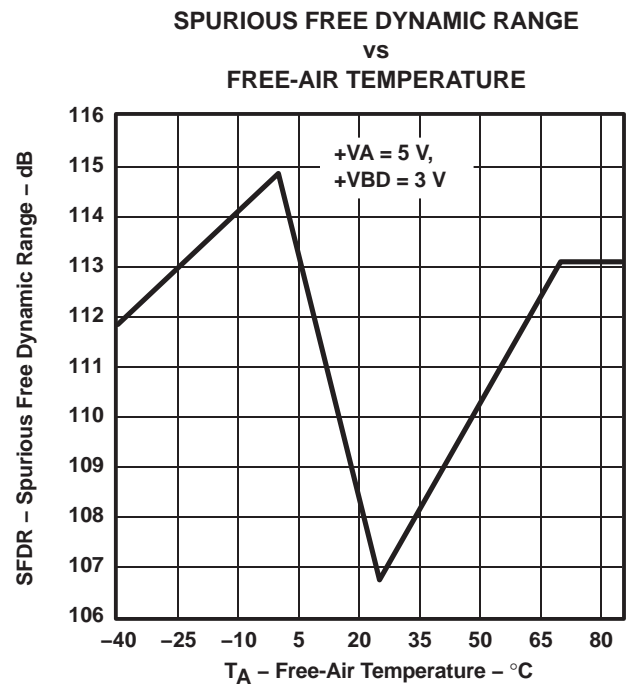


Figure 9

† At -40°C to 85°C , $+V_A = 5\text{ V}$, $+V_{BD} = 5\text{ V}$, $\text{REFIN} = 4.096\text{ V}$ and $f_{\text{sample}} = 500\text{ kHz}$ (unless otherwise noted)

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREE-AIR TEMPERATURE

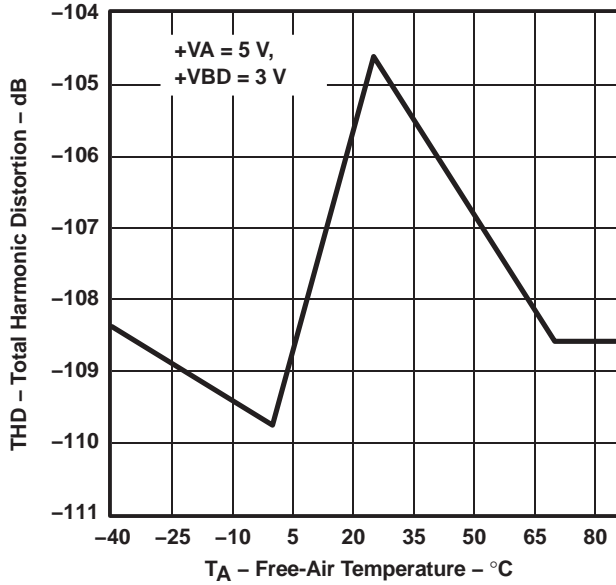


Figure 10

EFFECTIVE NUMBER OF BITS
vs
FREE-AIR TEMPERATURE

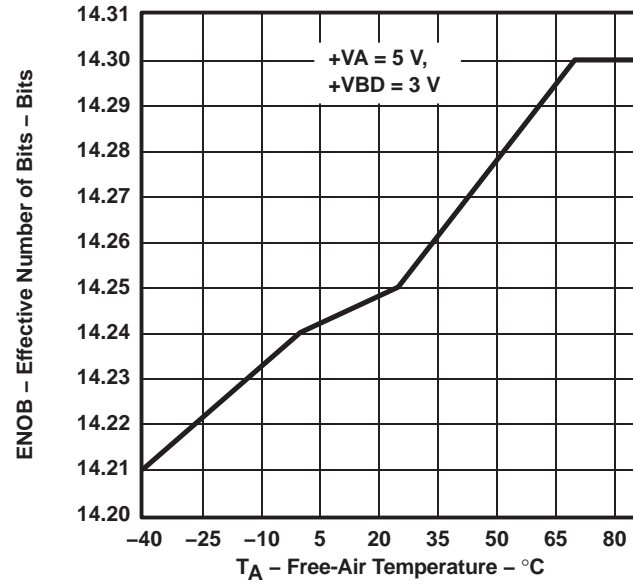


Figure 11

SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY

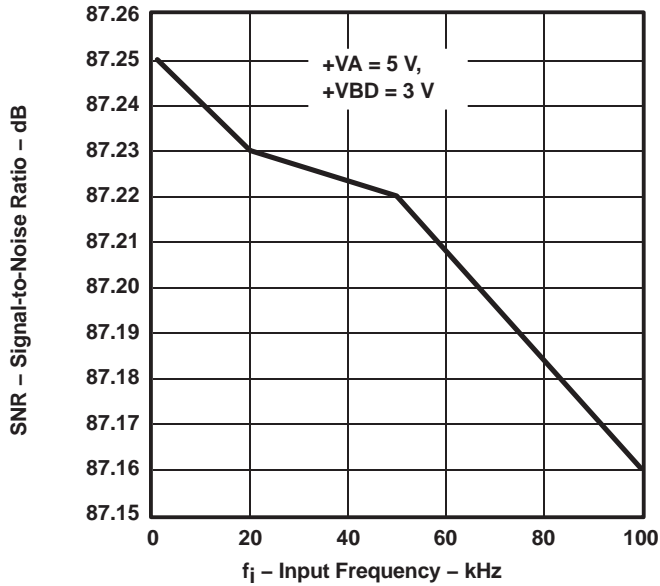


Figure 12

SIGNAL-TO-NOISE + DISTORTION
vs
INPUT FREQUENCY

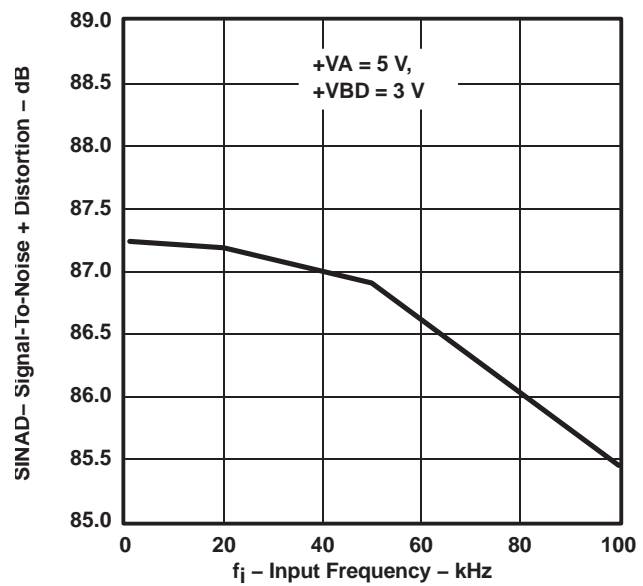


Figure 13

† At -40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and $f_{\text{sample}} = 500$ kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

EFFECTIVE NUMBER OF BITS
vs
INPUT FREQUENCY

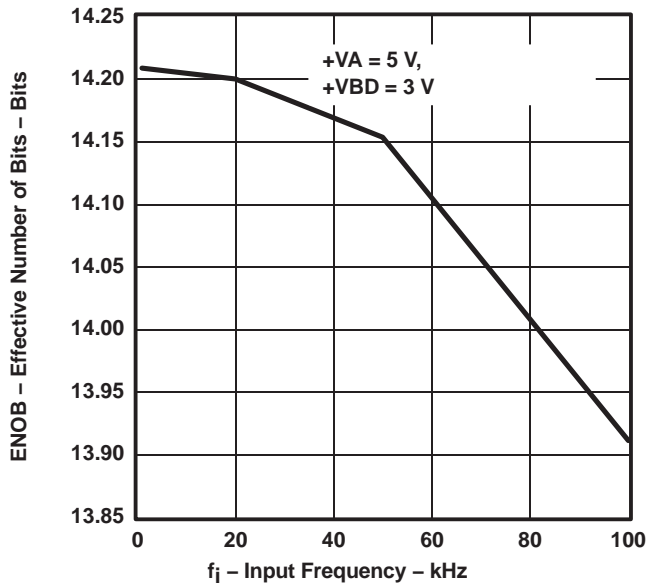


Figure 14

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY

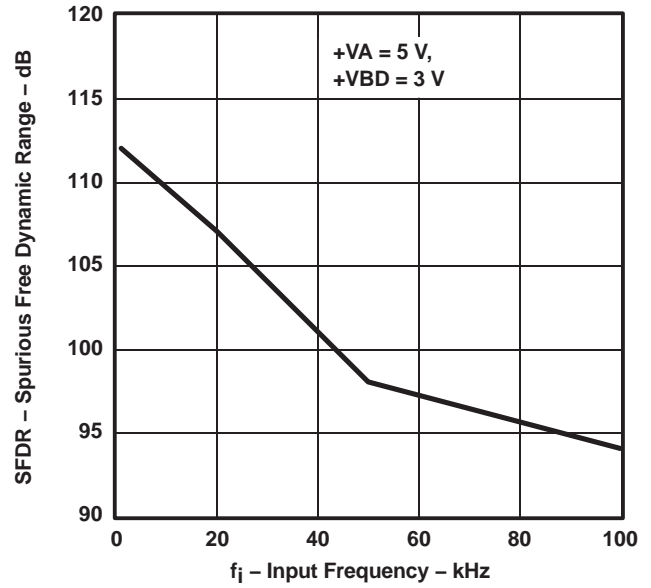


Figure 15

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

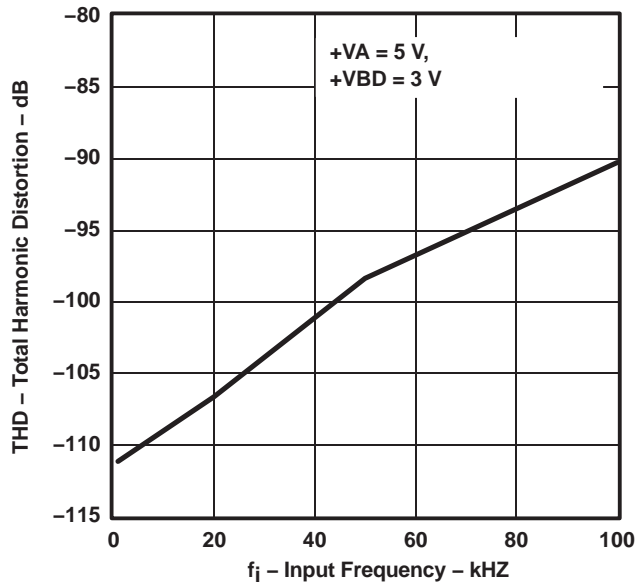


Figure 16

SUPPLY CURRENT
vs
SAMPLE RATE

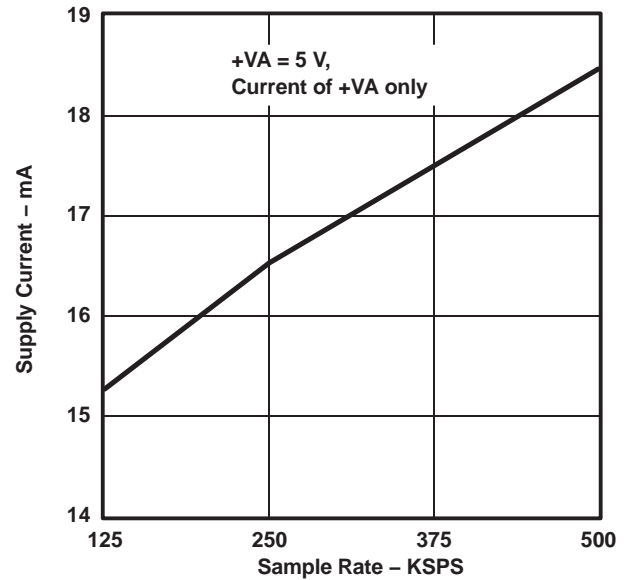


Figure 17

† At -40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and $f_{\text{sample}} = 500$ kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

INTEGRAL NONLINEARITY
vs
SAMPLE RATE

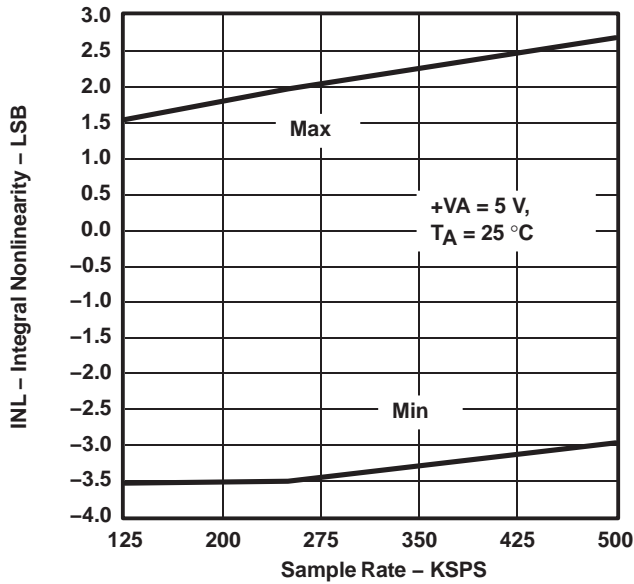


Figure 18

DIFFERENTIAL NONLINEARITY
vs
SAMPLE RATE

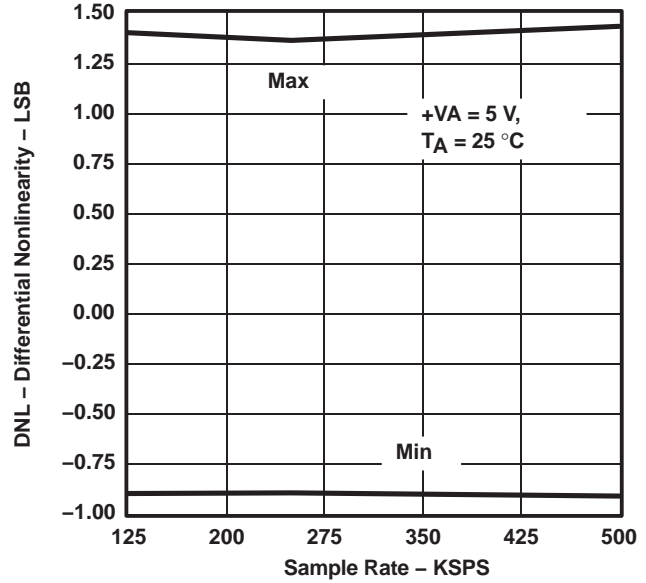


Figure 19

GAIN ERROR
vs
SUPPLY VOLTAGE

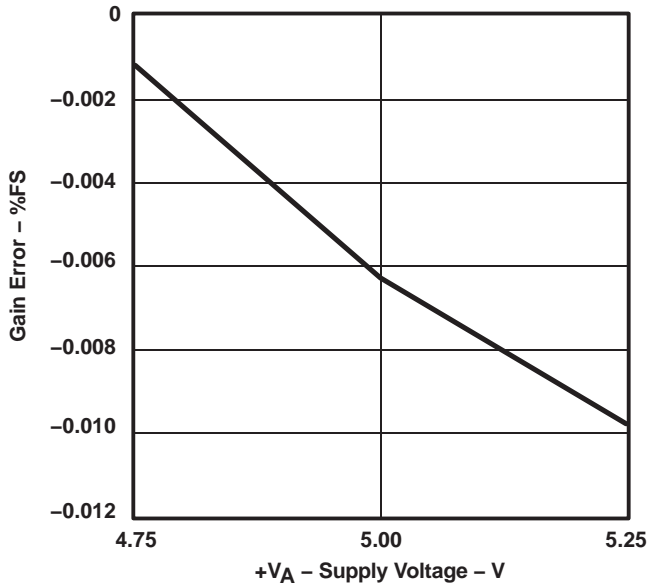


Figure 20

OFFSET VOLTAGE
vs
SUPPLY VOLTAGE

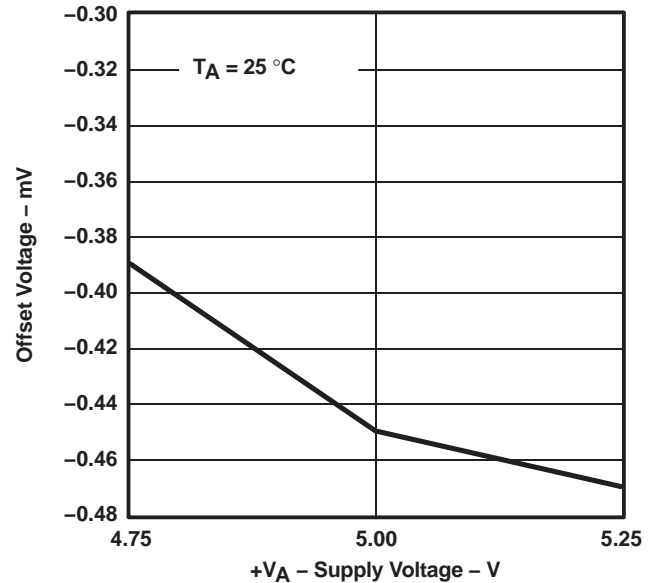


Figure 21

† At -40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

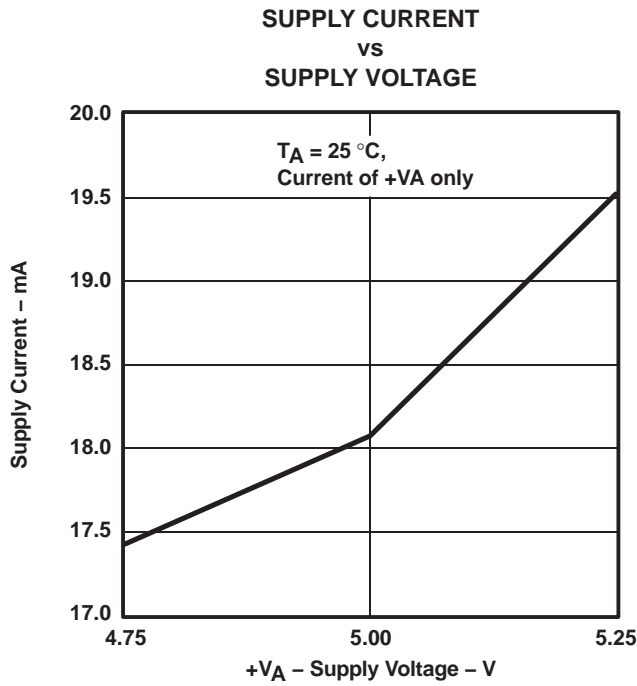


Figure 22

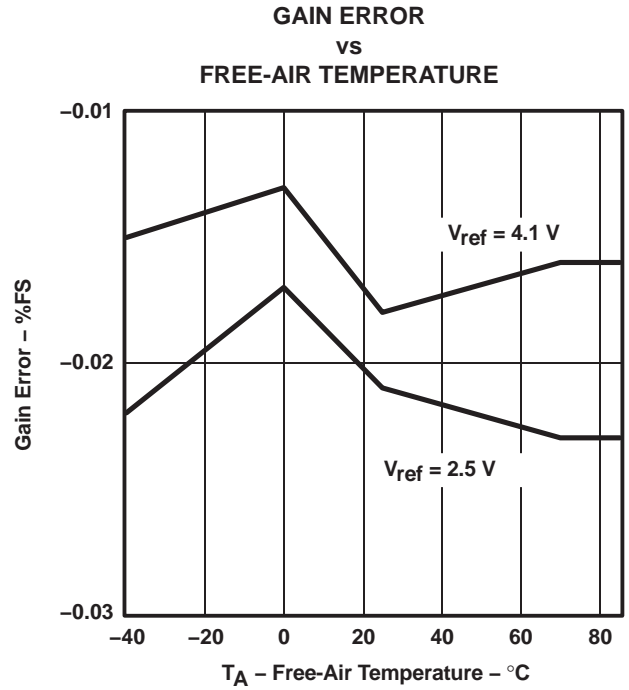


Figure 23

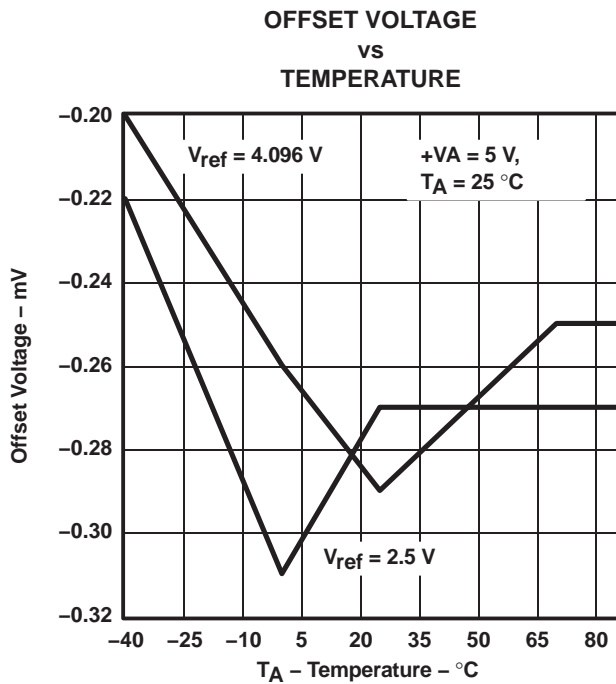


Figure 24

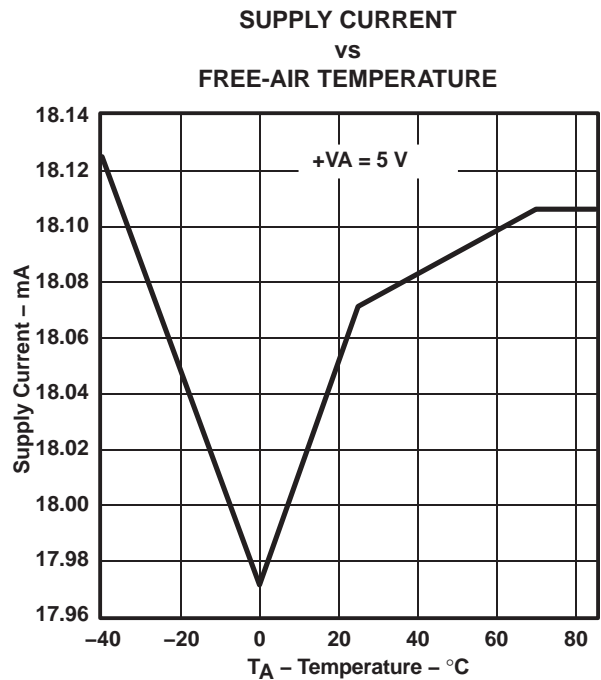


Figure 25

† At -40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

DIFFERENTIAL NONLINEARITY (Max)
vs
TEMPERATURE

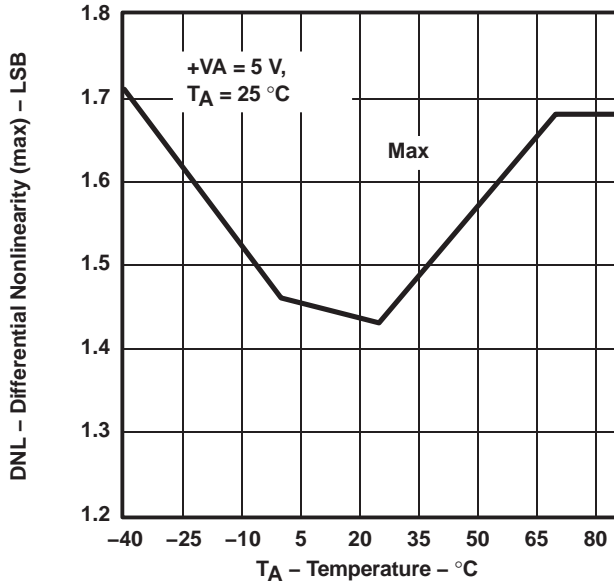


Figure 26

DIFFERENTIAL NONLINEARITY (Min)
vs
TEMPERATURE

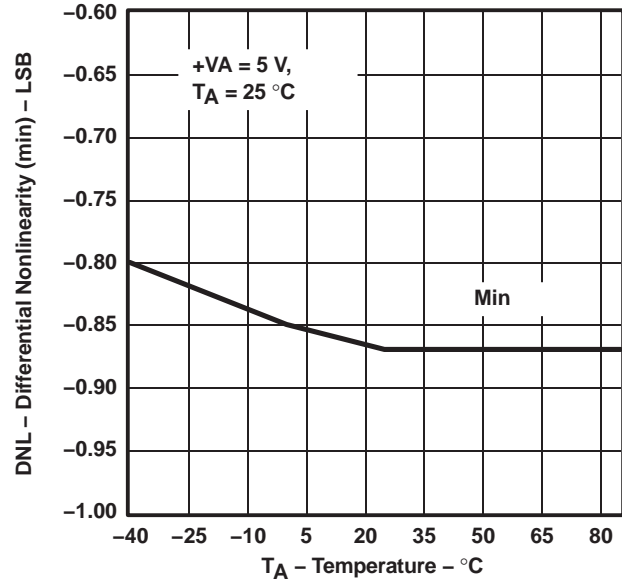


Figure 27

INTEGRAL NONLINEARITY (Max)
vs
TEMPERATURE

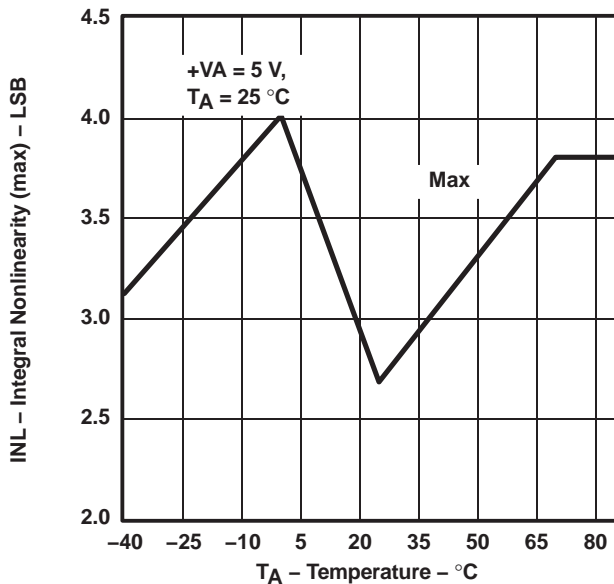


Figure 28

INTEGRAL NONLINEARITY (Min)
vs
TEMPERATURE

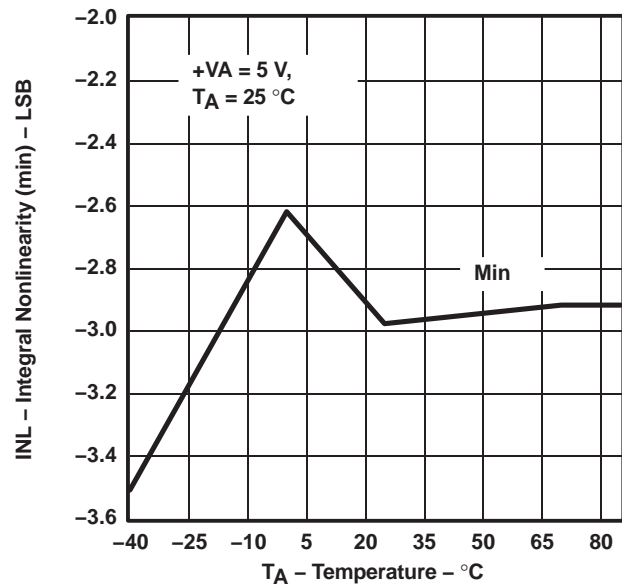


Figure 29

† At -40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

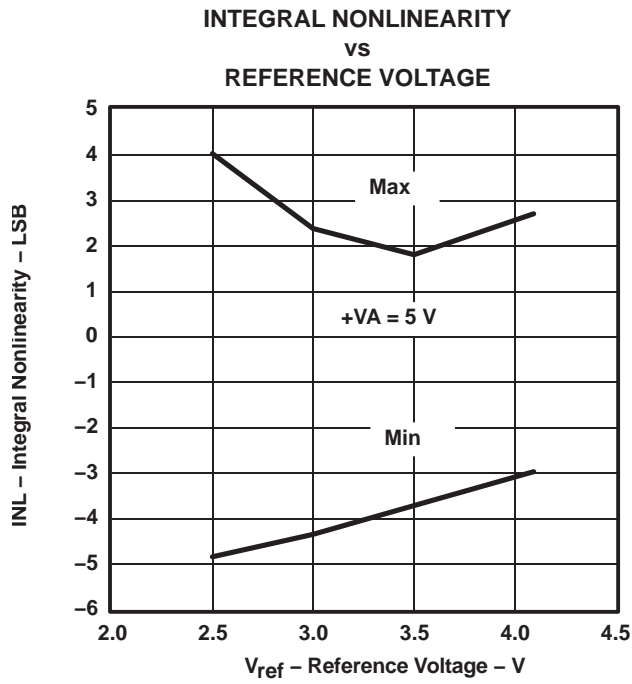


Figure 30

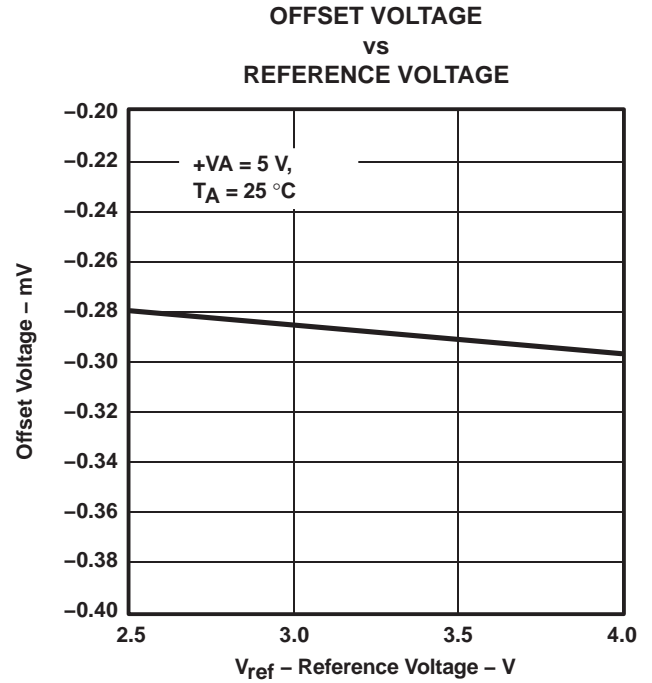


Figure 31

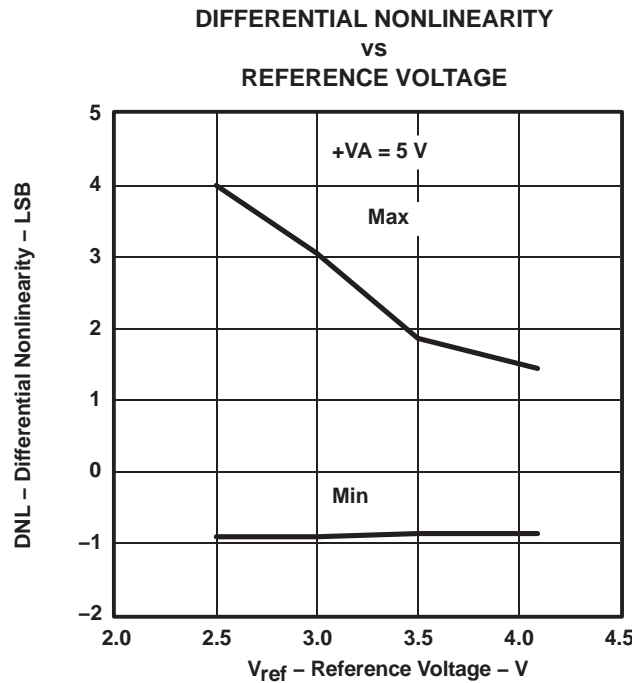


Figure 32

† At -40°C to 85°C, +VA = 5 V, +VBD = 5 V, REFIN = 4.096 V and f_{sample} = 500 kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

DIFFERENTIAL LINEARITY ERROR
vs
CODE

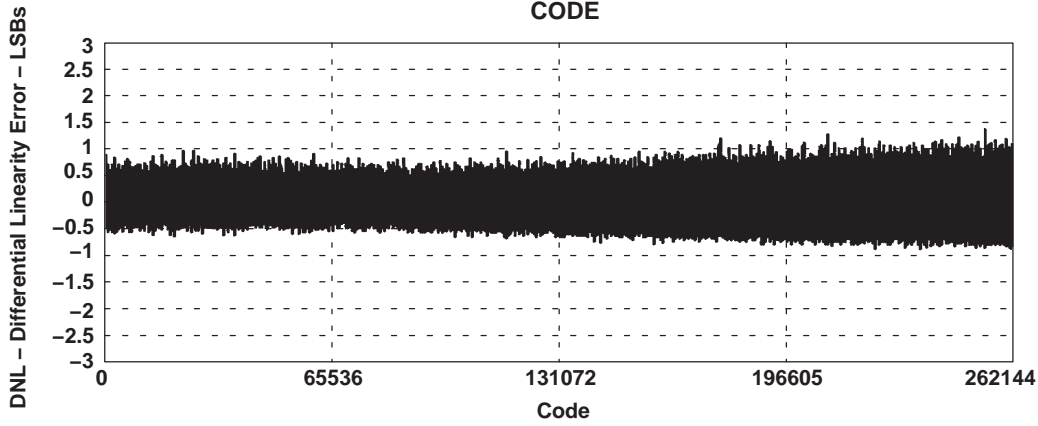


Figure 33

INTEGRAL LINEARITY ERROR
vs
CODE

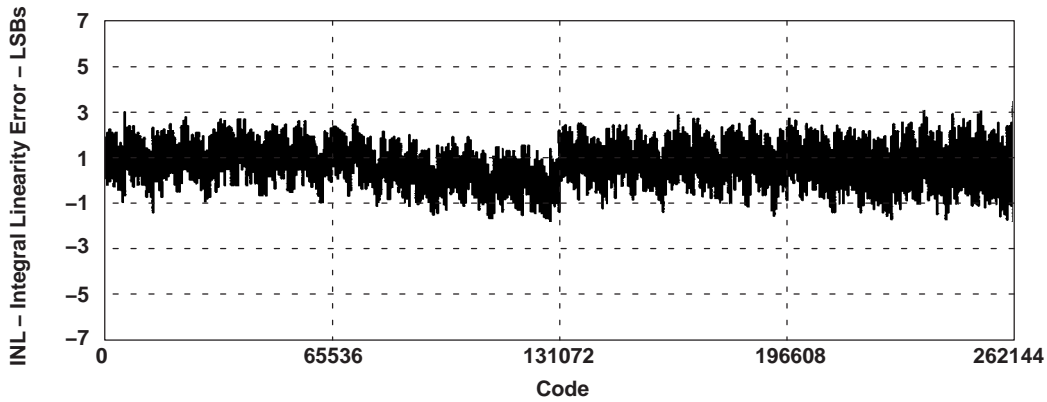


Figure 34

FFT SPECTRAL RESPONSE (100 kHz Input)

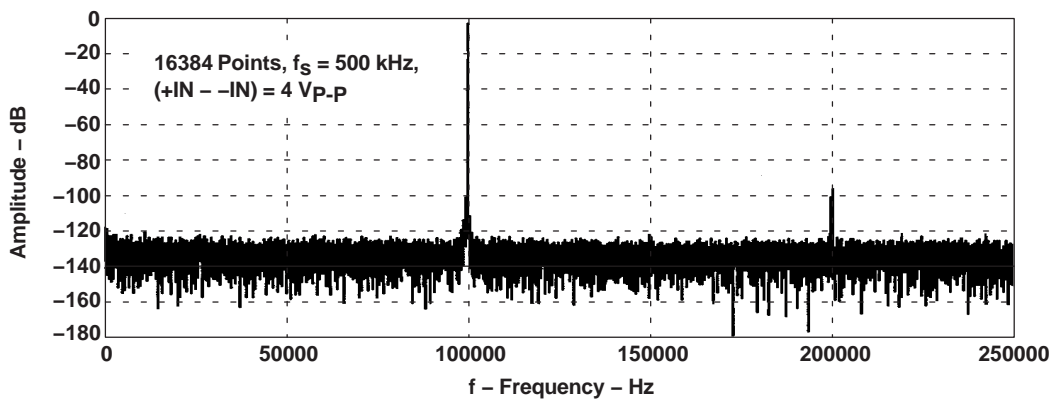


Figure 35

† At -40°C to 85°C , $+V_A = 5$ V, $+V_{BD} = 5$ V, $\text{REFIN} = 4.096$ V and $f_{\text{sample}} = 500$ kHz (unless otherwise noted)

TYPICAL CHARACTERISTICS†

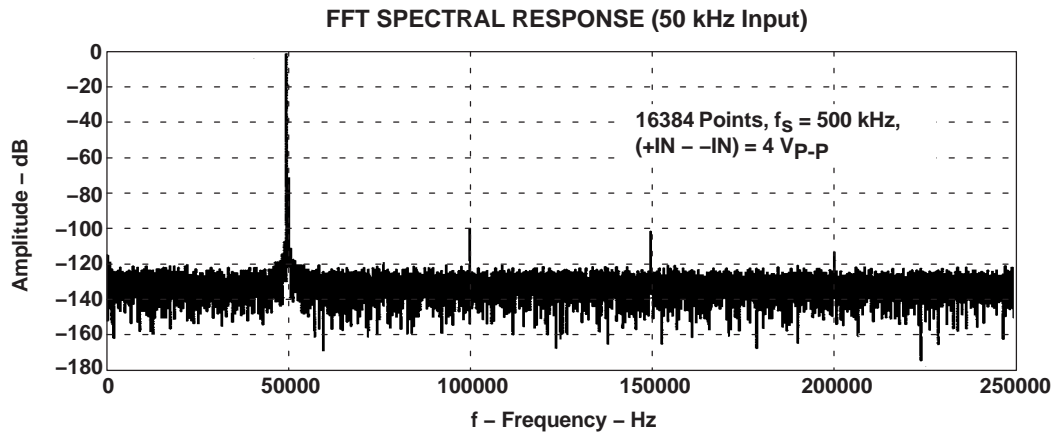


Figure 36

† At -40°C to 85°C , $+V_A = 5$ V, $+V_{BD} = 5$ V, $\text{REFIN} = 4.096$ V and $f_{\text{sample}} = 500$ kHz (unless otherwise noted)

APPLICATION INFORMATION

MICROCONTROLLER INTERFACING

ADS8383 to 8-Bit Microcontroller Interface

Figure 37 shows a parallel interface between the ADS8383 and a typical microcontroller using the 8-bit data bus. The BUSY signal is used as a falling-edge interrupt to the microprocessor.

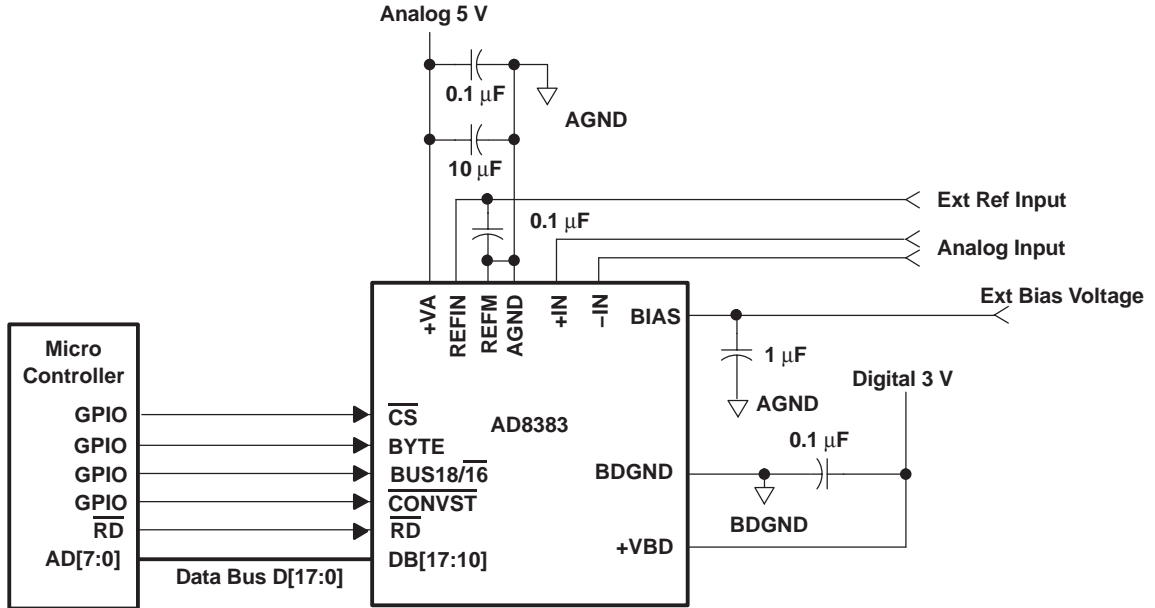


Figure 37. ADS8383 Application Circuitry

PRINCIPLES OF OPERATION

The ADS8383 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 37 for the application circuit for the ADS8383.

The conversion clock is generated internally. The conversion time of 1.52 μs is capable of sustaining a 500-kHz throughput.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8383 can operate with an external 4.096-V reference for a corresponding full-scale range of 4.096 V.

BIASING THE ADS8383

The ADS8383 requires an external 2.048-V bandgap reference to generate the bias currents for internal circuitry. Figure 38 shows the internal circuitry used to generate the bias currents. The bias generation circuit also pumps 100 μA (150 μA max) out from the BIAS pin. The bandgap used should be capable of sinking 100 μA (150 μA max) while holding the voltage on the pin steady. Table 1 shows the specification of the bandgap used to drive the BIAS pin of the ADS8383.

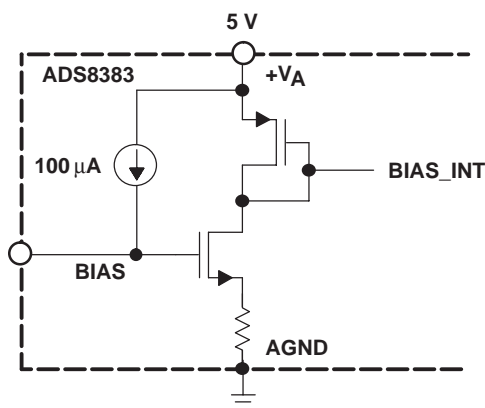


Figure 38. Bias Current Generation

Table 1. Bias Specifications

| PARAMETER | MIN | TYP | MAX | UNITS |
|-------------------|-----|-------|-----|---------------|
| Output Voltage | 2 | 2.048 | 2.1 | V |
| I_{sink} | | 100 | 150 | μA |

Any common bandgap like REF3020 can be used to drive the BIAS pin of the ADS8383. Figure 39 shows how REF3020 can be used with the ADS8383. A 1 μF decoupling capacitor is recommended between pins 2 and AGND of the ADS8383 for optimal performance.

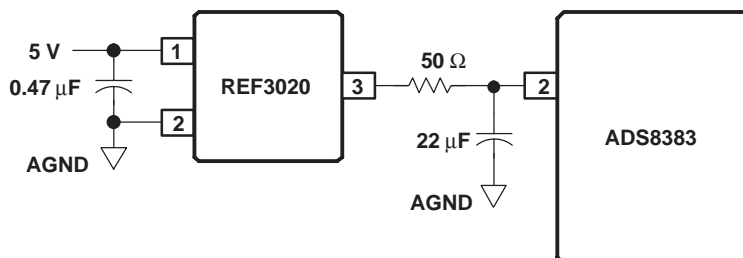


Figure 39. Using the REF3020 to Drive the ADS8383 BIAS Pin

ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2 V and 0.2 V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.2 V to $V_{ref} + 0.2$ V. The input span (+IN – (–IN)) is limited to 0 V to V_{ref} .

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8383 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45 pF) to an 18-bit settling level within the acquisition time (400 ns) of the device. When the converter goes into the hold mode, the input impedance is greater than 1 G Ω .

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN and –IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

DIGITAL INTERFACE

Timing And Control

See the timing diagrams in the specifications section for detailed information on timing signals and their requirements.

The ADS8383 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high), while $\overline{\text{CS}}$ is low. The ADS8383 switches from the sample to the hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY output is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high through the conversion process and returns low when the conversion has ended.

Sampling starts with the falling edge of the BUSY signal when $\overline{\text{CS}}$ is tied low or starts with the falling edge of $\overline{\text{CS}}$ when BUSY is low.

Both $\overline{\text{RD}}$ and $\overline{\text{CS}}$ can be high during and before a conversion with one exception ($\overline{\text{CS}}$ must be low when $\overline{\text{CONVST}}$ goes low to initiate a conversion). Both the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ pins are brought low in order to enable the parallel output bus with the conversion.

Reading Data

The ADS8383 outputs full parallel data in straight binary format as shown in Table 2. The parallel output is active when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{\text{CONVST}}$. This is 125 ns prior to the falling edge of $\overline{\text{CONVST}}$ and 40 ns after the falling edge. No data read should be attempted within this zone. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ sets the parallel output to 3-state. BYTE and BUS18/16 are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/16 is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 2 for ideal output codes.

Table 2. Ideal Input Voltages and Output Codes

| DESCRIPTION | ANALOG VALUE | DIGITAL OUTPUT STRAIGHT BINARY | |
|-----------------------------|------------------------------|--------------------------------|----------|
| | | BINARY CODE | HEX CODE |
| Full scale range | +V _{ref} | | |
| Least significant bit (LSB) | +V _{ref} /262144 | | |
| Full scale | +V _{ref} – 1 LSB | 11 1111 1111 1111 1111 | 3FFFF |
| Midscale | +V _{ref} /2 | 10 0000 0000 0000 0000 | 20000 |
| Midscale – 1 LSB | +V _{ref} /2 – 1 LSB | 01 1111 1111 1111 1111 | 1FFFF |
| Zero | 0 V | 00 0000 0000 0000 0000 | 00000 |

The output data is a full 18-bit word (D17–D0) on DB17–DB0 pins (MSB–LSB) if both BUS18/16 and BYTE are low.

The result may also be read on a 16-bit bus by using only pins DB17–DB2. In this case two reads are necessary: the first as before, leaving both BUS18/16 and BYTE low and reading the 16 most significant bits (D17–D2) on pins DB17–DB2, then bringing BUS18/16 high while holding BYTE low. When BUS18/16 is high, the lower two bits (D1–D0) appear on pins DB3–DB2.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17–DB10. In this case three reads are necessary: the first as before, leaving both BUS18/16 and BYTE low and reading the 8 most significant bits on pins DB17–DB10, then bringing BYTE high while holding BUS18/16 low. When BYTE is high, the medium bits (D9–D2) appear on pins DB17–DB10. The last read is done by bringing BUS18/16 high while holding BYTE high. When BUS18/16 is high, the lower two bits (D1–D0) appear on pins DB11–DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active \overline{RD} (toggling) or with \overline{RD} held low for simplicity. This is referred to as the AUTO READ operation. Note that \overline{RD} may not be tied to BDGND permanently due to the requirement of power-on initialization.

Table 3. Conversion Data Read Out

| BYTE | BUS18/16 | DATA READ OUT | | | | |
|------|----------|----------------|----------------|--------------|--------------|--------------|
| | | DB17–DB12 PINS | DB11–DB10 PINS | DB9–DB4 PINS | DB3–DB2 PINS | DB1–DB0 PINS |
| High | High | All One's | D1–D0 | All One's | All One's | All One's |
| Low | High | All One's | All One's | All One's | D1–D0 | All One's |
| High | Low | D9–D4 | D3–D2 | All One's | All One's | All One's |
| Low | Low | D17–D12 | D11–D10 | D9–D4 | D3–D2 | D1–D0 |

INITIALIZATION

At first power on there are three conversion cycles required. If an ANT conversion cycle is attempted before the initialization is completed, the first three conversion cycles will not produce valid results. These are used to load factory trimming data for a specific device to ensure high accuracy of the converter. Because of this requirement, the \overline{RD} pin cannot be tied permanently to BDGND. System designers can still achieve the AUTO READ function if the power-on requirement is satisfied.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8383 circuitry.

As the ADS8383 offers single-supply operation, it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are at least n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8383 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1- μ F bypass capacitor is recommended from pin 1 (REFIN) directly to pin 48 (REFM). REFM and AGND should be shorted on the same ground plane under the device.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8383 should be clean and well bypassed. A 0.1- μ F ceramic bypass capacitor should be placed as close to the device as possible. See Table 4 for the placement of the capacitor. In addition, a 1- μ F to 10- μ F capacitor is recommended. In some situations, additional bypassing may be required, such as a 100- μ F electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 4. Power Supply Decoupling Capacitor Placement

| POWER SUPPLY PLANE | CONVERTER ANALOG SIDE | CONVERTER DIGITAL SIDE |
|---------------------------------------------------------------|-----------------------------------------------------|------------------------|
| SUPPLY PINS | | |
| Pin pairs that require shortest path to decoupling capacitors | (4,5), (8,9), (10,11), (13,15), (43,44), (45,46) | (24,25) |
| Pins that require no decoupling | 12, 14 | 37 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|----------------|
| ADS8383IBPFBT | ACTIVE | TQFP | PFB | 48 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | ADS8383I B | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PFB (S-PQFP-G48)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PFB (S-PQFP-G48)



4209366/A 03/08

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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