

## BQ25173: 适用于 1-4 芯超级电容器的 800mA 线性电池充电器

### 1 特性

- 可承受高达 40V 的输入电压
- 自动睡眠模式，可降低功耗
  - 350nA 泄漏电流
  - 禁用充电时，输入泄漏电流为 2 $\mu$ A
- 支持 1-4 芯超级电容器
- 支持从 0V 为超级电容器充电
- 操作可使用外部电阻器进行编程
  - FB 引脚用于调节超级电容器稳压电压
  - ISET 用于设置 10mA 至 800mA 的充电电流
- 高精度
  - 充电电压精度为  $\pm 1\%$
  - 充电电流精度为  $\pm 10\%$
- 充电特性
  - $\overline{CE}$  引脚用于充电功能控制
  - 用于状态和故障指示的开漏输出
  - 用于电源正常指示的开漏输出
- 集成故障保护
  - 18V 输入过压保护
  - 1000mA 过流保护
  - 125°C 热调节；150°C 热关断保护
  - OUT 短路保护
  - ISET 引脚短路/开路保护

### 2 应用

- 智能仪表
- 条形码扫描仪
- 便携式医疗设备
- 仪表板摄像头

### 3 说明

BQ25173 是一款集成式 800mA 线性充电器，适用于面向空间受限型应用的 1-4 芯超级电容器。该器件具有为超级电容器充电的单电源输出。可以将系统负载与超级电容器并联；充电电流由系统和超级电容器共享。

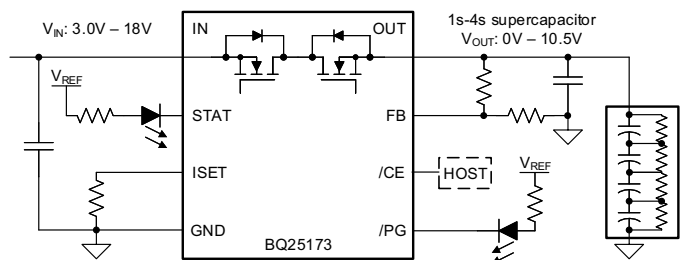
在充电期间，内部控制环路会监视 IC 结温并在超过内部温度阈值  $T_{REG}$  时减小充电电流。此功能可为完全放电的超级电容器提供快速充电。

充电器功率级和充电电流感测功能均完全集成。该充电器具有高精度电流和电压调节环路功能、充电状态显示和充电功能控制。充电电压和快速充电电流可通过外部电阻编程设定。

#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
BQ25173	WSON (8)	2.0mm x 2.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



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## 4 Revision History

DATE	REVISION	NOTES
November 2021	*	Initial Release

## 5 Pin Configuration and Functions

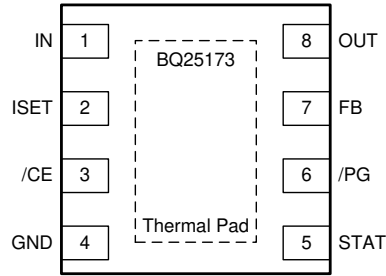


图 5-1. DSG (WSON) Package 8-Pin Top View

表 5-1. Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
IN	1	P	Input power. Connect to external DC supply. Bypass IN with at least 1- $\mu$ F capacitor to GND, placed close to the IC.
ISET	2	I	Programs the device fast-charge current, $I_{CHG}$ . External resistor from ISET to GND defines fast-charge current value. Expected range is 30 k $\Omega$ (10 mA) to 375 $\Omega$ (800 mA). $I_{CHG} = K_{ISET} / R_{ISET}$ .
CE	3	I	Active low charge enable pin. Charging is enabled when the CE pin is LOW. IC remains in Shutdown mode and charging is disabled when the CE pin is HIGH. An internal pulldown resistor ( $R_{PD\_CE}$ ) enables the IC by default if this pin is floating.
GND	4	-	Ground pin.
STAT	5	O	Open-drain charger status indication output. Connect to pullup rail with a 10-k $\Omega$ resistor. LOW indicates $V_{OUT}$ has reached 98% of the programmable regulation voltage, $V_{REG}$ . HIGH indicates charge in progress.
PG	6	O	Open-drain charger power-good output. Connect to pullup rail with a 10-k $\Omega$ resistor. $\overline{PG}$ goes LOW when $V_{IN} > V_{IN\_LOWV}$ and $V_{OUT} + V_{SLEEPZ} < V_{IN} < V_{IN\_OV}$ .
FB	7	I	Programs the supercapacitor regulation voltage, $V_{REG}$ . Use a feedback divider not exceeding 1 M $\Omega$ from $V_{OUT}$ to GND to set the regulation voltage. The bottom of the resistor divider network can be connected to $\overline{PG}$ for reduced power consumption when the input is removed (for $V_{REG} \leq 5$ V).
OUT	8	P	Supercapacitor connection. System load may be connected in parallel with supercapacitor. Bypass OUT with at least 1- $\mu$ F capacitor to GND, placed close to the IC.
Thermal Pad	—	P	Exposed pad beneath the IC for heat dissipation. Solder thermal pad to the board with vias connecting to solid GND plane.

(1) I = Input, O = Output, P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	IN	- 0.3	40	V
Voltage	OUT	- 0.3	13	V
Voltage	$\overline{CE}$ , FB, ISET, STAT, $\overline{PG}$	- 0.3	5.5	V
Output Sink Current	$\overline{PG}$ , STAT		5	mA
Junction temperature, $T_J$		- 40	150	°C
Storage temperature, $T_{stg}$		- 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device may reduce reliability, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001 <sup>(1)</sup>	±2500	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	3.0		18	V
$V_{OUT}$	Output voltage	0		10.5	V
$I_{OUT}$	Output current			0.8	A
$T_J$	Junction temperature	- 40		125	°C
$C_{IN}$	IN capacitor	1			μF
$C_{OUT}$	OUT capacitor	1			μF
$R_{ISET}$	ISET resistor	0.375		30	kΩ

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		BQ25173	UNIT
		DSG (WSON)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC <sup>(1)</sup> )	75.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	3.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	41.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.0	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

3.0V < V<sub>IN</sub> < 18V and V<sub>IN</sub> > V<sub>OUT</sub> + V<sub>SLEEP</sub>, T<sub>J</sub> = -40°C to +125°C, and T<sub>J</sub> = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>QUIESCENT CURRENTS</b>						
I <sub>Q_OUT</sub>	Quiescent output current (OUT)	OUT = 4.2V, IN floating or IN = 0V - 5V, Charge Disabled ( $\overline{CE}$ high), T <sub>J</sub> = 25 °C	0.350	0.6		μA
		OUT = 4.2V, IN floating or IN = 0V - 5V, Charge Disabled ( $\overline{CE}$ high), T <sub>J</sub> < 105 °C	0.350	0.8		μA
I <sub>Q_OUT</sub>	Quiescent output current (OUT)	OUT = 8.4V, IN floating or IN = 0V - 14V, Charge Disabled ( $\overline{CE}$ high), T <sub>J</sub> = 25 °C	0.8	1.2		μA
		OUT = 8.4V, IN floating or IN = 0V - 14V, Charge Disabled ( $\overline{CE}$ high), T <sub>J</sub> < 105 °C	0.8	1.5		μA
I <sub>SD_IN</sub>	Shutdown input current (IN) with charge disabled	IN = 5V, Charge Disabled ( $\overline{CE}$ high), no capacitor	2	4		μA
		IN = 14V, Charge Disabled ( $\overline{CE}$ high), no capacitor	3.5	6		μA
I <sub>Q_IN</sub>	Quiescent input current (IN)	IN = 5V, OUT = 3.8V, Charge Enabled ( $\overline{CE}$ low), I <sub>CHG</sub> = 0A	0.45	0.6		mA
I <sub>Q_IN</sub>	Quiescent input current (IN)	IN = 14V, OUT = 7.6V, Charge Enabled ( $\overline{CE}$ low), I <sub>CHG</sub> = 0A	0.45	0.6		mA
<b>INPUT</b>						
V <sub>IN_OP</sub>	IN operating range		3.0		18	V
V <sub>IN_LOWV</sub>	IN voltage to start charging	IN rising	3.05	3.09	3.15	V
V <sub>IN_LOWV</sub>	IN voltage to stop charging	IN falling	2.80	2.95	3.10	V
V <sub>SLEEPZ</sub>	Exit sleep mode threshold	IN rising, V <sub>IN</sub> - V <sub>OUT</sub> , OUT = 4V	95	135	175	mV
V <sub>SLEEP</sub>	Sleep mode threshold hysteresis	IN falling, V <sub>IN</sub> - V <sub>OUT</sub> , OUT = 4V		80		mV
V <sub>IN_OV</sub>	VIN overvoltage rising threshold	IN rising	18.1	18.4	18.7	V
V <sub>IN_OVZ</sub>	VIN overvoltage falling threshold	IN falling		18.2		V
<b>CONFIGURATION PINS SHORT/OPEN PROTECTION</b>						
R <sub>ISET_SHORT</sub>	Highest resistor value considered short	R <sub>ISET</sub> below this at startup, charger does not initiate charge, power cycle or $\overline{CE}$ toggle to reset			350	Ω
<b>CHARGER</b>						
V <sub>FB_REF</sub>	Feedback reference voltage			0.8		V
V <sub>FB_REF_ACC</sub>	Feedback reference voltage accuracy	T <sub>J</sub> = -40°C to 125°C	-1		1	%
I <sub>CHG_RANGE</sub>	Typical charge current regulation range	V <sub>OUT</sub> > V <sub>BAT_LOWV</sub>	10		800	mA
K <sub>ISET</sub>	Charge current setting factor, I <sub>CHG</sub> = K <sub>ISET</sub> / R <sub>ISET</sub>	10mA < I <sub>CHG</sub> < 800mA	270	300	330	A Ω
I <sub>CHG_ACC</sub>	Charge current accuracy	R <sub>ISET</sub> = 375 Ω, OUT = 3.8V or 7.6V	720	800	880	mA
		R <sub>ISET</sub> = 600 Ω, OUT = 3.8V or 7.6V	450	500	550	mA
		R <sub>ISET</sub> = 3.0k Ω, OUT = 3.8V or 7.6V	90	100	110	mA
		R <sub>ISET</sub> = 30k Ω, OUT = 3.8V or 7.6V	9	10	11	mA
V <sub>CHG</sub>	Supercapacitor charged threshold	OUT rising, as percentage of FB regulation target		98		%
R <sub>ON</sub>	Charging path FET on-resistance	I <sub>OUT</sub> = 400mA, T <sub>J</sub> = 25°C		845	1000	m Ω
		I <sub>OUT</sub> = 400mA, T <sub>J</sub> = -40 - 125°C		845	1450	m Ω
<b>CHARGER PROTECTION</b>						
I <sub>OUT_OCP</sub>	Output current limit threshold	I <sub>OUT</sub> rising	0.9	1	1.1	A

## 6.5 Electrical Characteristics (continued)

$3.0V < V_{IN} < 18V$  and  $V_{IN} > V_{OUT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , and  $T_J = 25^{\circ}C$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TEMPERATURE REGULATION AND TEMPERATURE SHUTDOWN</b>						
$T_{REG}$	Typical junction temperature regulation			125		$^{\circ}C$
$T_{SHUT}$	Thermal shutdown rising threshold	Temperature increasing		150		$^{\circ}C$
	Thermal shutdown falling threshold	Temperature decreasing		135		$^{\circ}C$
<b>LOGIC INPUT PIN (<math>\overline{CE}</math>)</b>						
$V_{IH}$	Input high threshold level		1.3			V
$V_{IL}$	Input low threshold level				0.4	V
$R_{PD\_CE}$	$\overline{CE}$ pin internal pull-down resistor		3.3			$M\Omega$
<b>LOGIC OUTPUT PIN (STAT, <math>\overline{PG}</math>)</b>						
$V_{OL}$	Output low threshold level	Sink current = 5mA			0.4	V
$I_{OUT\_BIAS}$	High-level leakage current	Pull up rail 3.3V			1	$\mu A$

## 6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>CHARGER</b>					
$t_{OUT\_OCP\_DGL}$	Deglintch time for $I_{OUT\_OCP}$ , IOUT rising		100		$\mu s$

## 6.7 Typical Characteristics

$C_{IN} = 1 \mu F$ ,  $C_{OUT} = 1 \mu F$

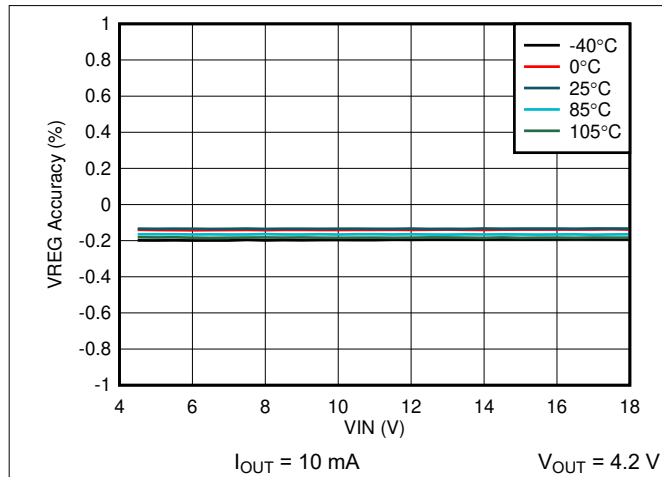


图 6-1. Line Regulation

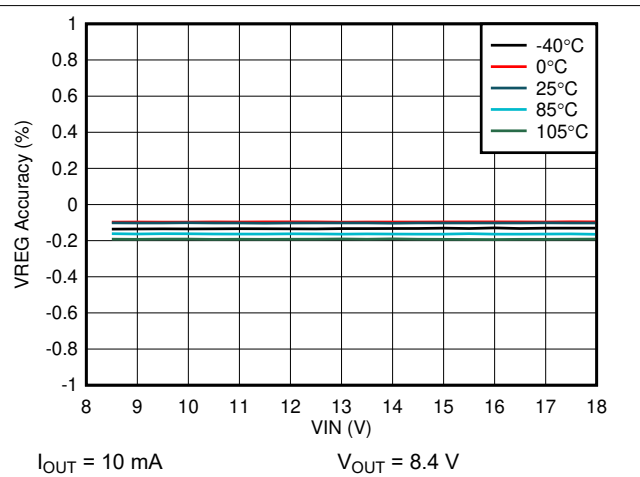


图 6-2. Line Regulation

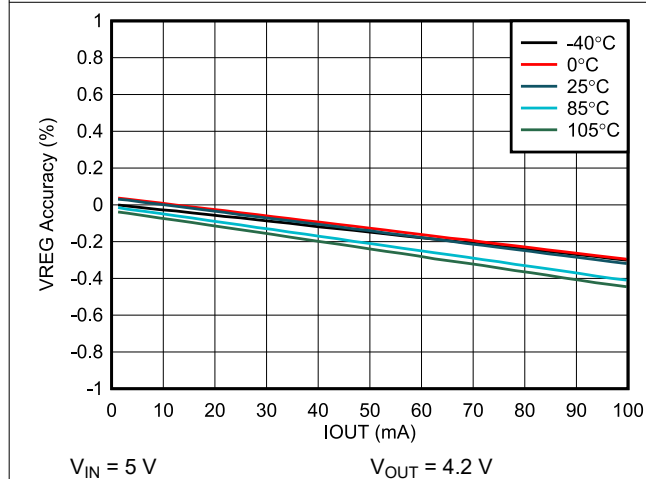


图 6-3. Load Regulation

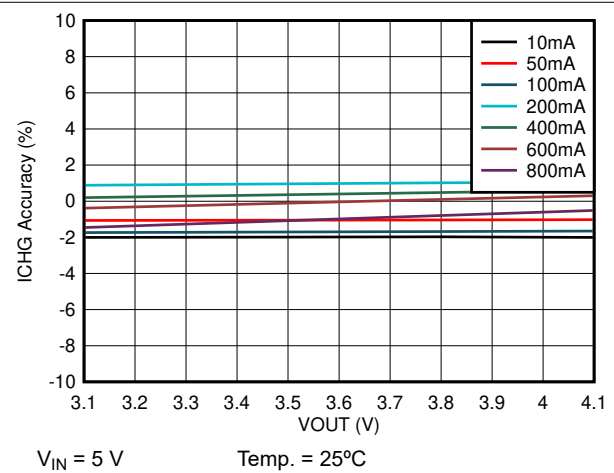


图 6-4. ICHG Accuracy vs. VOUT

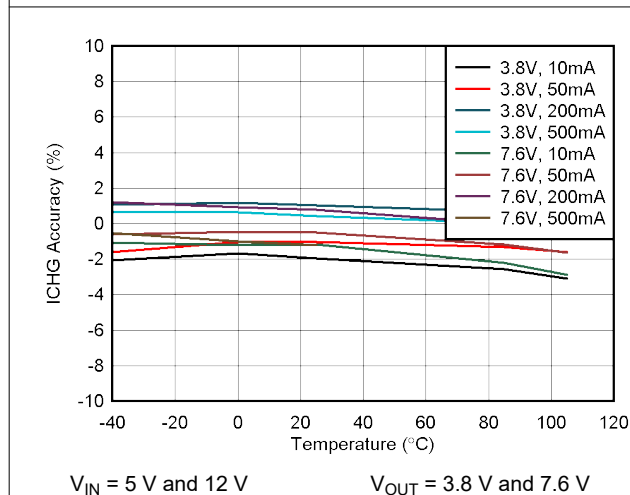


图 6-5. ICHG Accuracy vs. Temperature

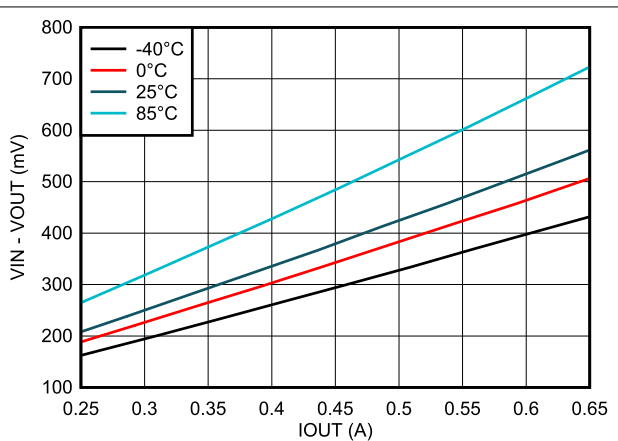
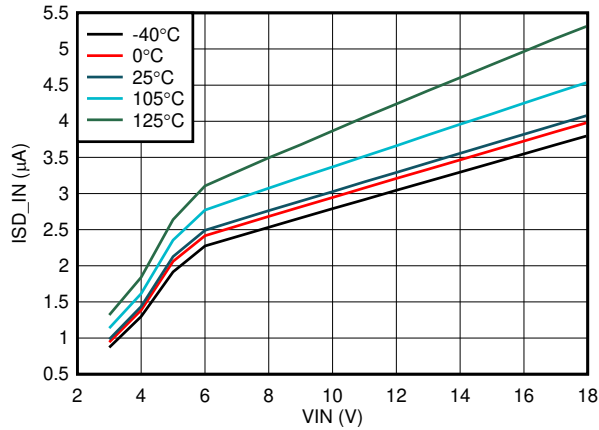


图 6-6. Dropout Voltage vs. Output Current



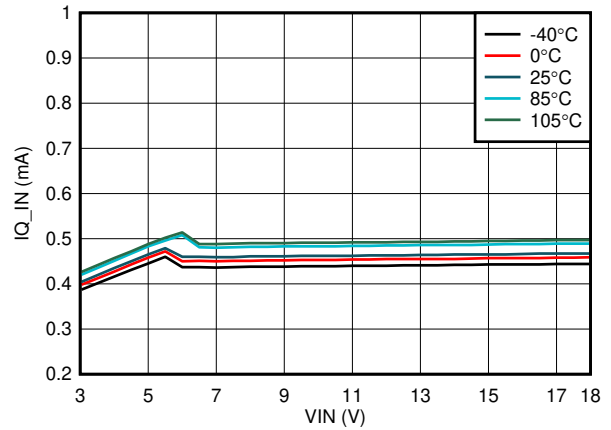
## 6.7 Typical Characteristics (continued)

$C_{IN} = 1 \mu F$ ,  $C_{OUT} = 1 \mu F$



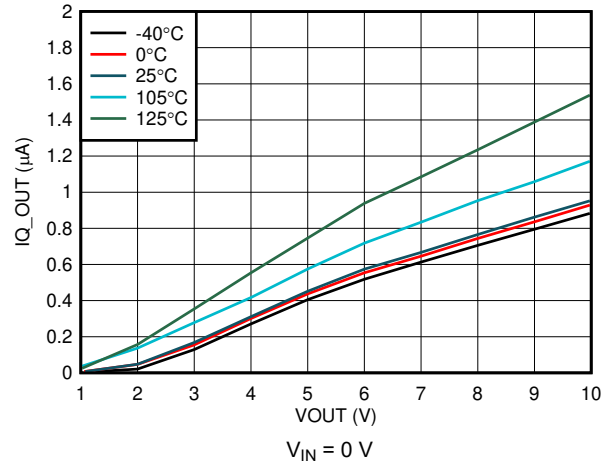
$\overline{CE}$  Pin = HIGH  $V_{OUT} = 0 V$

图 6-7. Input Shutdown Current vs. Input Voltage



$\overline{CE}$  Pin = LOW  $ICHG = 0 A$

图 6-8. Input Quiescent Current vs. Input Voltage



$V_{IN} = 0 V$

图 6-9. Output Quiescent Current vs. Output Voltage

## 7 Detailed Description

### 7.1 Overview

The device has a single power output that charges the supercapacitor. The system load can be placed in parallel with the supercapacitor; the charge current is shared between the system and supercapacitor.

The charger is designed for a single path from the input to the output to charge the supercapacitor. Upon application of a valid input power source, the ISET pin is checked for short/open circuit.

The device attempts to charge the supercapacitor at the fast-charge current setting from fully discharged (0 V) up to the programmable regulation voltage,  $V_{REG}$ . Power dissipation in the IC is greatest in fast charge with a lower supercapacitor voltage. If the IC temperature reaches  $T_{REG}$ , the IC enters thermal regulation and reduces the charge current as needed to keep the temperature from rising any further. The fast-charge current is programmed using the ISET pin. 图 7-1 shows the typical supercapacitor charging profile with thermal regulation. At lower fast-charge settings, the junction temperature of the IC is less than  $T_{REG}$  and thermal regulation is not entered.

Once the supercapacitor has charged to the regulation voltage, the voltage loop takes control and holds the voltage at the regulation voltage as the current tapers down to zero. There is no current termination threshold as seen in Li-ion chargers.

Further details are described in 节 7.3.

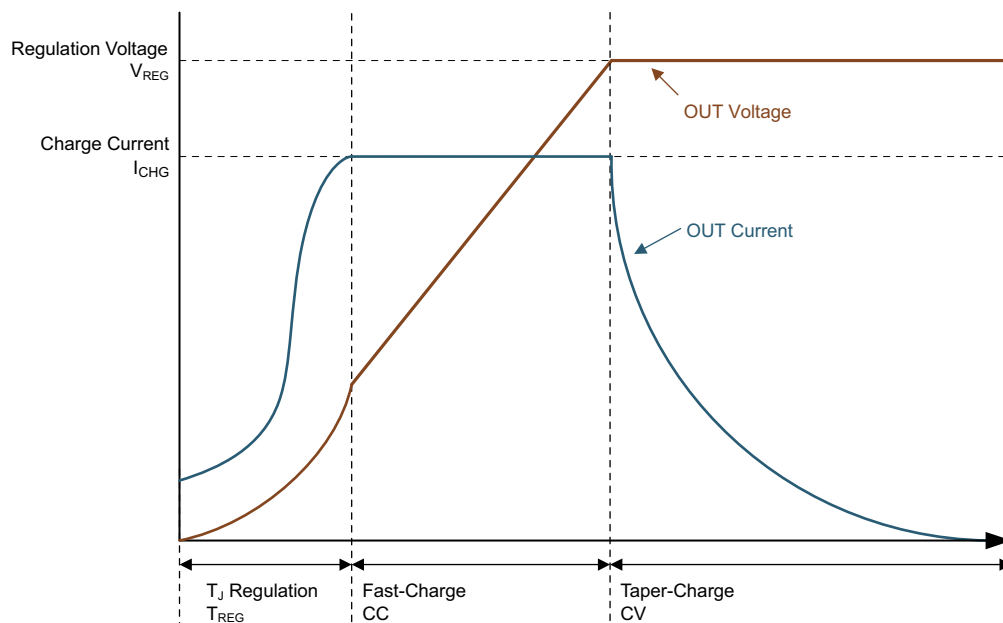
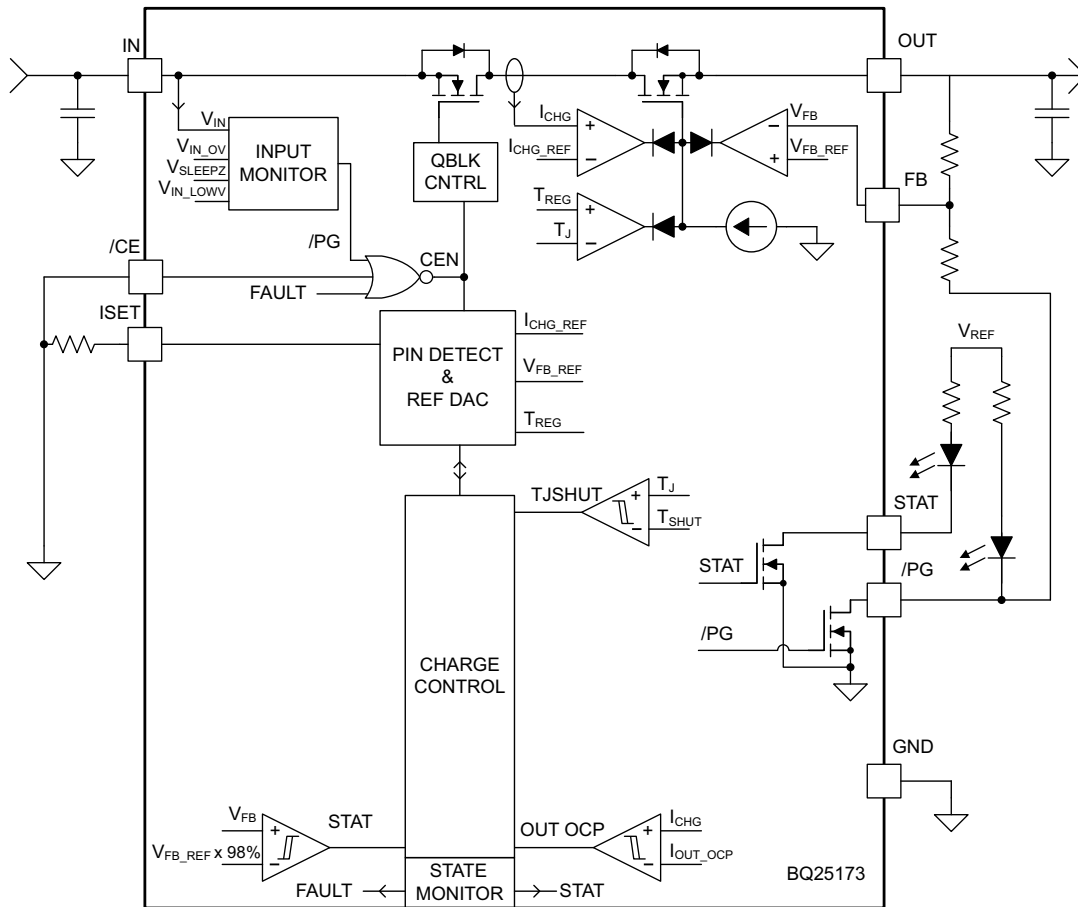


图 7-1. Supercapacitor Charging Profile with Thermal Regulation

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Device Power Up from Input Source

When an input source is plugged in and charge is enabled, the device checks the input source voltage to turn on all of the bias circuits. The device detects and sets the charge current limits before the linear regulator is started. The power-up sequence from the input source is listed below:

1. ISET pin detection
2. Charger power up

#### 7.3.1.1 ISET Pin Detection

After a valid VIN is plugged in and the  $\overline{CE}$  pin is pulled LOW, the device checks the resistor on the ISET pin for a short circuit ( $R_{ISET} < R_{ISET\_SHORT}$ ). If a short condition is detected, the charger remains in the FAULT state until the input or  $\overline{CE}$  pin is toggled. If the ISET pin is open circuit, the charger proceeds through pin detection and starts the charger with no charge current. This pin is monitored during charging and changes in  $R_{ISET}$  while the charger is operating immediately translates to changes in charge current.

An external pulldown resistor ( $\pm 1\%$  or better recommended to minimize charge current error) from the ISET pin to GND sets the charge current as:

$$I_{CHG} = \frac{K_{ISET}}{R_{ISET}} \quad (1)$$

where:

- $I_{CHG}$  is the desired fast-charge current
- $K_{ISET}$  is the gain factor found in the electrical specifications
- $R_{ISET}$  is the pulldown resistor from the ISET pin to GND

For charge currents below 50 mA, an extra RC circuit is recommended on the ISET pin to achieve a more stable current signal. For greater accuracy at lower currents, part of the current-sensing FET is disabled to give better resolution.

### 7.3.2 Supercapacitor Regulation Voltage

The device allows for the supercapacitor regulation voltage,  $V_{REG}$ , to be programmed with a resistor divider between the OUT and FB pins:

$$V_{REG} = V_{FB\_REF} \times \frac{R_{FBT} + R_{FBB}}{R_{FBB}} \quad (2)$$

Where  $V_{FB\_REF}$  is listed in the electrical characteristics table. The resistors can be seen in [图 7-2](#). The total resistance ( $R_{FBT} + R_{FBB}$ ) should not exceed 1 M $\Omega$ .

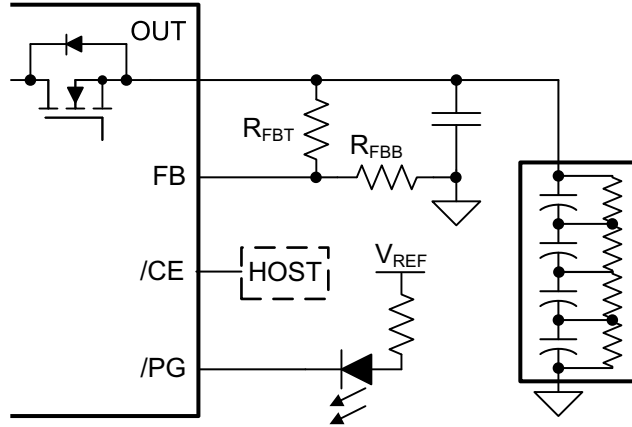


图 7-2. BQ25173 Feedback Divider

### 7.3.3 Supercapacitor Charging Profile

The device charges a supercapacitor in two phases: constant current and constant voltage. Power dissipation in the IC is greatest in fast charge with a lower supercapacitor voltage. If the IC temperature reaches  $T_{REG}$ , the IC enters thermal regulation and reduces the charge current as needed to keep the temperature from rising any further. As the supercapacitor approaches the regulation voltage, the current tapers down to 0 mA. There is no current termination threshold as seen in Li-Ion chargers.

### 7.3.4 Status Outputs ( $\overline{PG}$ , STAT)

#### 7.3.4.1 Power Good Indicator ( $\overline{PG}$ Pin)

This open-drain pin pulls LOW to indicate a good input source when:

1.  $V_{IN}$  above  $V_{IN\_LOWV}$
2.  $V_{IN}$  above  $V_{OUT} + V_{SLEEPZ}$  (not in SLEEP)
3.  $V_{IN}$  below  $V_{IN\_OV}$

The  $\overline{PG}$  pin can be used as the GND connection for the bottom resistor in the feedback divider to prevent divider leakage current from the supercapacitor when the charger is disabled. This is only recommended when  $V_{REG} \leq 5$  V (1-2s supercapacitors) as the absolute maximum rating on  $\overline{PG}$  is 5.5 V. An example circuit can be seen in 图 8-1.

#### 7.3.4.2 Charging Status Indicator (STAT)

The device indicates the charging state on the open-drain STAT pin. This pin can drive an LED.

表 7-1. STAT Pin State

CHARGING STATE	STAT PIN STATE
$V_{FB} < 98\%$ of $V_{FB\_REF}$	High
$V_{FB} > 98\%$ of $V_{FB\_REF}$	Low
Fault ( $V_{IN}$ OVP, OUT OCP, or ISET pin short)	Blink at 1 Hz

### 7.3.5 Protection Features

The device closely monitors input and output voltage, as well as internal FET current and temperature for safe linear regulator operation.

#### 7.3.5.1 Input Overvoltage Protection ( $V_{IN}$ OVP)

If the voltage at the IN pin exceeds  $V_{IN\_OV}$ , the device enters STANDBY mode. Once the IN voltage recovers to normal level, charging resumes.

### 7.3.5.2 Output Overcurrent Protection (OUT OCP)

During normal operation, the OUT current should be regulated to the ISET programmed value. However, if a short circuit occurs on the ISET pin, the OUT current may rise to an unintended level. If current at the OUT pin exceeds  $I_{OUT\_OCP}$ , the device turns off after a deglitch,  $t_{OUT\_OCP\_DGL}$ , and the device remains latched off. An input supply or  $\overline{CE}$  pin toggle is required to restart operation.

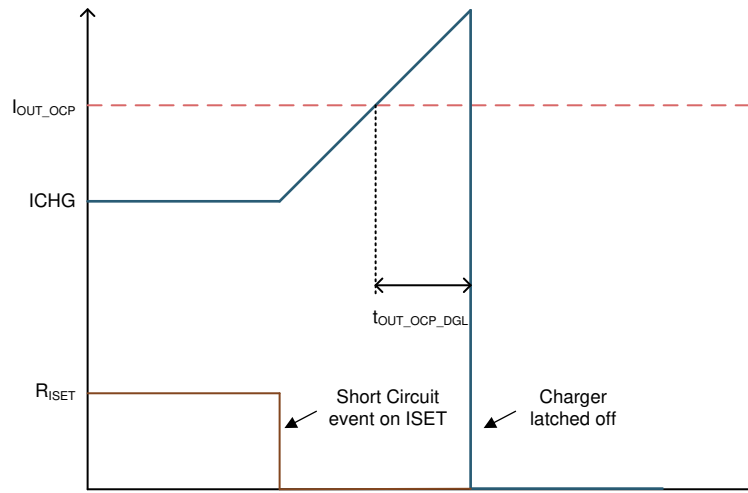


图 7-3. Overcurrent Protection

### 7.3.5.3 Thermal Regulation and Thermal Shutdown ( $T_{REG}$ and $T_{SHUT}$ )

The device monitors its internal junction temperature ( $T_J$ ) to avoid overheating and to limit the IC surface temperature. When the internal junction temperature exceeds the thermal regulation limit, the device automatically reduces the charge current to maintain the junction temperature at the thermal regulation limit ( $T_{REG}$ ). During thermal regulation, the actual charging current is usually below the programmed value on the ISET pin.

Additionally, device thermal shutdown turns off the linear regulator when the IC junction temperature exceeds the  $T_{SHUT}$  threshold. The charger resumes operation when the IC die temperature decreases below the  $T_{SHUT}$  falling threshold.

## 7.4 Device Functional Modes

### 7.4.1 Shutdown or Undervoltage Lockout (UVLO)

The device is in the shutdown state if the IN pin voltage is less than  $V_{IN\_LOWV}$ . The internal circuitry is powered down, all the pins are high impedance, and the device draws from the input supply. Once the IN voltage rises above the  $V_{IN\_LOW}$  threshold, the IC will enter Sleep Mode or Active Mode depending on the OUT pin voltage.

### 7.4.2 Sleep Mode

The device is in Sleep Mode when  $V_{IN\_LOWV} < V_{IN} < V_{OUT} + V_{SLEEPZ}$ . The device waits for the input voltage to rise above  $V_{OUT} + V_{SLEEPZ}$  to start operation.

### 7.4.3 Active Mode

The device is powered up and charges the supercapacitor when the  $\overline{CE}$  pin is LOW and the IN voltage ramps above both  $V_{IN\_LOWV}$ , and  $V_{OUT} + V_{SLEEPZ}$ . The device draws  $I_{Q\_IN}$  from the supply to bias the internal circuitry. For details on the device power-up sequence, refer to 节 7.3.1.

#### **7.4.3.1 Standby Mode**

The device is in Standby Mode if a valid input supply is present and a recoverable fault is detected. The internal circuitry is partially biased, and the device continues to monitor for the recoverable fault to be removed.

#### **7.4.4 Fault Mode**

The fault conditions are categorized into recoverable and nonrecoverable as follows:

- Recoverable, from which the device should automatically recover once the fault condition is removed:
  - VIN OVP
- Nonrecoverable, requiring pin or input supply toggle to resume operation:
  - OUT OCP
  - ISET pin short detected

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

A typical application consists of the device configured as a standalone charger for a 1- to 4-cell supercapacitor. The regulation voltage,  $V_{REG}$ , is configured using a resistor divider between the OUT and FB pins. The charge current is configured using a pulldown resistor on the ISET pin. Pulling the  $\overline{CE}$  pin above  $V_{IH}$  disables the charging function. Charger and input supply status are reported with the STAT and PG pins.

### 8.2 Typical Applications

#### 8.2.1 1s Supercapacitor Charger Design Example

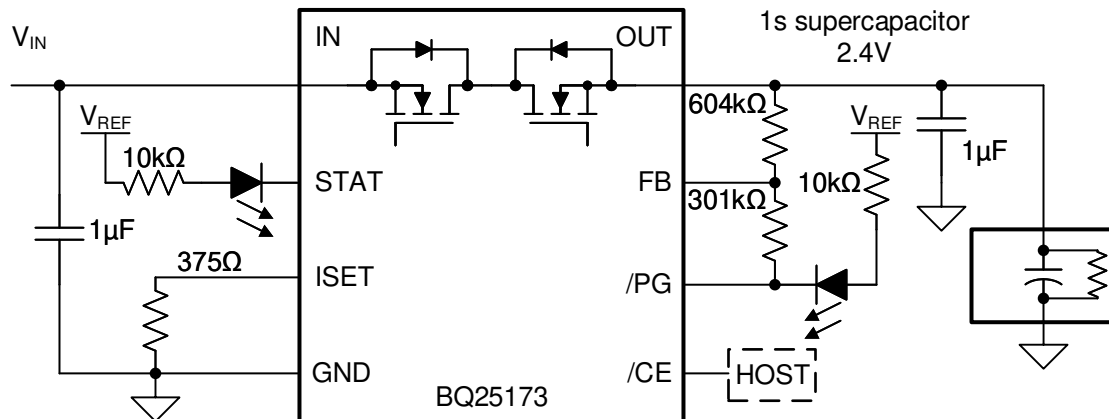


图 8-1. BQ25173 1s Supercapacitor Application Diagram

#### 8.2.1.1 Design Requirements

- Supply voltage is 5 V to 18 V
- Fast charge current:  $I_{CHG} = 800$  mA
- Regulation voltage:  $V_{REG} = 2.4$  V
- $\overline{CE}$  is an open-drain control pin
- PG pin is used as the GND connection in the feedback divider to minimize supercapacitor current leakage

#### 8.2.1.2 Detailed Design Procedure

- With  $R_{FBT} = 604$  k $\Omega$ , calculate  $R_{FBB}$  so  $V_{REG} = 2.4$  V using [方程式 2](#)
- $R_{ISET} = [K_{ISET} / I_{CHG}]$  from electrical characteristics table.
  - $K_{ISET} = 300$  A $\Omega$
  - $R_{ISET} = [300 \text{ A}\Omega / 0.8 \text{ A}] = 375 \Omega$



### 8.2.1.3 Application Curves

$C_{IN} = 1 \mu F$ ,  $C_{OUT} = 1 \mu F$ ,  $C_{SC} = 25 F$ ,  $V_{IN} = 5 V$  (unless otherwise specified)

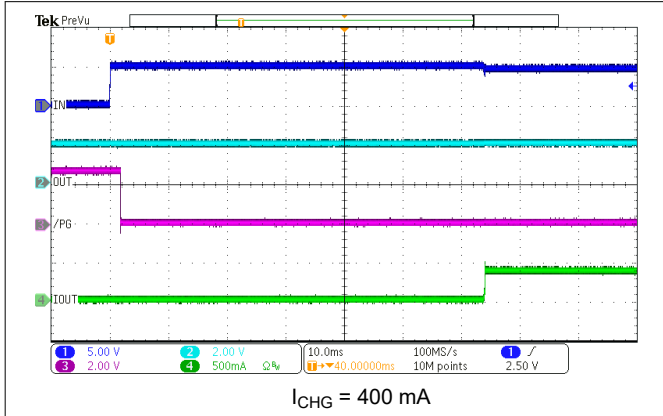


图 8-2. Power Up with Supercapacitor

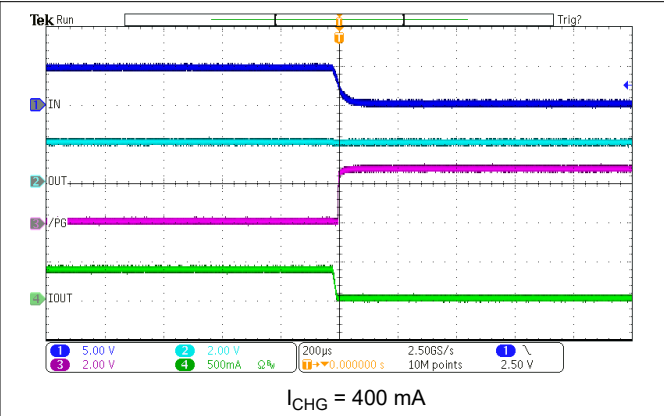


图 8-3. Power Down with Supercapacitor

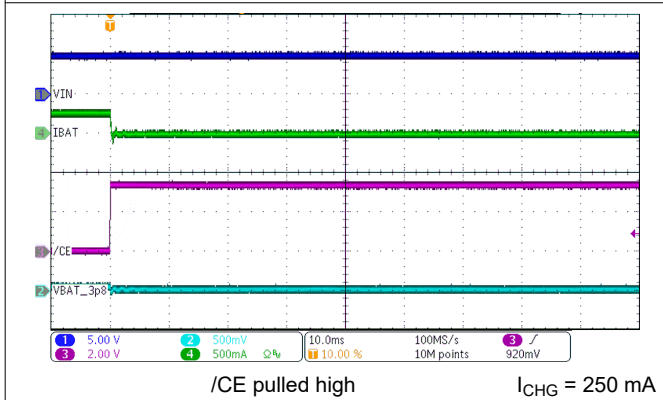


图 8-4. Charge Disable

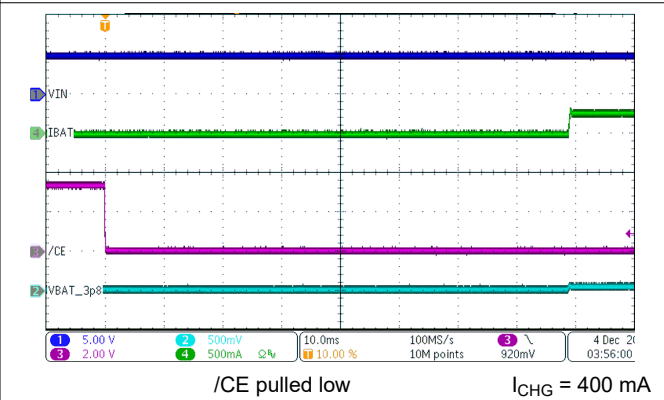


图 8-5. Charge Enable

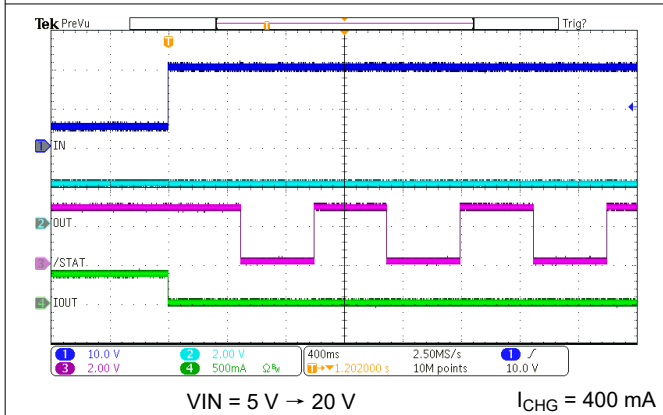


图 8-6. IN OVP Response

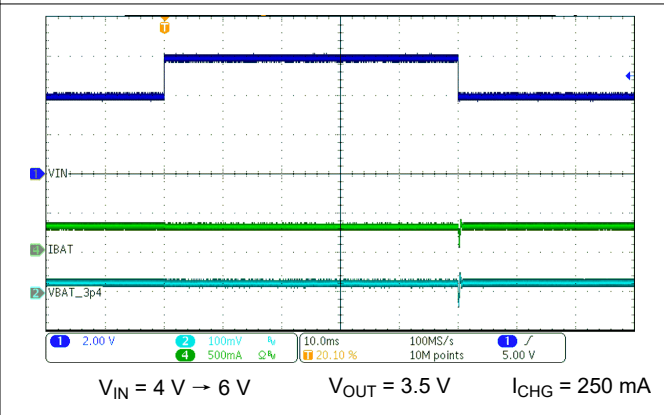
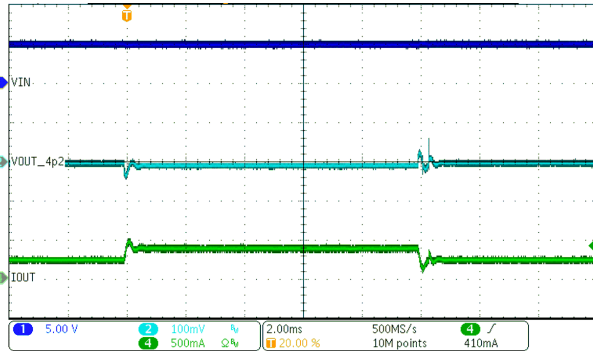
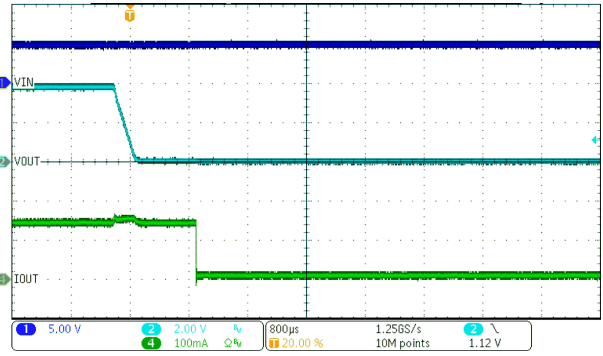


图 8-7. IN Transient Response



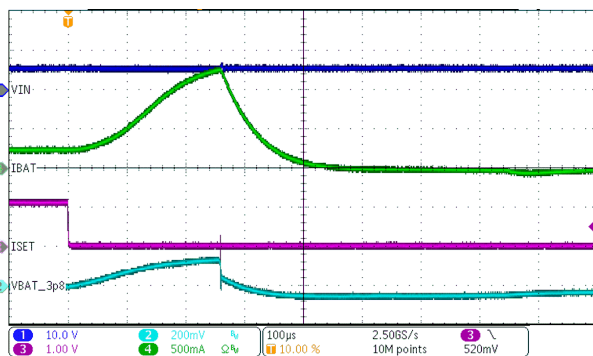
$V_{OUT} = 4.2\text{ V}$   $I_{SYS} = 0\text{ mA} \rightarrow 500\text{ mA}$   $I_{CHG} = 250\text{ mA}$   
 $\text{mA} \rightarrow 0\text{ mA}$

图 8-8. OUT Transient Response



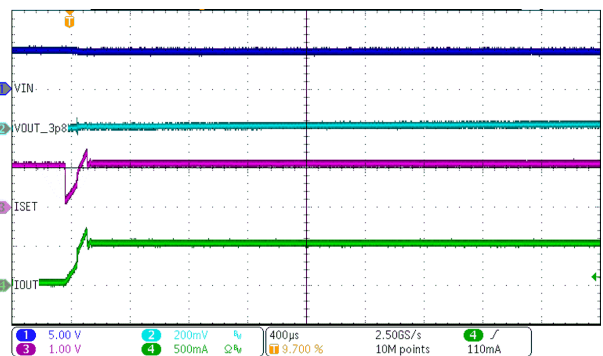
$V_{OUT} = 4.0\text{ V} \rightarrow 0\text{ V}$   $I_{CHG} = 250\text{ mA}$

图 8-9. OUT Short-Circuit Response



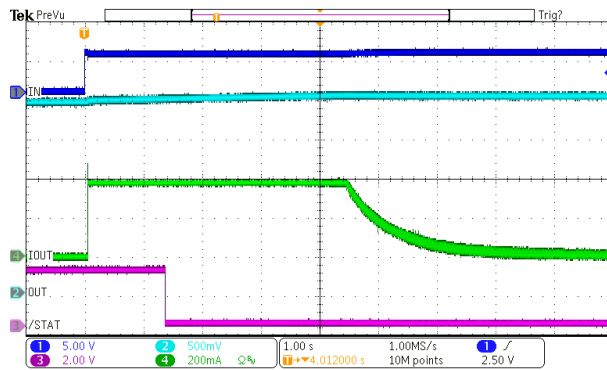
$I_{SET} = 1.2\text{ k}\Omega \rightarrow 0\ \Omega$

图 8-10. ISET Short-Circuit Response



$I_{SET} = 50\text{ mA} \rightarrow 500\text{ mA}$

图 8-11. ISET Change Response



$V_{REG} = 2.5\text{ V}$

$I_{CHG} = 400\text{ mA}$

图 8-12. Charge Complete

## 8.2.2 4s Supercapacitor Charger Design Example

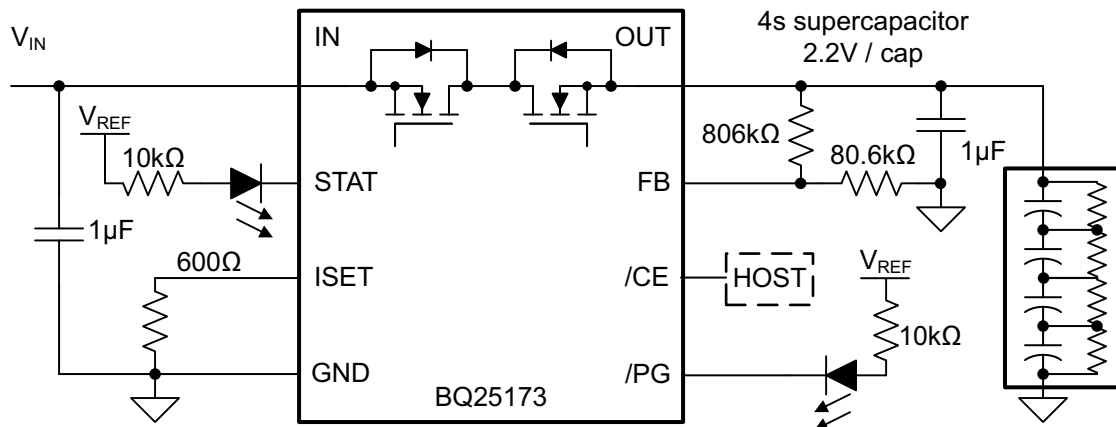


图 8-13. BQ25173 4s Supercapacitor Application Diagram

### 8.2.2.1 Design Requirements

The design requirements include the following:

- Supply voltage is 9 V to 18 V
- Fast charge current:  $I_{CHG} = 500 \text{ mA}$
- Regulation voltage:  $V_{REG} = 8.8 \text{ V}$
- $\overline{CE}$  is a control pin, pull high to disable the charger

### 8.2.2.2 Application Curves

For application curves, refer to [节 8.2.1.3](#).

## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3.0 V and 18 V (up to 40 V tolerant) and current capability of at least the maximum designed charge current. If located more than a few inches from the IN and GND pins, a larger capacitor is recommended.

## 10 Layout

### 10.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND and the output filter capacitor from OUT to GND should be placed as close as possible to the device, with short trace runs to both IN, OUT, and GND.

- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the supercapacitor. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high-current charge paths into the IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.

### 10.2 Layout Example

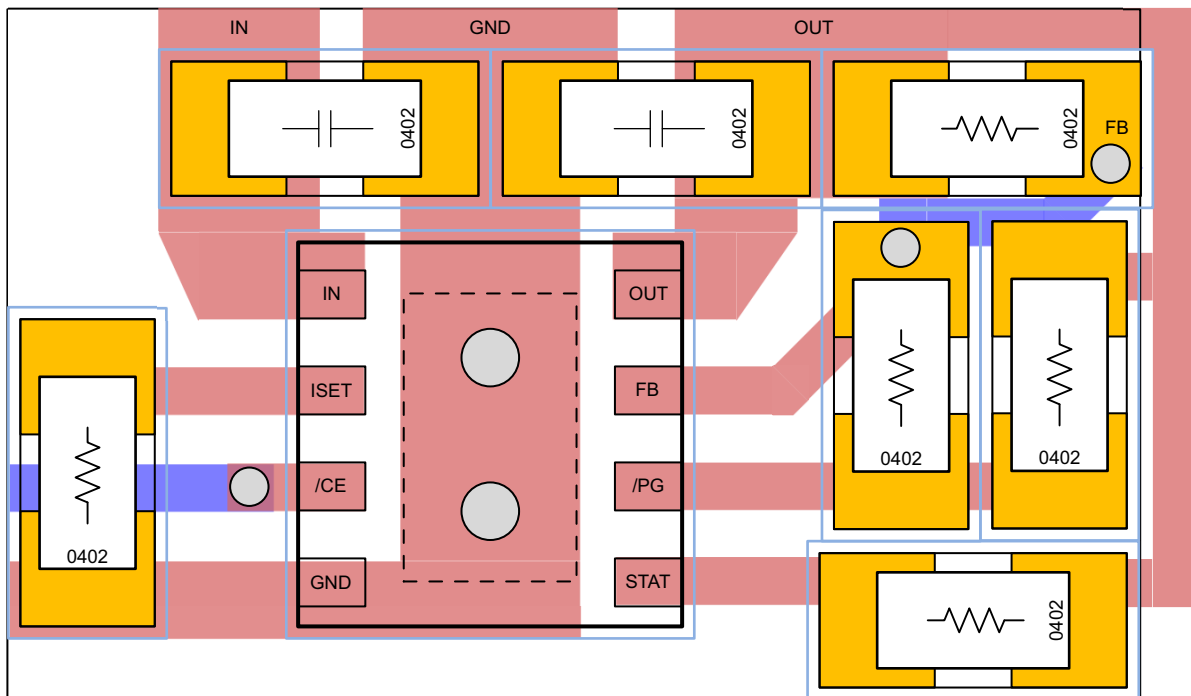


图 10-1. BQ25173 Board Layout Example

### 10.3 Thermal Package

The most common measure of package thermal performance is thermal impedance ( $\theta_{JA}$ ) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for  $\theta_{JA}$  is:

$$\theta_{JA} = (T_J - T) / P \quad (3)$$

Where:

$T_J$  = chip junction temperature

$T$  = ambient temperature

$P$  = device power dissipation

Factors that can influence the measurement and calculation of  $\theta_{JA}$  include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of supercapacitors, maximum power dissipation is typically seen at the beginning of the charge cycle when the voltage is at its lowest.

Device power dissipation,  $P$ , is a function of the charge rate and the voltage drop across the internal PowerFET.  $P$  can be calculated from the following equation during charging:

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} \quad (4)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for nontypical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 第三方产品免责声明

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#### 11.3 支持资源

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#### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 11.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25173DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	B173	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## GENERIC PACKAGE VIEW

**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

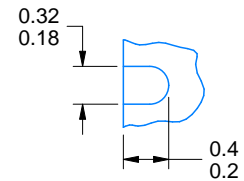
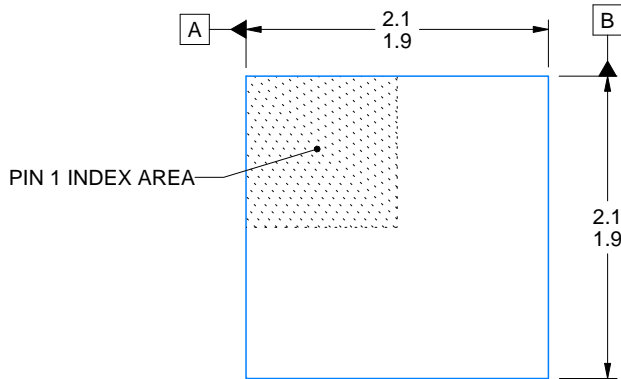
# DSG0008A



# PACKAGE OUTLINE

## WSON - 0.8 mm max height

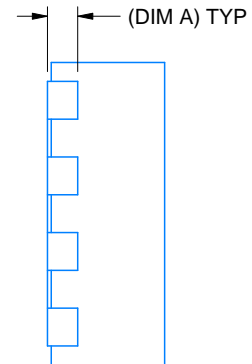
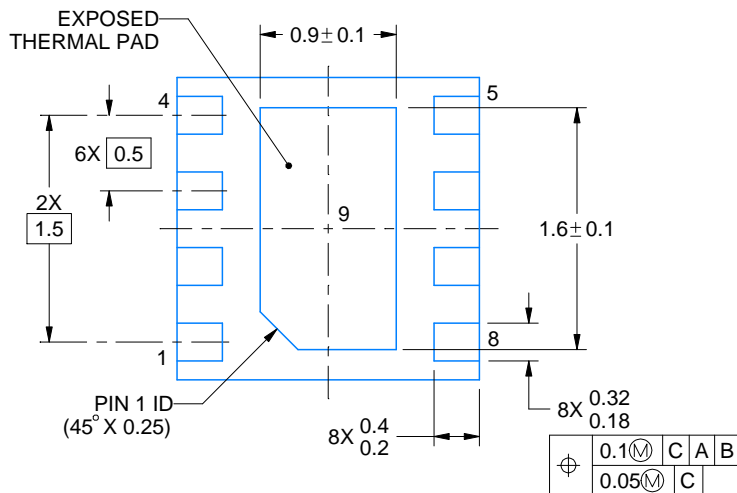
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

### NOTES:

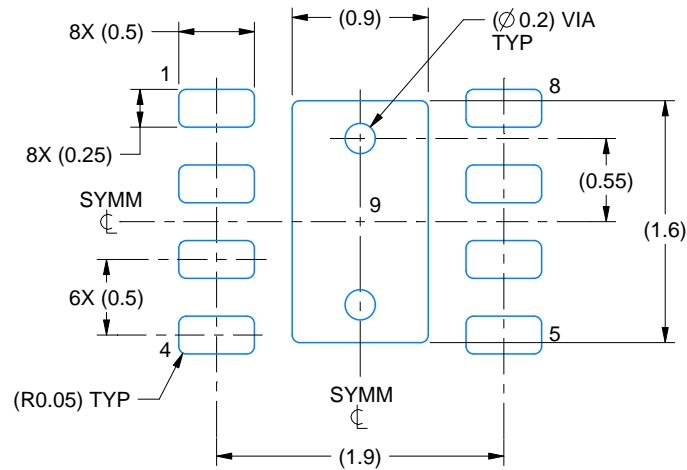
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

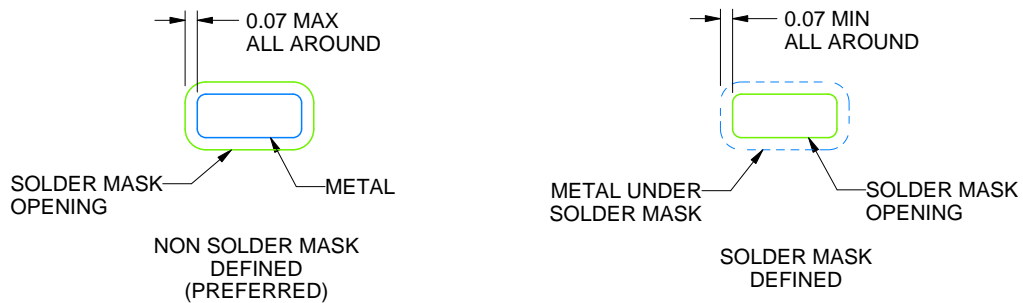
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

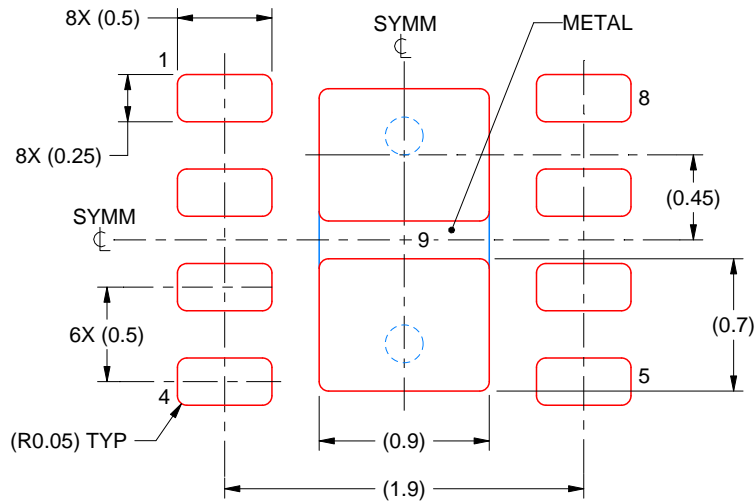
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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