Voltage Protection for 3-Series to 6-Series Cell Lithium-Ion/Polymer Batteries

Check for Samples: bq77PL157A4225

FEATURES

- **Single IC Li-Ion Protection for 3-Series to 6-Series Cells**
- **Stackable to Protect up to 18-Series Cells**
- **Programmable Detection Time Delay**
- **Low Power Consumption**
  - **Typical 2-µA to 2.5-µA Normal Mode**
- **Fixed 4.225 V Overvoltage Threshold**
- **Highly Accurate: ±20-mV MAX, T_A = 0°C to 50°C**
- **Output Activation for Low Side FET (Contact TI for Alternate Output Options: High/Low-side Fuse or FET)**
- **Protected Output, Power, and Ground Pins for Added Safety and Reliability**
- **Permanent or Recoverable Fault Options**
- **16-pin Small Outline Package**

APPLICATIONS

- **Primary or Secondary Level Voltage Protection for Li-Ion Battery Packs for Use in:**
  - **Power Tools**
  - **UPS Systems**
  - **E-Bikes, Scooters, and Small Mobility Vehicles**
  - **Medical Devices, Test Equipment, and Industrial Products**

DESCRIPTION

The bq77PL157 is a stackable overvoltage protection device for 3, 4, 5 or 6 series cell Li-Ion battery packs. This device incorporates a precise and accurate overvoltage detection circuit with preconfigured threshold limits. Additional features include the ability to stack multiple parts to monitor up to 18 series cells.

FUNCTION

Each series cell in a Li-Ion battery pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq77PL157 starts charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes state and the LVO pin becomes active.

If multiple bq77PL157 devices are stacked, the LVIN pin of the next-lower device receives the LVO pin from the above device and similarly starts a shortened delay timer before activating its OUT pin. (No additional isolation or level-shift circuitry is required.) The lowest bq77PL157 in the string is used to activate a power MOSFET located in the low side of the power path.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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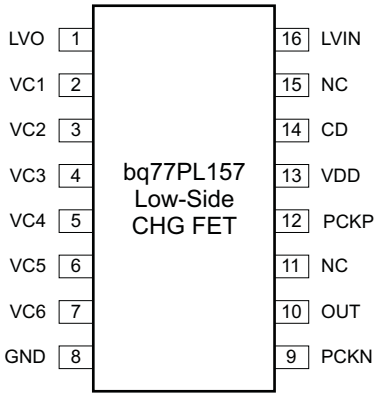
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

$V_{PROTECT}$	DEVICE	FEATURE CONFIGURATION	PACKAGING	FULL PART NAME
4.225 V	bq77PL157A	Recoverable Output	Tape and Reel	bq77PL157APWR-4225
			Tube	bq77PL157APW-4225

DEVICE INFORMATION

PW PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
CD	14	External capacitor to GND to set delay time
GND	8	Ground pin and negative end of cell stack
LVIN	16	Level-shift input (used for stacking, input is from next-higher part)
LVO	1	Level-shift output (used for stacking, route this output to next-lower part)
NC	11, 15	No connection
OUT	10	Output gate drive to external MOSFET
PCKN	9	Pack negative supply for OUT driver (connect to source of external MOSFET or GND if device not at bottom of stack)
PCKP	12	Pack positive supply for OUT driver (connect to most positive cell input of device)
VC1	2	Sense voltage input for most positive cell
VC2	3	Sense voltage input for second most positive cell
VC3	4	Sense voltage input for third most positive cell
VC4	5	Sense voltage input for fourth most positive cell
VC5	6	Sense voltage input for fifth most positive cell
VC6	7	Sense voltage input for least positive cell
VDD	13	Power supply (via RC filter)

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FUNCTIONAL BLOCK DIAGRAMS

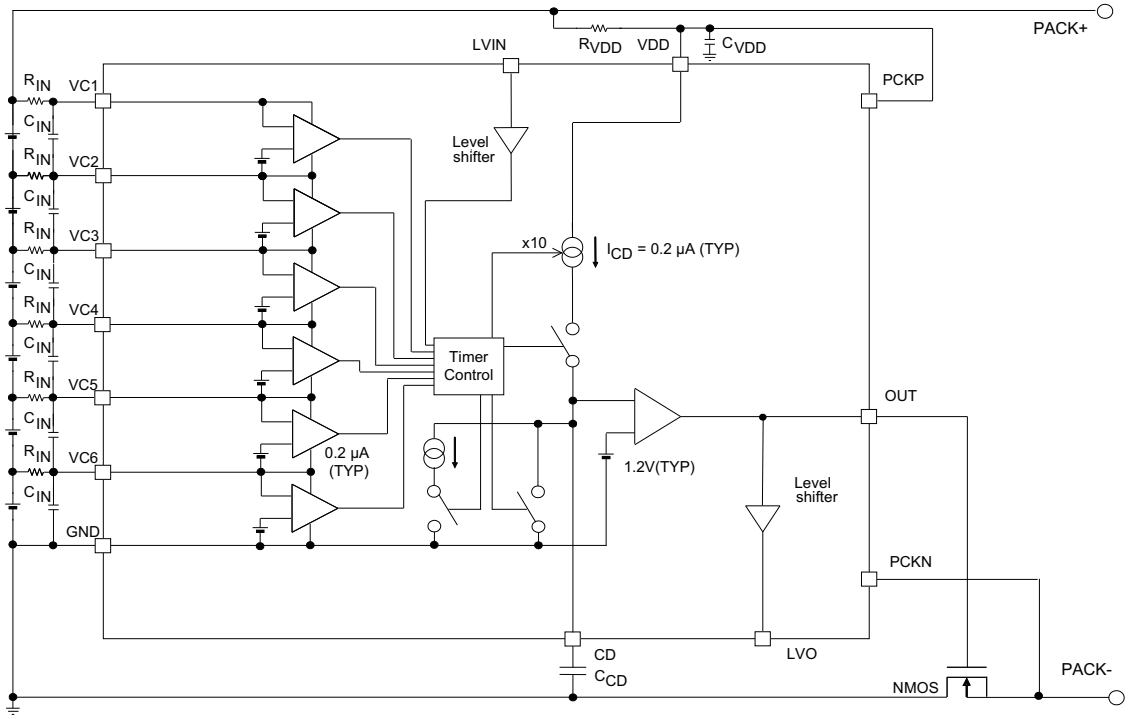

Figure 1. bq77PL157 – Low-Side Power NMOS Direct-Drive Output

ABSOLUTE MAXIMUM RATINGS

over recommended operating free-air temperature range, (unless otherwise noted)(1)

		RANGE
Supply voltage range, V_{MAX}	VDD, PCKP	–0.3 to 35 V
	PCKN	(VDD – 50) to VSS + 35 V
Input voltage range, V_{IN}	VCn (n=1 to 6)	–0.3 to 35 V
	VCn – VC(n+1), (n=1 to 5), VC6–GND	–0.3 to 8 V
	LVIN	–0.3 to 35 V
Output voltage range, V_{OUT}	OUT	–0.3 to 35 V
	CD	–0.3 to 35 V
	LVO	–0.3 to 35 V
Storage temperature range, T_{stg}		–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VDD	4.2		30	V
Pack positive voltage	PCKP	0		30	V
Pack negative voltage	PCKN	VDD – 30		30	V
Input voltage range	VCn (n = 1 to 6)	0		VDD	V
	VCn – VC(n + 1), (n = 1 to 5) VC6–GND	0		5	
Delay time capacitor	C_{CD}		0.22		µF
Voltage monitor filter resistance	R_{IN}			1	kΩ
Voltage monitor filter capacitance	C_{IN}	0.01		0.1	µF
Supply voltage filter resistance	R_{VDD}	0		1	kΩ
Supply voltage filter capacitance	C_{VDD}		0.1		µF
Operating ambient temperature range, T_A		–40		110	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted), typical values stated where T_A = 25°C

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{OA}	Overvoltage detection accuracy	T_A = 0°C to 50°C			±5	±25	mV
		T_A = –20°C to 85°C			±5	±40	
		T_A = –40°C to 110°C			±5	±70	
$V_{PROTECT}$	Overvoltage detection voltage				4.225		V
V_{TH}	Overvoltage detection hysteresis			150		450	mV
I_{IN} (1)	Input current on VCn (n = 2 to 6),	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ – 25 mV				±0.2	µA
	Input current on VC1 (2)	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ – 3.5 V			1	1.5	µA
t_D	Overvoltage detection delay time	VCn – VC(n+1), (n=1 to 5), VC6 – GND = $V_{PROTECT}$ + 25 mV, VDD = VC1 CD = 0.22 µF		1	1.5	2	s
t_{OA}	Minimum output active (fault) time	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ – V_{TH}, VDD = VC1, CD = 0.22 µF		0.7	1.5	2.3	s
$V_{CD,TH1}$	CD threshold voltage for output transition from inactive (no fault) to active (fault)				1.2		V
$V_{CD,TH2}$	CD clamp voltage after output change to active (fault)				2.4		V
I_{CH1}	CD charge current by overvoltage CD voltage = GND to $V_{CD,TH1}$	VCn – VC(n+1), (n=1 to 5), VC6-GND = $V_{PROTECT}$ + 25 mV VDD = VC1	Before output active CD = GND	–0.1	–0.2	–0.3	µA
I_{CH2}	CD clamp current after output active CD voltage = $V_{CD,TH1}$ to $V_{CD,TH2}$		After output active CD = $V_{CD,TH1}$	1	2	3	µA
I_{DS1}	CD discharge current CD voltage = $V_{CD,TH2}$ to $V_{CD,TH1}$	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ – V_{TH}, VDD = VC1	After OUT active and CD reaches $V_{CD,TH2}$ CD = $V_{CD,TH2}$	0.1	0.2	0.3	µA
I_{DS2}	CD clamp current CD voltage = $V_{CD,TH1}$ to GND		After OUT inactive, CD = $V_{CD,\ TH1}$		90		µA
I_{DD}	VDD Supply current	All cell voltages at 3.5 V/cell			2	3.5	µA
I_{PCKP}	Output supply current	PCKP = 22 V			0.4	0.8	µA

(1) Input current of each VCx does not include I_{DD} current of VDD.
(2) Input current from top cell does not contribute to cell imbalance.

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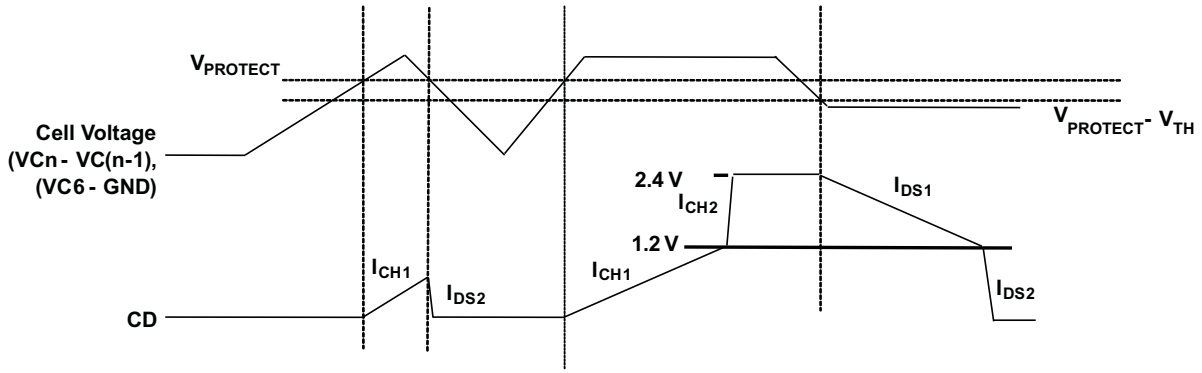

Figure 2. CD charge Current and Discharge Current

bq77PL157 OUTPUT

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OUT} OUT pin drive voltage	VCn – VC(n + 1), (n =1 to 5), VC6 – GND = $V_{PROTECT}$ + 25 mV, VDD = VC1, I_{OUT} = 0 to –0.1 mA, T_A = –40°C to 110°C			PCKN + 0.2	V
	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ – 25 mV, VDD = VC1, I_{OUT} = 0 to 0.1 mA, T_A = –40°C to 110°C	PCKN + 9	PCKN + 14	PCKN + 16	
V_{OUT} rise time	C_L = 5000 pF, V_{OUT}: 10% to 90%			100	µs
V_{OUT} fall time	C_L = 5000 pF, V_{OUT}: 90% to 10%			100	µs

LEVEL SHIFT FUNCTION

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
I_{LVL}	LVIN pull down current	VCn – VC(n + 1), (n = 1 to 5), VC6 –GND = $V_{PROTECT}$ – 25 mV, VDD = VC1, LVIN = VDD + 4 V		2	3.8	7	µA
V_{LVL}	LVIN threshold voltage			VDD + 1		VDD + 3.5	V
V_{OH}	LVO output high voltage	I_{OH} = –7 µA		GND + 4		GND + 6	V
t_{DA}	Output-active time-delay time	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ –25 mV, LVIN = VDD + 4 V	C_{CD} = 0.22 µF		132		ms
I_{CHLV}	CD charge current by LVIN input		CD = GND	9 × I_{CH2}	10 × I_{CH2}	11 × I_{CH2}	µA
t_{DIA}	Output-inactive delay time	VCn – VC(n + 1), (n = 1 to 5), VC6 – GND = $V_{PROTECT}$ –25 mV, LVIN = VDD	C_{CD} = 0.22 µF		3.5		ms
I_{DSLV}	CD charge current by LVIN input		CD = GND	I_{DS2}	I_{DS2}	I_{DS2}	µA

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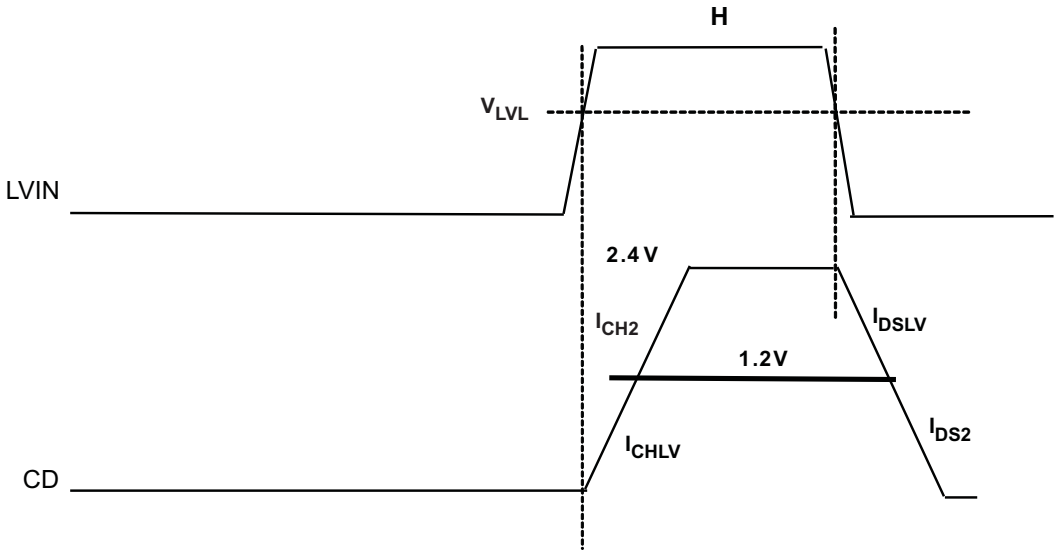

Figure 3. CD Charge Current and Discharge Current

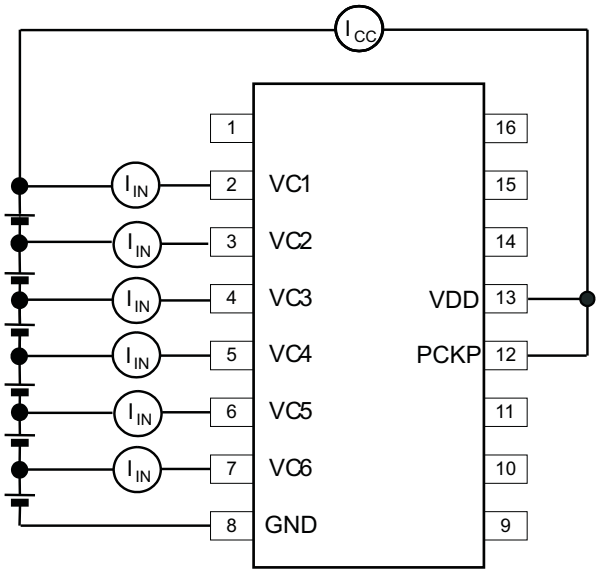

Figure 4. I_{CC}, I_{IN} Measurement Test Setup

OPERATION AND TIMING OF PROTECTION OUTPUT

From Direct Cell Inputs

When any one of the cell voltages exceeds $V_{PROTECT}$, an internal current source begins to charge capacitor C_{CD} connected to the CD pin, which acts as a delay timer. If all cell voltages fall below $V_{PROTECT}$ before V_{CD} reaches $V_{CD,TH1}$, the delay timer is reset and the OUT pin is not activated (i.e., no fault detected, output remains unchanged). An internal switch clamps the CD pin to GND, discharges the capacitor C_{CD}, and resets the full delay time for the next occurring overvoltage event.

If any cell voltage exceeds $V_{PROTECT}$ long enough for the voltage at the CD pin (V_{CD}) to reach $V_{CD,TH1}$ (1.2 V typical), then the OUT and LVO pins are activated (i.e., fault detected, output changes state), thus interrupting the circuit via the FET protection device. Once the output is activated, the CD pin is charged up to its maximum value $V_{CD,TH2}$ (2.4 V typical).

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When the recovery option is selected, if all cell voltages fall below $V_{PROTECT} - V_{TH}$ (threshold hysteresis), an internal current source begins to discharge capacitor C_{CD}, also acting as a delay timer. If any cell voltage returns back above $V_{PROTECT} - V_{TH}$ before V_{CD} reaches $V_{CD,TH1}$, the delay timer is reset and the OUT and LVO pins remains active (i.e. in the fault state). The CD pin is charged back to its maximum value $V_{CD,TH2}$.

If all cell voltages remain below $V_{PROTECT} - V_{TH}$ long enough for the voltage at the CD pin to reach $V_{CD,TH1}$, then the OUT and LVO pins are deactivated (i.e. output returns to the no fault state). An internal switch clamps the CD pin to GND, discharges the capacitor C_{CD}, and resets the full delay time for the next occurring overvoltage event.

The delay time for detecting an overvoltage fault is the time between charging C_{CD} from 0 to $V_{CD,TH1}$ and can be calculated as follows:

$t_D = (V_{CD,TH1} \times C_{CD}) / I_{CH1}$
$C_{CD} = (t_D \times I_{CH1}) / V_{CD,TH1}$
where I_{CH1} = CD charge current = 0.2 µA (typical)

The recovery delay time is the time between discharging from $V_{CD,TH2}$ to $V_{CD,TH1}$. The minimum output active time (t_{OA}) can be calculated as follows:

$t_{OA} = (V_{CD,TH2} - V_{CD,TH1}) \times C_{CD}) / I_{DS1}$
$C_{CD} = (t_{OA} \times I_{DS1}) / (V_{CD,TH2} - V_{CD,TH1})$
where I_{DS1} = CD discharge current = 0.2 µA (typical)

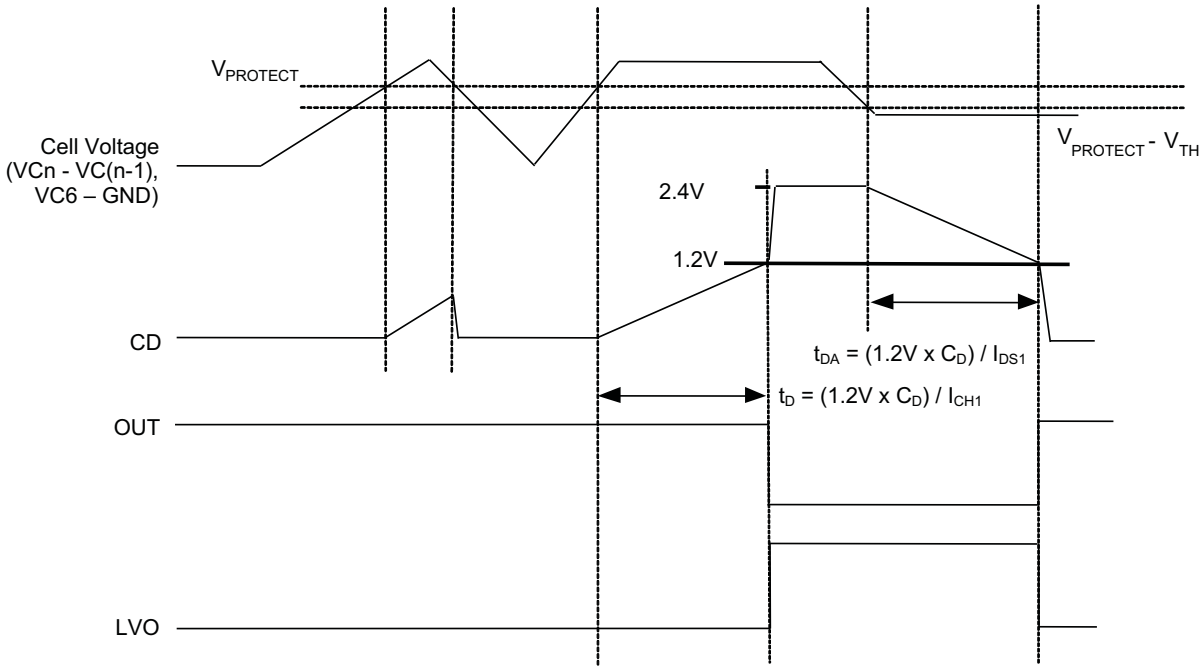

Figure 5. Timing for Overvoltage Sensing (With Recovery Option)

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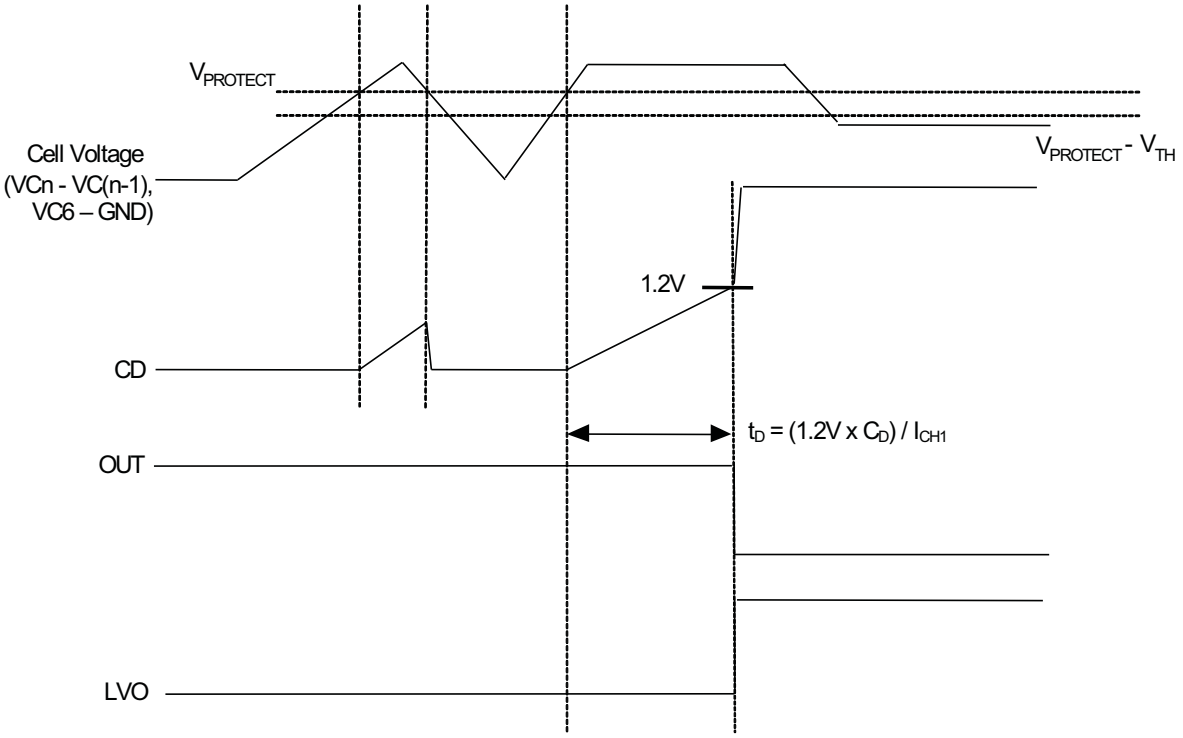

Figure 6. Timing for Overvoltage Sensing (Without Recovery Option – Permanent Latch)

From Level Shift Input

More than six cells can be monitored with multiple bq77PL157 devices by using the LVO and LVIN pins to cascade or stack multiple parts. The LVO pin from the *upper* bq77PL157 is connected to the LVIN pin of the *lower* bq77PL157. The OUT pin of the *lowest* bq77PL157 is used to control the activation element while the OUT pins of the upper bq77PL157 devices are not used.

When the LVIN pin changes from a low to high level, an internal current source begins to charge capacitor C_{CD}, connected to the CD pin, quickly. If the voltage at the CD pin, V_{CD}, reaches $V_{CD,TH1}$ (1.2 V typical), then the OUT pin and the LVO pin are both activated. Once the output is activated, the CD pin continues to charge up to its maximum value of $V_{CD,TH2}$ (2.4 V typical).

The delay time from LVIN to either LVO or OUT is minimized by quickly charging the CD pin and is approximately 10 times faster than the delay time from an overvoltage fault at the direct cell inputs. When more than two bq77PL157 devices are stacked, this delay time is additive.

The delay time per device can be calculated as follows:

$t_{DA} = (V_{CD,TH1} \times C_{CD}) / I_{CHLV}$
where IC_{HLV} = CD charge current = 10 × I_{CH1} = 2 µA (typical)

When the LVIN pin changes from a high to low level, an internal switch clamps the CD pin to GND, discharging the capacitor C_{CD}. The delay time (per part) can be calculated as follows.

$t_{DIA} = (V_{CD,TH2} – V_{CD,TH1}) \times C_{CD} / I_{DSLV}$
where I_{DSLV} = CD discharge current = 90 µA (typical)

To find the total expected delay time from LVIN to OUT, a variable internal latency of approximately 4 - 12 ms should be added.

Faults detected via LVIN have the highest priority and will interrupt the timing of all lower priority faults.

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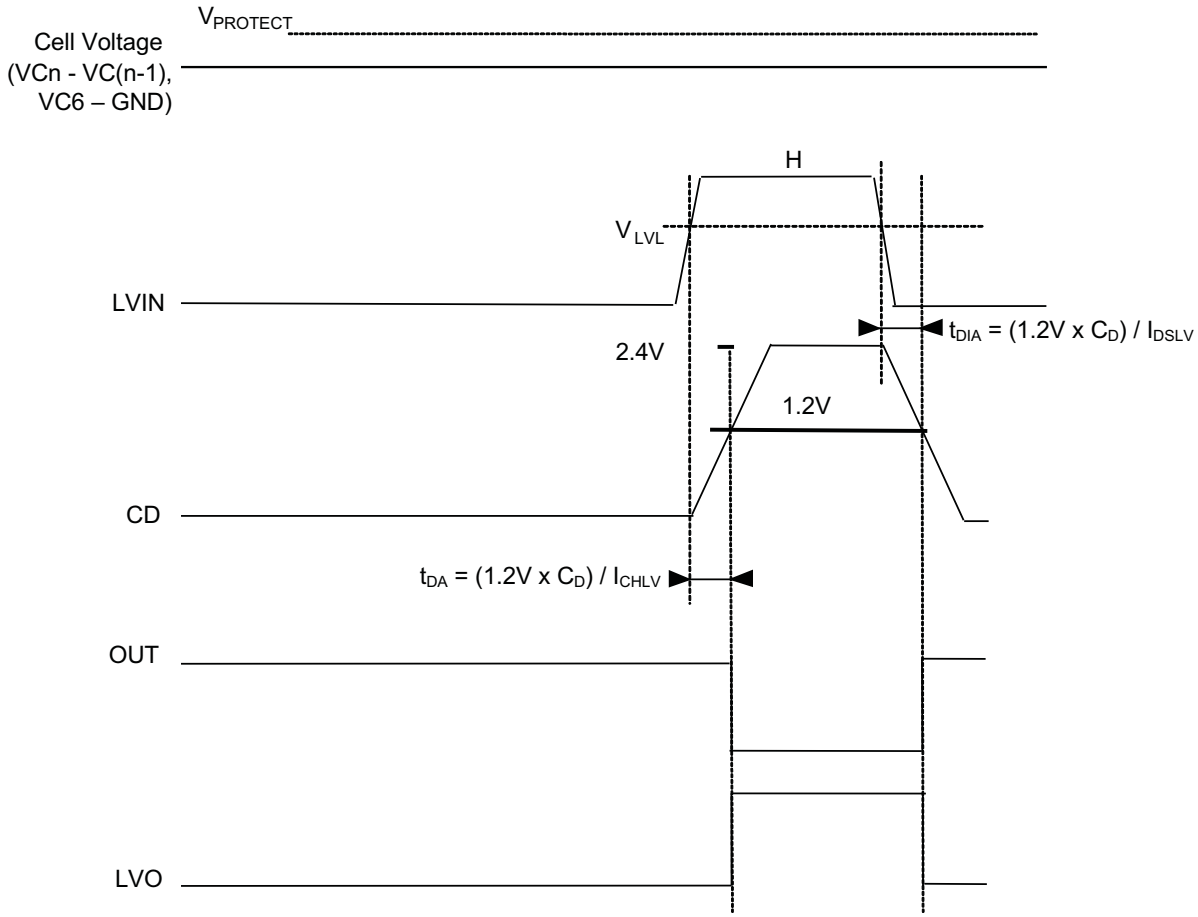

Figure 7. LVIN to OUT and LVO Timing

CELL CONNECTION SEQUENCE

Unused VCx cell input pins should be connected to the most positive connected cell input pin as shown in the *Battery Connection Diagrams* section. VDD is connected through a resistor to the most-positive VCx pin of the cell stack. Note that VC1 is the most-positive connection to the most-positive cell.

During pack assembly, it is recommended that the cell input pins be connected in order from lowest to highest potential: GND, VC6, VC5, VC4, VC3, VC2, VC1.

NOTE

if a random cell connection order is used, a false overvoltage condition may be sensed depending on the order of connection.

To prevent a fault from being detected in this scenario, the CD pin may be held low so that the fault timer is disabled and OUT and LVO will not be activated. Alternatively, the VDD pin may be held low during cell connection, or pulsed low after cell connection in order to reset the device.

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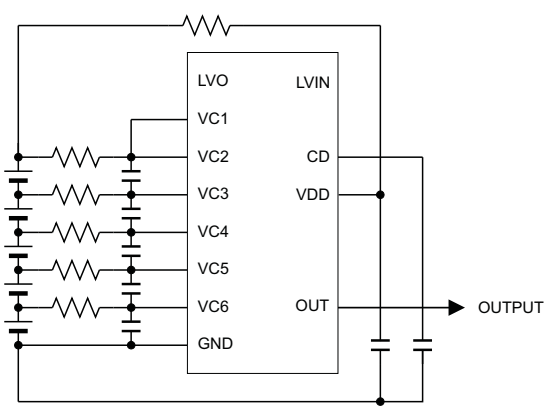
BATTERY CONNECTION DIAGRAMS

The following schematics indicate the cell connections for several battery configurations. Unused cell inputs should be connected together on the most positive end of the cell stack. **(VC1 is the most positive input.)**

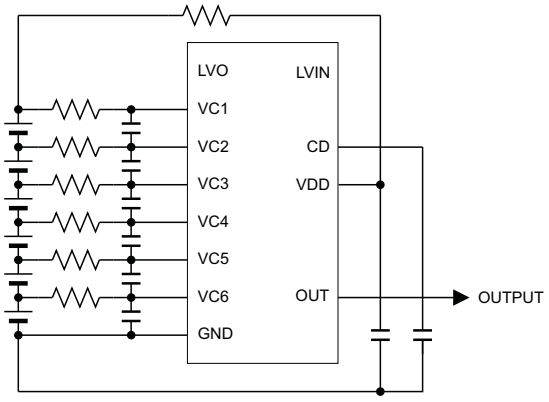
The PCKP and PCKN pins supply power to the output FET driver. PCKP is always connected to the most positive cell input of the device. PCKN for a single device or the bottom device in a stack is connected to the source terminal of the protection FET device. For an upper device in a stacked configuration, PCKN is connected to GND.

NOTE

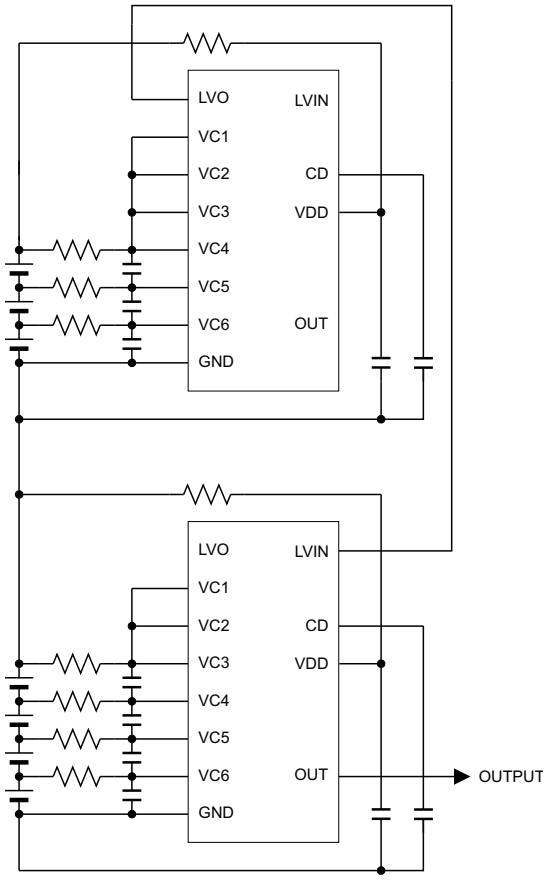
Not all connections shown. Diagrams are simplifications of full circuits and do not include key constraints when stacking these parts.



5 Cells



6 Cells



7 Cells (Stacked)

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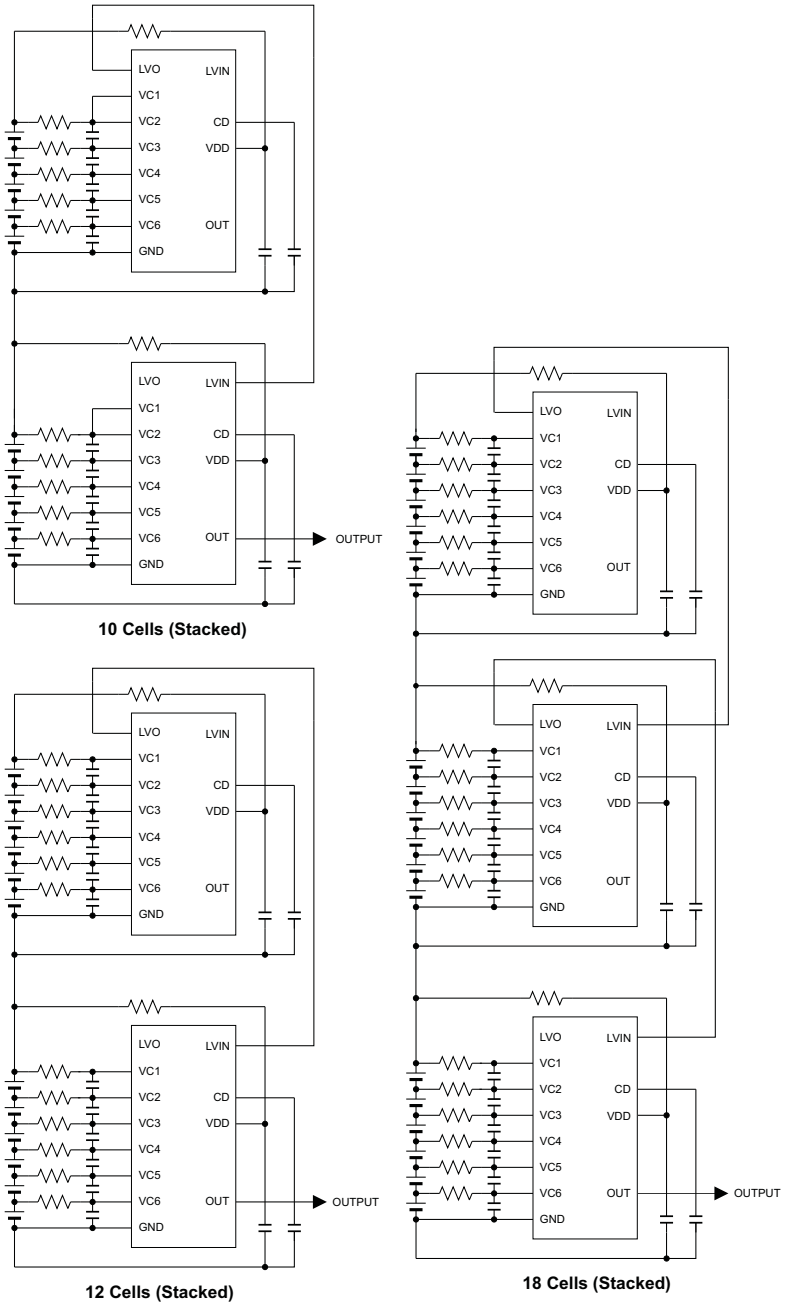

REDUCING TEST TIME

By controlling the CD pin, it is possible to reduce the time for functional test at PC board assembly:

To make a shorter overvoltage delay time, pull the CD pin over 1.2 V (typ) (MAX to VDD).

To recover from an overvoltage condition, pull the CD pin down to GND and set cell VCx < $V_{PROTECT} - V_{TH}$.

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REVISION HISTORY

Changes from Original (March 2010) to Revision A **Page**

- Changed the overvoltage detection hysteresis (V_{TH}) minimum value of 100 mV to 150 mV 4

Changes from Revision A (October 2011) to Revision B **Page**

- Changed Features Item From: Fixed Overvoltage Thresholds Available From 3.75 V to 4.35 V in 25-mV Steps To: Fixed 4.225 V Overvoltage Threshold 1
- Changed the DESCRIPTION paragraph 1
- Changed the ORDERING INFORMATION section 2
- Deleted Test Conditions for $V_{PROTECT}$. Deleted the MIN and MAX values. Added a TYP value of 4.225 V 4

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ77PL157APW-4225	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ODZ	Samples
BQ77PL157APWR-4225	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ODZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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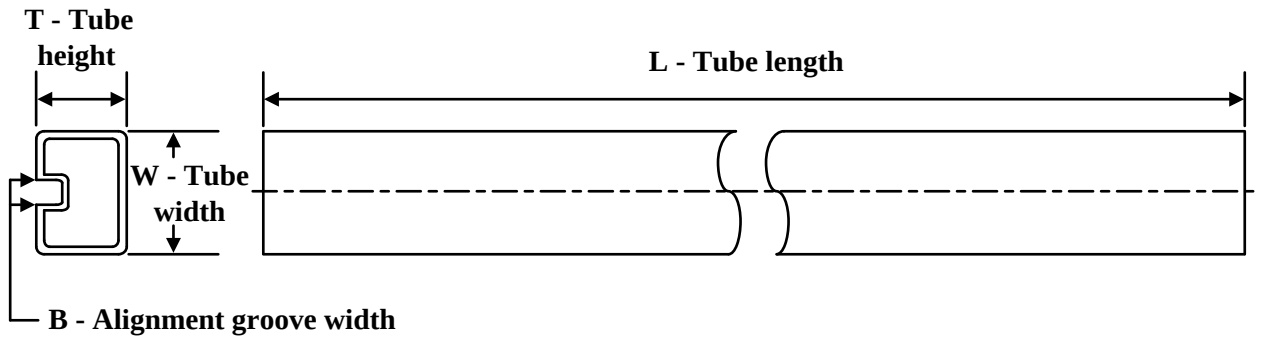
TUBE



*All dimensions are nominal

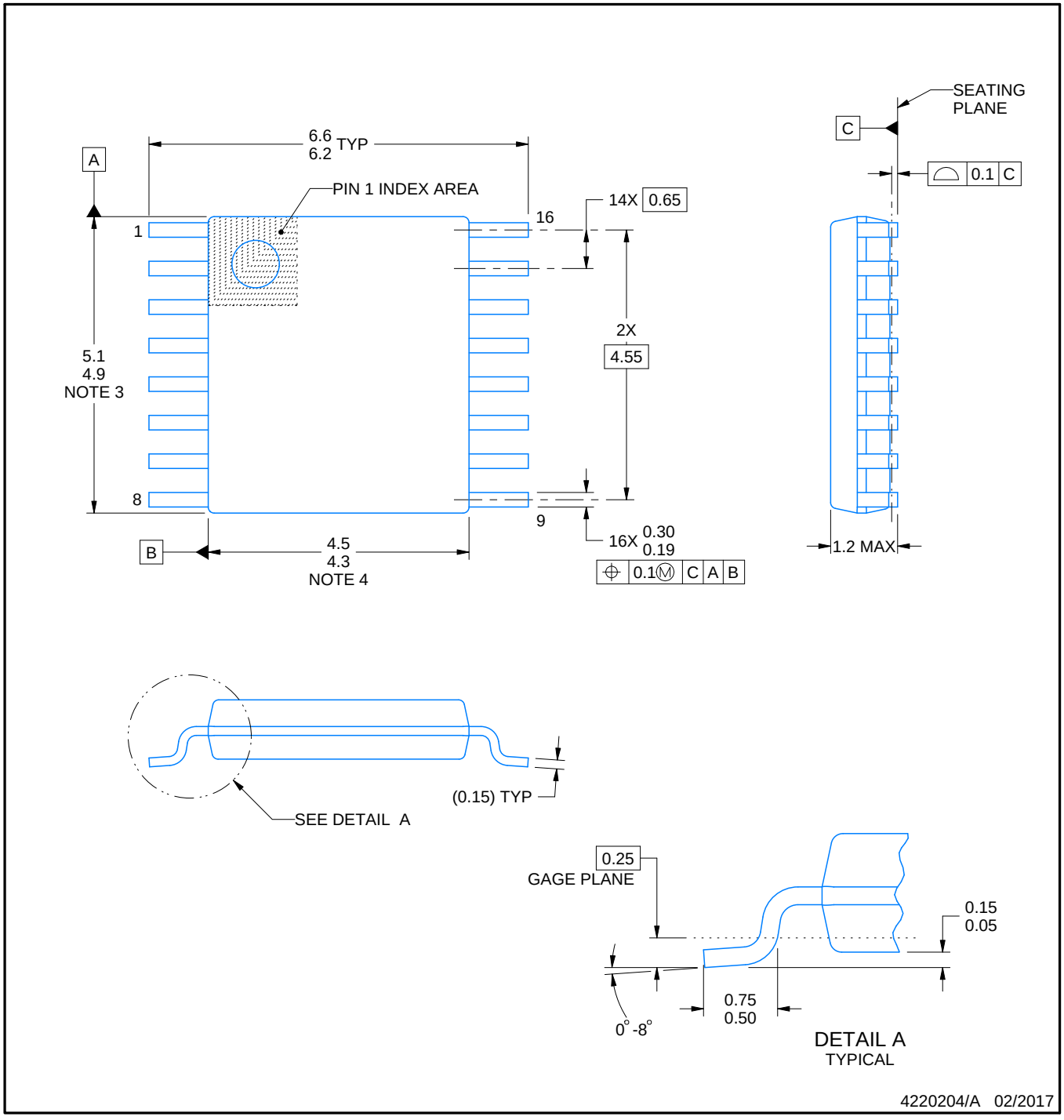
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ77PL157APW-4225	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

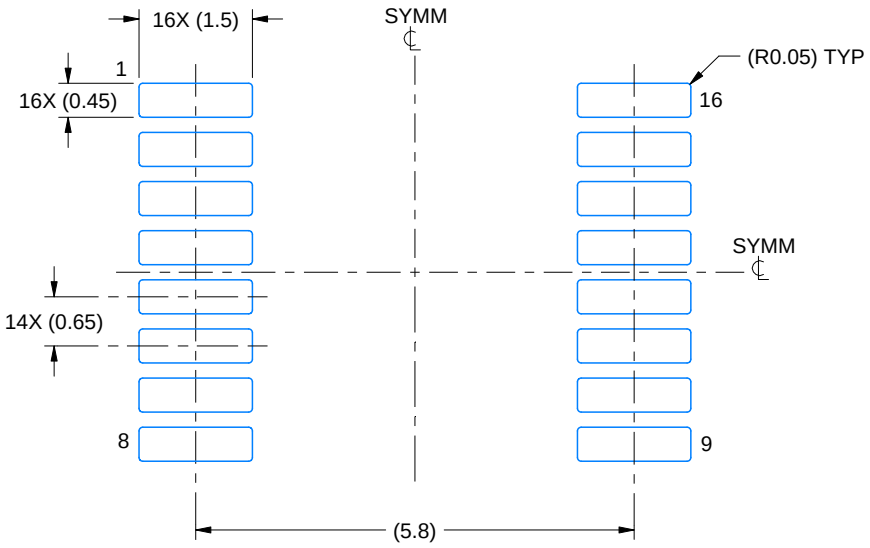
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

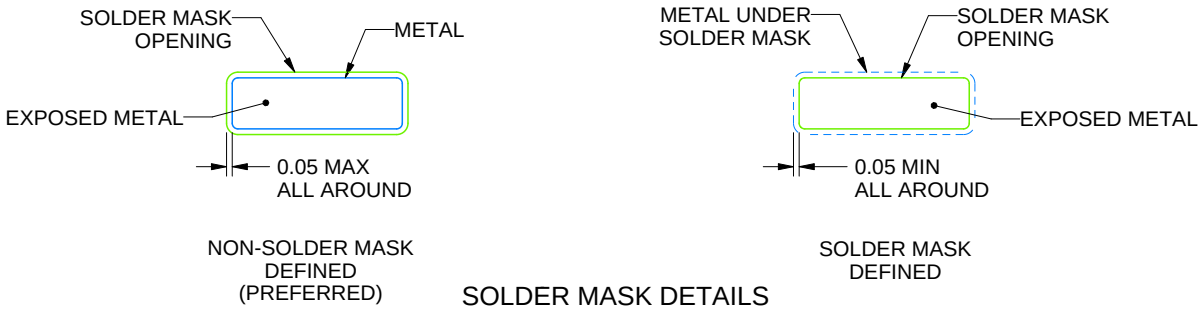


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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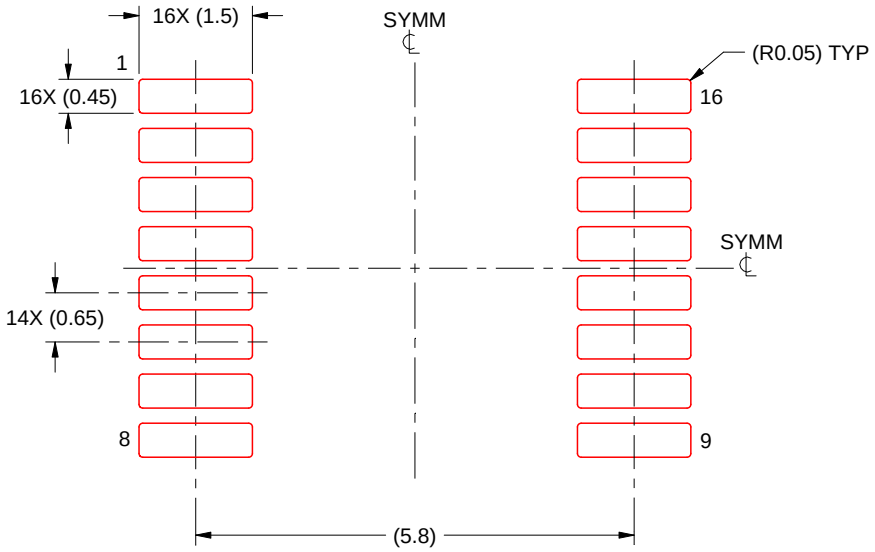
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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