

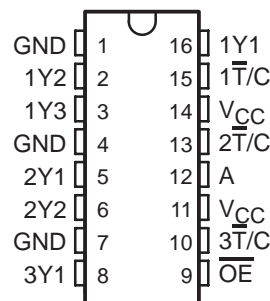
CDC391

1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY AND 3-STATE OUTPUTS

SCAS334A – DECEMBER 1992 – REVISED NOVEMBER 1995

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Six Clock Outputs
- Polarity Control Selects True or Complementary Outputs
- Distributed V_{CC} and GND Pins Reduce Switching Noise
- High-Drive Outputs ($-48\text{-mA } I_{OH}$, $48\text{-mA } I_{OL}$)
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Packaged in Plastic Small-Outline Package

**D PACKAGE
(TOP VIEW)**



description

The CDC391 contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control ($\overline{T/C}$) inputs, various combinations of true and complementary outputs can be obtained. The output-enable (\overline{OE}) input is provided to disable the outputs to a high-impedance state.

The CDC391 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}	$\overline{T/C}$	A	Y
H	X	X	Z
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L



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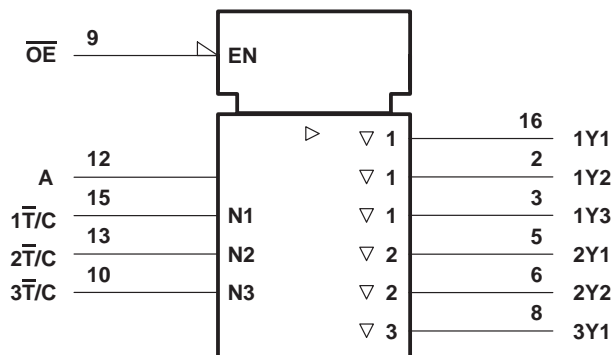
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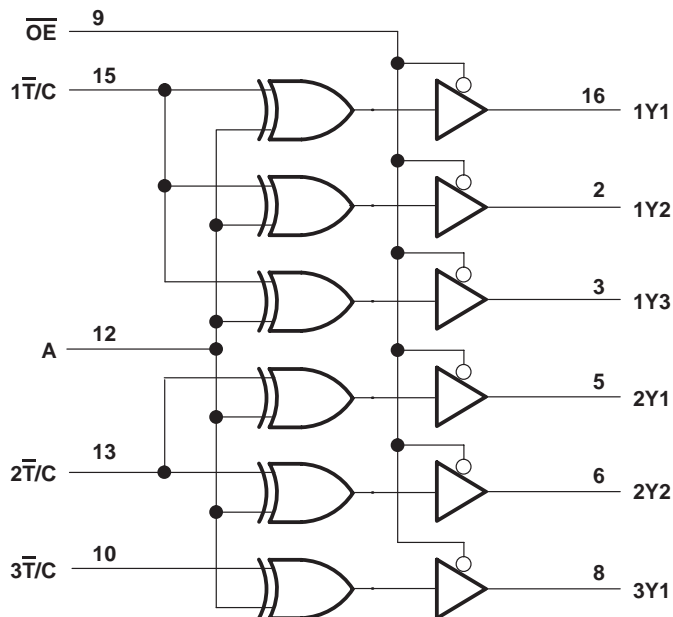
SCAS334A – DECEMBER 1992 – REVISED NOVEMBER 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



CDC391

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SCAS334A – DECEMBER 1992 – REVISED NOVEMBER 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	0.77 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 300 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
V_I Input voltage	0	V_{CC}		V
I_{OH} High-level output current			–48	mA
I_{OL} Low-level output current			48	mA
$\Delta t/\Delta v$ Input transition rise or fall rate			5	ns/V
f_{clock} Input clock frequency			100	MHz
T_A Operating free-air temperature	–40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	$V_{CC} = 4.75$ V,	$I_I = -18$ mA			–1.2	V
V_{OH}	$V_{CC} = 4.75$ V,	$I_{OH} = -48$ mA	2			V
V_{OL}	$V_{CC} = 4.75$ V,	$I_{OL} = 48$ mA			0.5	V
I_I	$V_{CC} = 5.25$ V,	$V_I = V_{CC}$ or GND			± 1	μA
I_{OZ}	$V_{CC} = 5.25$ V,	$V_O = V_{CC}$ or GND			± 50	μA
I_{O}^{\S}	$V_{CC} = 5.25$ V,	$V_O = 2.5$ V	–15		–100	mA
I_{CC}	$V_{CC} = 5.25$ V, $V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high		10	mA
			Outputs low		40	
			Outputs disabled		10	
C_i	$V_I = 2.5$ V or 0.5 V			3		pF
C_o	$V_O = 2.5$ V or 0.5 V			5		pF

‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.



CDC391
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SCAS334A – DECEMBER 1992 – REVISED NOVEMBER 1995

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

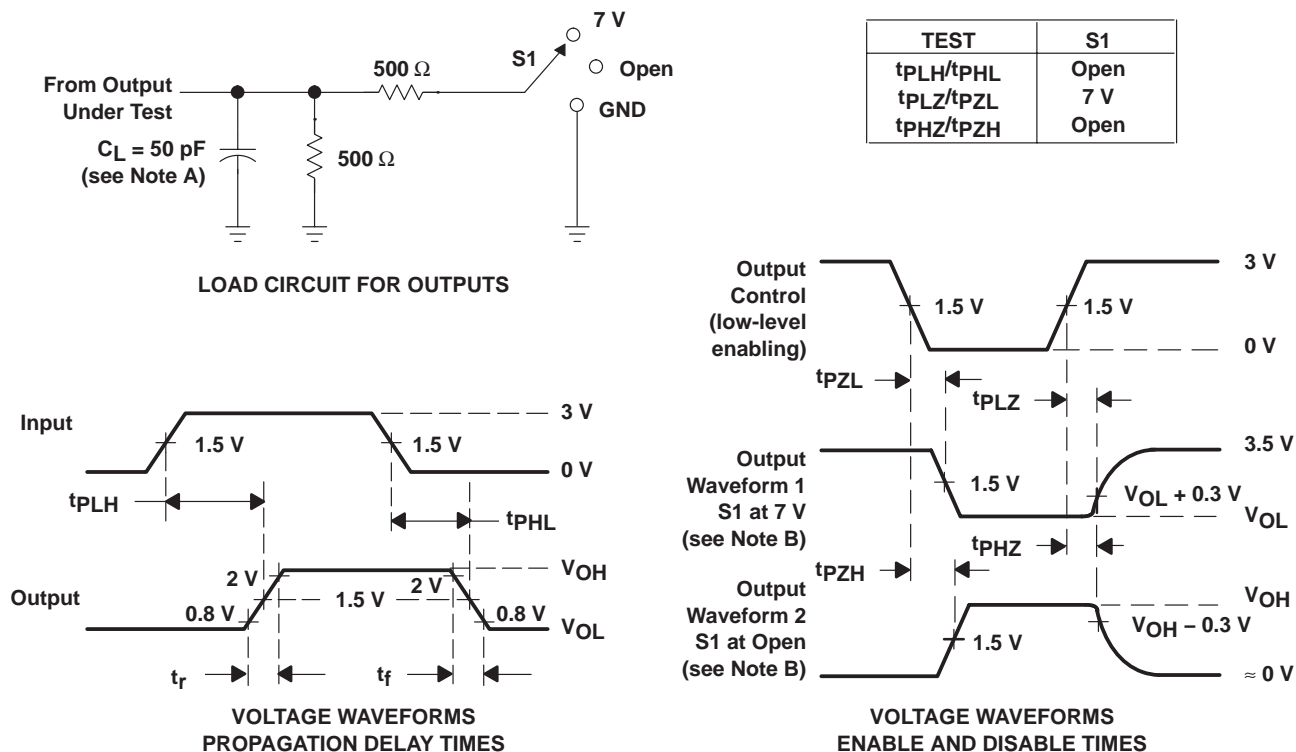
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t _{PLH}	A	Any Y	1.5	5	ns
t _{PHL}			1.5	5	
t _{PLH}	\bar{T}/C	Any Y	1.5	5	ns
t _{PHL}			1.5	5	
t _{PZH}	\overline{OE}	Any Y	1.5	5	ns
t _{PZL}			3	7	
t _{PHZ}	\overline{OE}	Any Y		5	ns
t _{PLZ}				5	
t _{sk(o)}	A	Any Y (same phase)		0.5	ns
		Any Y (any phase)		1	
t _{sk(p)}	A	Any Y		1	ns
t _r				1.5	ns
t _f				1.5	ns



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SCAS334A – DECEMBER 1992 – REVISED NOVEMBER 1995

PARAMETER MEASUREMENT INFORMATION



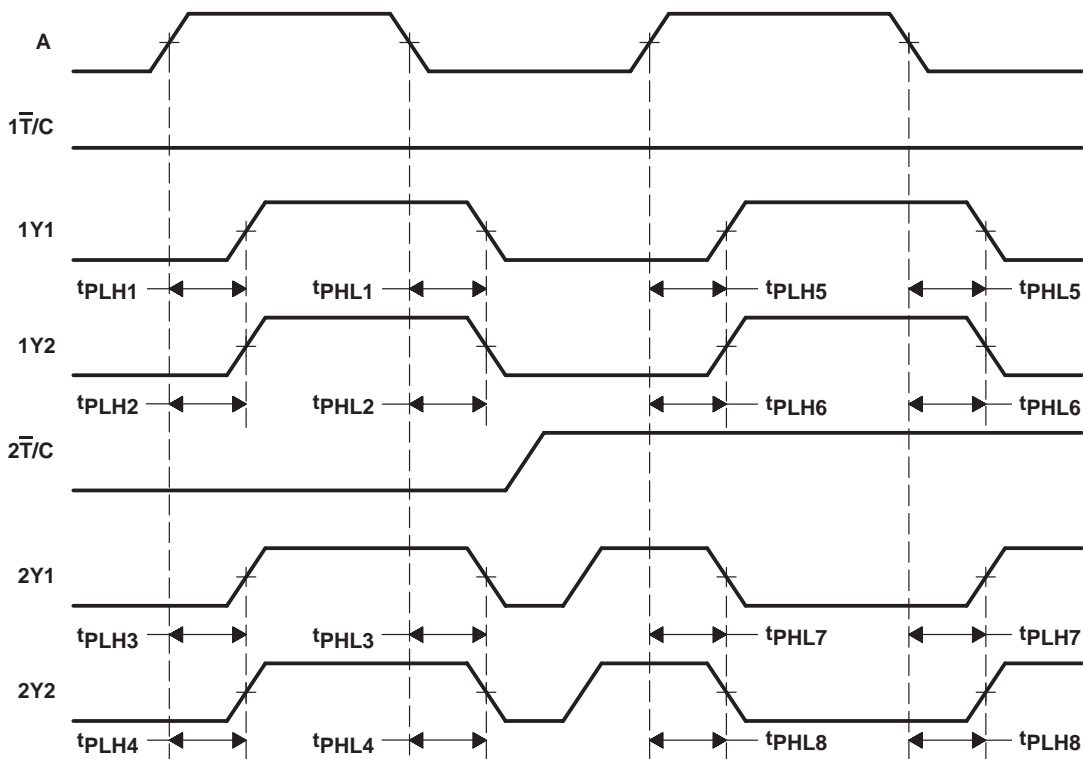
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

CDC391
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SCAS334A – DECEMBER 1992 – REVISED NOVEMBER 1995

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T/C}$) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from $A\uparrow$ to any Y (e.g., t_{PLHn} , $n = 1$ to 4; or t_{PLHn} , $n = 5$ to 6)
 - The difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6)
 - The difference between the fastest and slowest of t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PLHn} , $n = 7$ to 8)
 - The difference between the fastest and slowest of t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PHLn} , $n = 7$ to 8)
- B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T/C}$) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from $A\uparrow$ to any Y or t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PLHn} , $n = 1$ to 4; or t_{PLHn} , $n = 5$ to 6, and t_{PHLn} , $n = 7$ to 8)
 - The difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y or t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6, and t_{PLHn} , $n = 7$ to 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC391D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC391	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

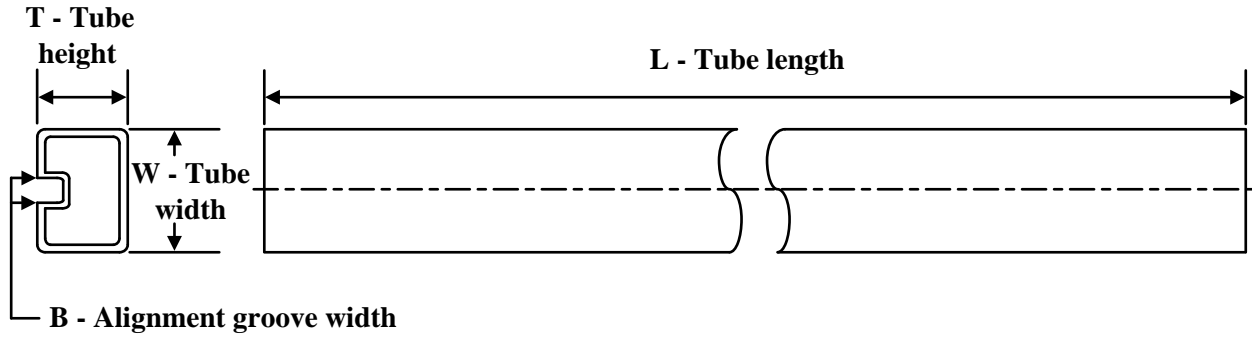
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDC391D	D	SOIC	16	40	505.46	6.76	3810	4

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