CSD18533KCS 60V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

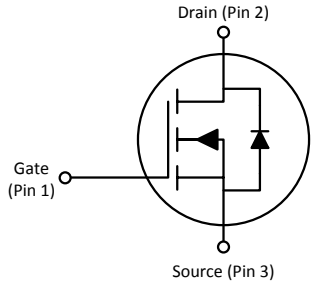
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 逻辑电平
- 无铅端子镀层
- 符合 RoHS 环保标准
- 无卤素
- 晶体管 (TO)-220 塑料封装

2 应用范围

- 直流 - 直流转换
- 次级侧同步整流器
- 电机控制

3 说明

这款 5.0mΩ，60V TO-220 NexFET™ 功率 MOSFET 被设计成在功率转换应用中最大限度地降低损耗。



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	60		V
Q_g	栅极电荷总量 (10V)	28		nC
Q_{gd}	栅漏栅极电荷	3.9		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 4.5V	6.9	mΩ
		V_{GS} = 10V	5.0	mΩ
$V_{GS(th)}$	阈值电压	1.9		V

订购信息

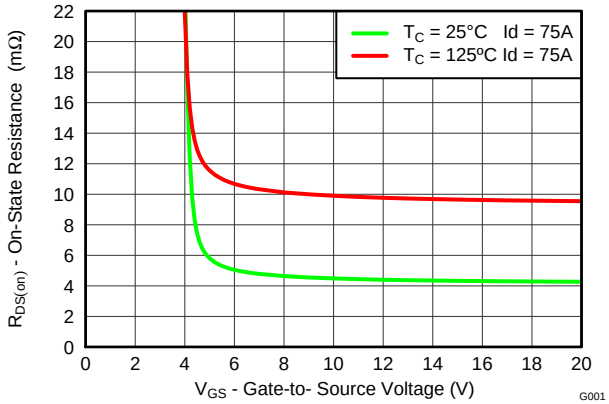
器件	封装	介质	数量	出货
CSD18533KCS	TO-220 塑料封装	管	50	管

最大绝对额定值

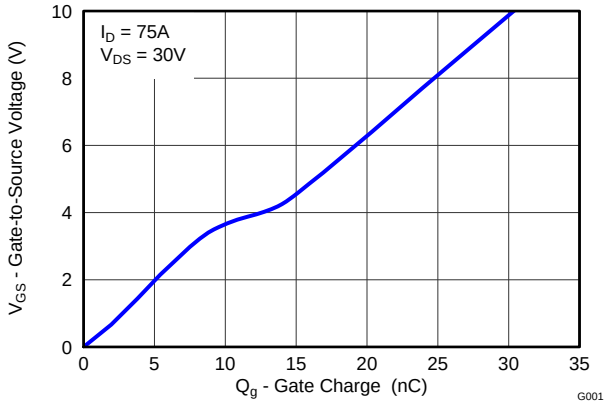
T_A = 25°C		值	单位
V_{DS}	漏源电压	60	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	118	
	持续漏极电流（受芯片限制），T_C = 100°C 时测得	84	
I_{DM}	脉冲漏极电流 (1)	140	A
P_D	功率耗散	192	W
T_J, T_{stg}	运行结温和储存温度范围	-55 至 175	°C
E_{AS}	雪崩能量，单脉冲 I_D = 52A，L = 0.1mH，R_G = 25Ω	135	mJ

(1) 脉冲持续时间 ≤ 300μs，占空比 ≤ 2%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2013) to Revision B **Page**

- 已将文档标题更新为包含产品型号 1
- 已更新产品说明 1
- 已将电流增加为反映最大温度情况下电流的增加量 1
- 已将最大功率增加为反映最大温度情况下的最大功率增加量 1
- 已将最大温度增加为 175°C 1
- Updated Figure 6 to extend to 175ºC 5
- Updated Figure 8 to extend to 175ºC 5
- Updated Figure 12 to extend to 175ºC 6

Changes from Original (September 2012) to Revision A **Page**

- Changed $Q_{g(th)}$, Gate Charge at V_{th} value From: 7.3 To: 4.6 3

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.5	1.9	2.3	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V, I_D = 75 A		6.9	9.0	mΩ
		V_{GS} = 10 V, I_D = 75 A		5.0	6.3	mΩ
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 75 A		150		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		2420	3025	pF
C_{oss}	Output Capacitance			300	375	pF
C_{rss}	Reverse Transfer Capacitance			7	9.1	pF
R_G	Series Gate Resistance			1.4	2.8	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = 30 V, I_D = 75 A		14	17	nC
Q_g	Gate Charge Total (10 V)			28	34	nC
Q_{gd}	Gate Charge Gate to Drain			3.9		nC
Q_{gs}	Gate Charge Gate to Source			9.4		nC
$Q_{g(th)}$	Gate Charge at V_{th}			4.6		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		31		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 75 A, R_G = 0 Ω		5.7		ns
t_r	Rise Time			4.8		ns
$t_{d(off)}$	Turn Off Delay Time			13		ns
t_f	Fall Time			3.2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 75 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30 V, I_F = 75 A, di/dt = 300 A/µs		97		nC
t_{rr}	Reverse Recovery Time			49		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.8	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	°C/W

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

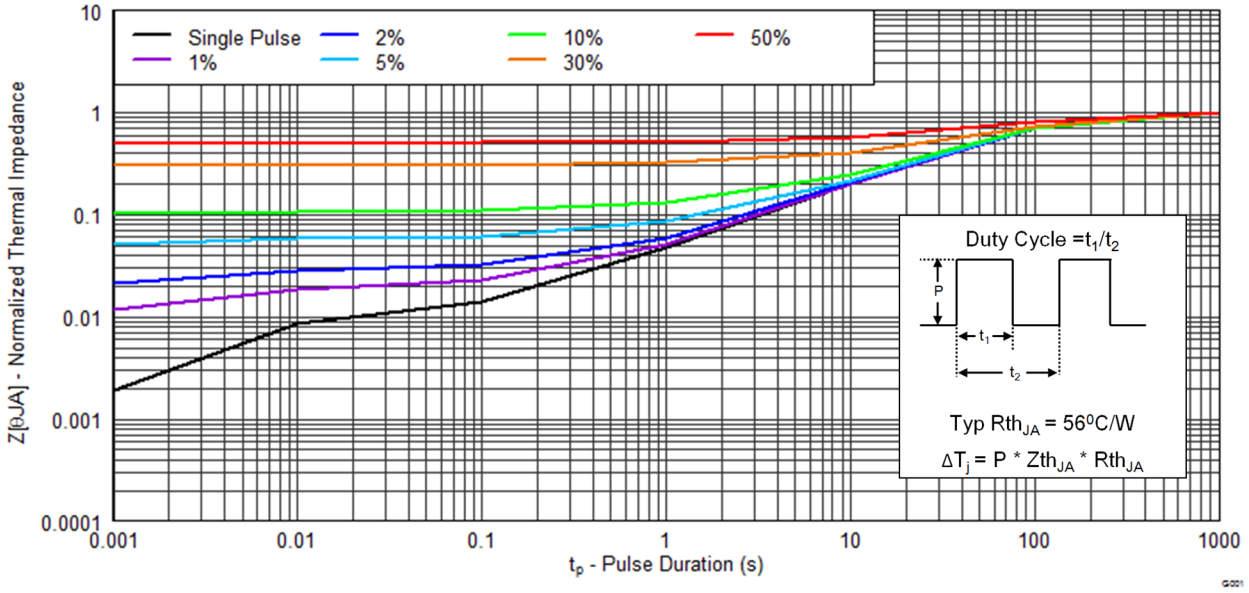


Figure 1. Transient Thermal Impedance

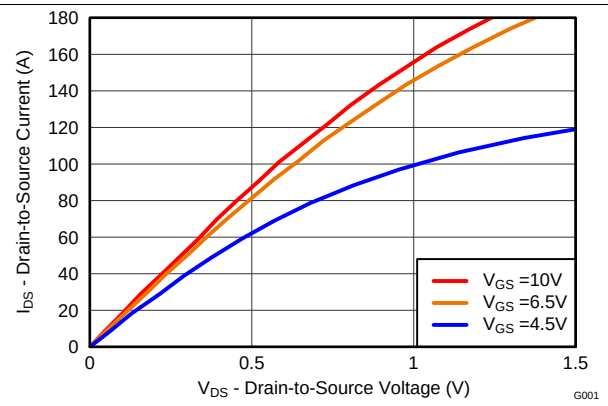


Figure 2. Saturation Characteristics

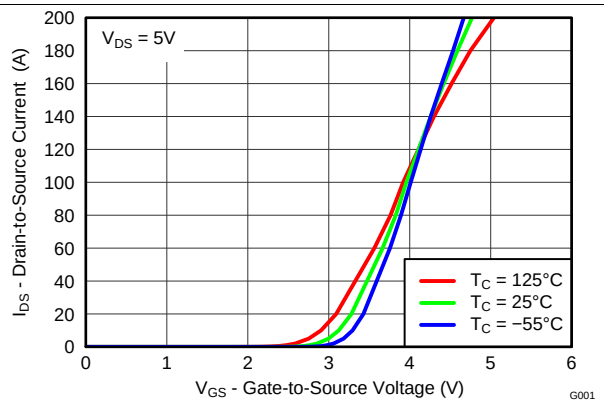


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

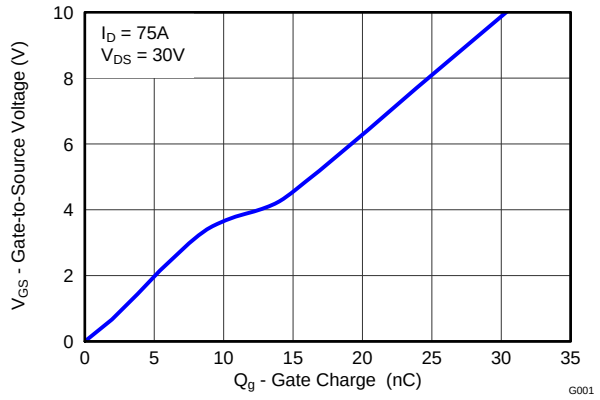


Figure 4. Gate Charge

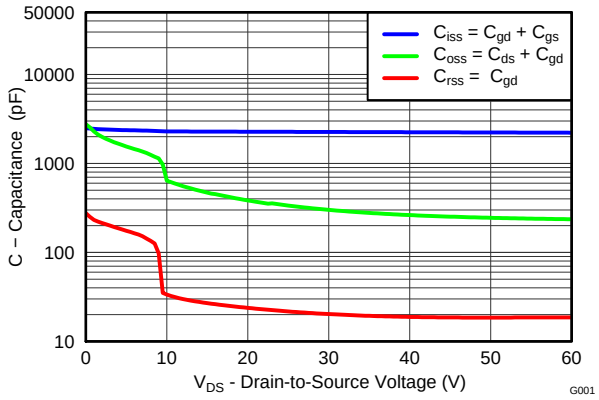


Figure 5. Capacitance

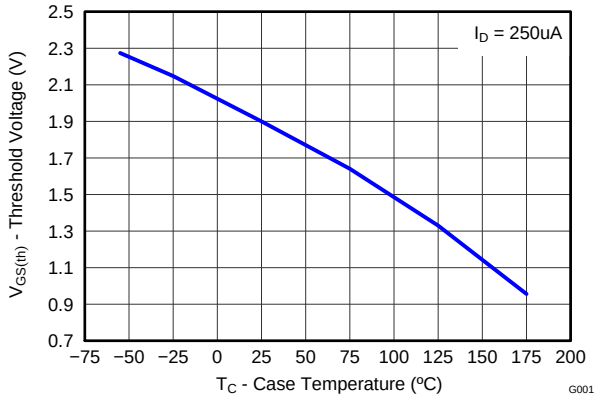


Figure 6. Threshold Voltage vs Temperature

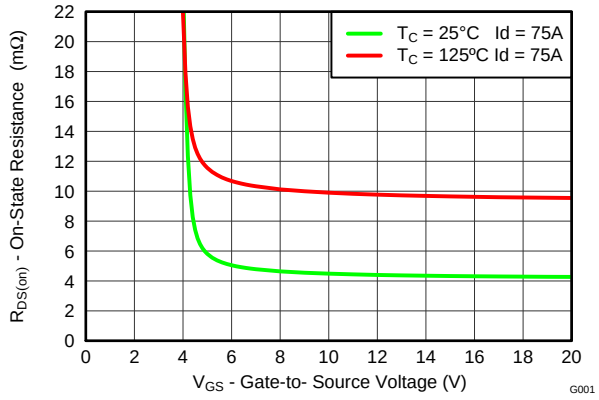


Figure 7. On-State Resistance vs Gate-to-Source Voltage

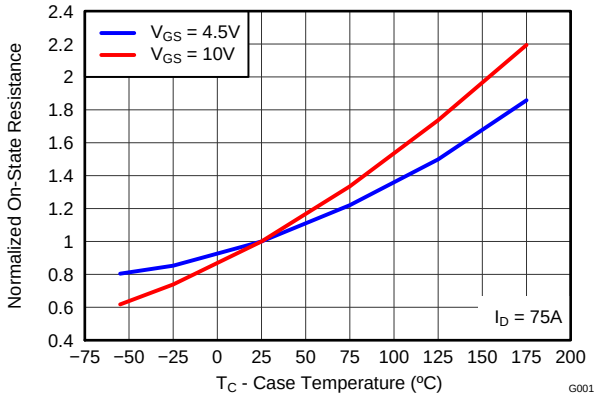


Figure 8. Normalized On-State Resistance vs Temperature

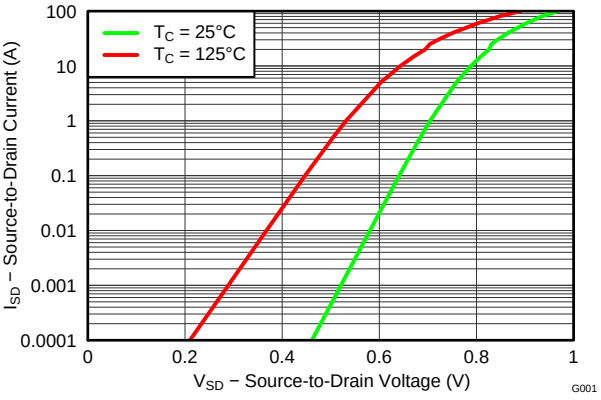


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

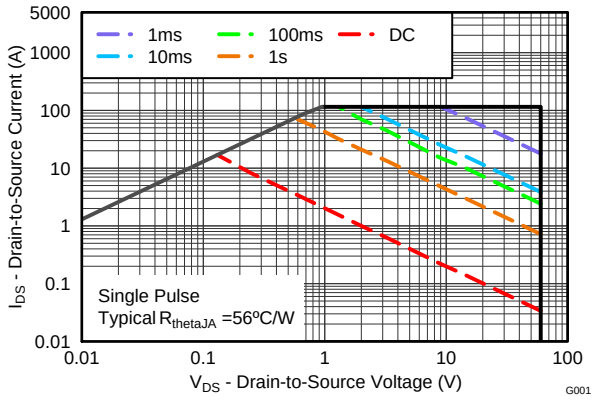


Figure 10. Maximum Safe Operating Area

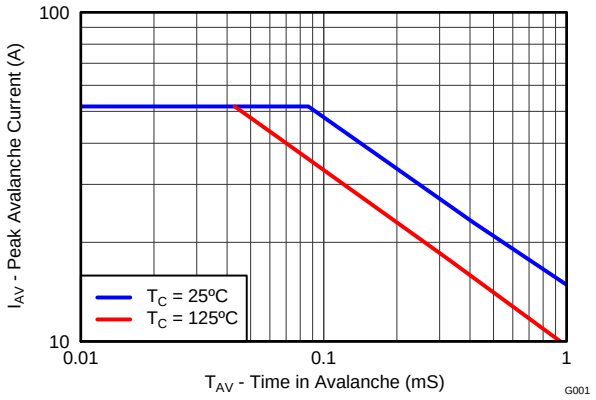


Figure 11. Single Pulse Unclamped Inductive Switching

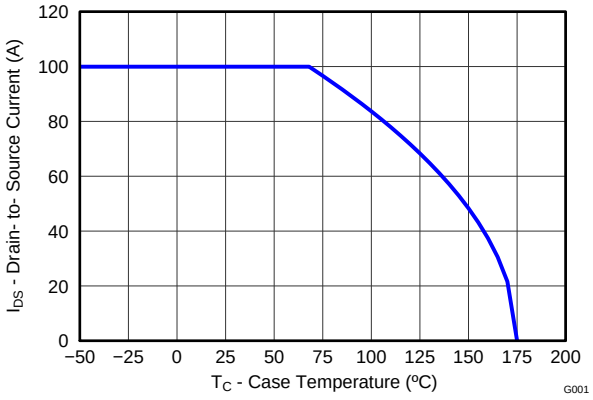


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

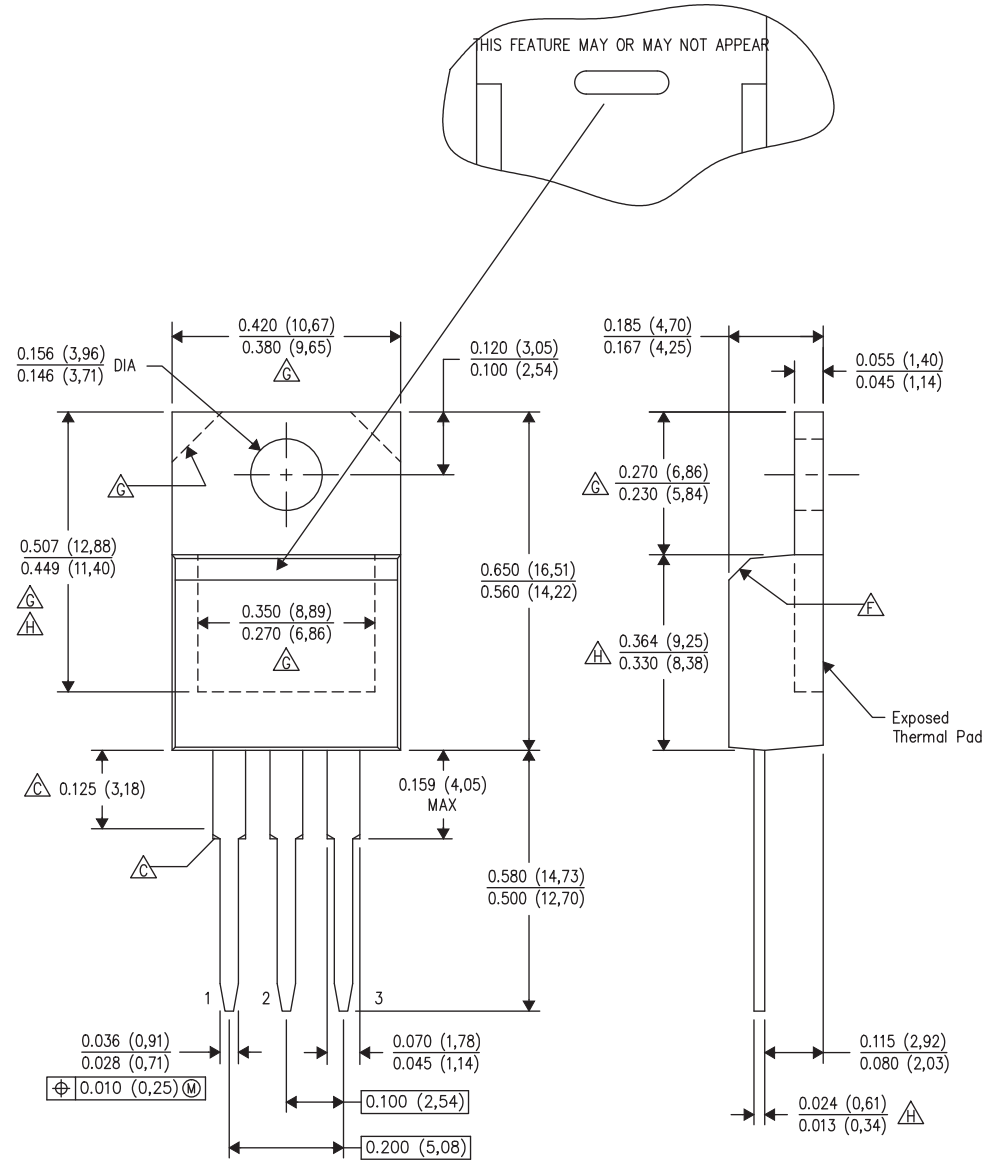
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

7 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧导航栏。

7.1 KCS 封装尺寸



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Thermal pad contour optional within these dimensions.
H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

端子配置

位置	名称
端子 1	栅极
端子 2 / 标签	漏
端子 3	源

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18533KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD18533KCS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

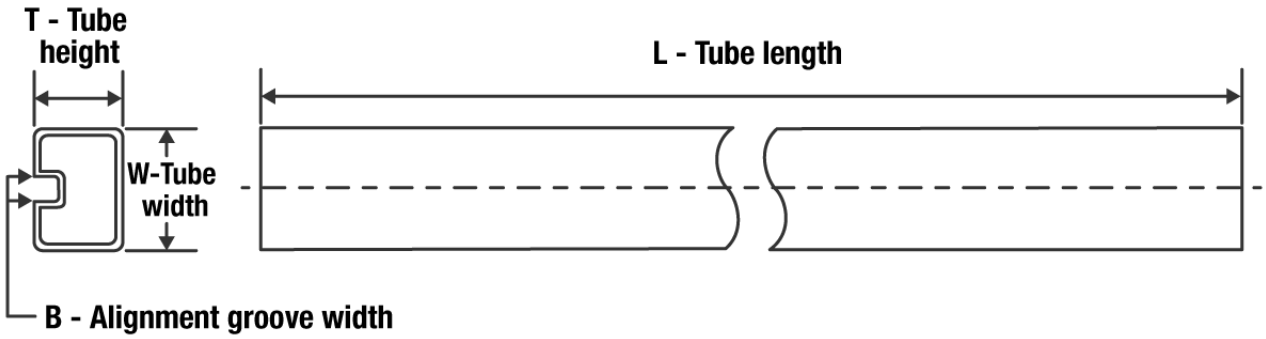
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CSD18533KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD18533KCS	KCS	TO-220	3	50	532	34.1	700	9.6

重要声明和免责声明

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