

# 双路 30V N 通道 NextFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

## 特性

- 共源连接
- 超低漏极到漏极导通电阻
- 节省空间的小外形尺寸无引线 (SON) 3.3mm x 3.3mm 塑料封装
- 针对 5V 栅极驱动进行了优化
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS 标准
- 无卤素

## 应用范围

- 针对笔记本个人电脑 (PC) 和平板电脑的适配器 / USB 输入保护

## 说明

CSD87312Q3E 是一款设计用于适配器 / USB 输入保护的 30V 共源、双路 N 通道器件。此类 SON 3.3mm x 3.3mm 器件有低漏极到漏极导通电阻，这大大减少了损耗并且为空间受限的多节电池充电类应用提供低组件数量。

## 产品概述

T <sub>A</sub> =25°C		典型值	单位
V <sub>DS</sub>	漏源电压	30	V
Q <sub>g</sub>	栅极电荷总量 (4.5V)	6.3	nC
Q <sub>gd</sub>	栅漏栅极电荷	0.7	nC
R <sub>DD</sub> (导通)	漏极到漏极导通电阻 (Q1+Q2)	V <sub>GS</sub> =4.5V	31 mΩ
		V <sub>GS</sub> =8V	27 mΩ
V <sub>GS(th)</sub>	阈值电压	1.0	V

## 订购信息

器件	封装	介质	数量	出货
CSD87312Q3E	小外形尺寸无引线 (SON) 3.3mm x 3.3mm 塑料封装	13 英寸卷带	2500	卷带封装

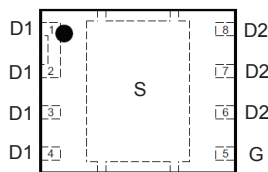
## 绝对最大额定值

T <sub>A</sub> =25°C		值	单位
V <sub>DS</sub>	漏源电压	30	V
V <sub>GS</sub>	栅源电压	+10/-8	V
I <sub>D</sub>	持续漏极电流, T <sub>C</sub> =25°C 时测得 <sup>(1)</sup>	27	A
I <sub>DM</sub>	脉冲漏极电流 <sup>(2)</sup>	45	A
P <sub>D</sub>	功率耗散	2.5	W
T <sub>J</sub> , T <sub>STG</sub>	运行结温和储存温度范围	-55 至 150	°C
E <sub>AS</sub>	雪崩能量, 单一脉冲 I <sub>D</sub> =24A, L=0.1mH, R <sub>G</sub> =25Ω	29	mJ

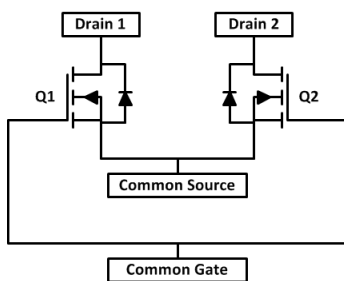
(1) R=63°C/W, 这是在厚度为 0.060" 的环氧板印刷电路板 (FR4PCB) 上 1 in<sup>2</sup> (2 盎司) 铜过渡垫片上测得的典型值

(2) 脉冲持续时间 ≤ 300μs, 占空比 ≤ 2%

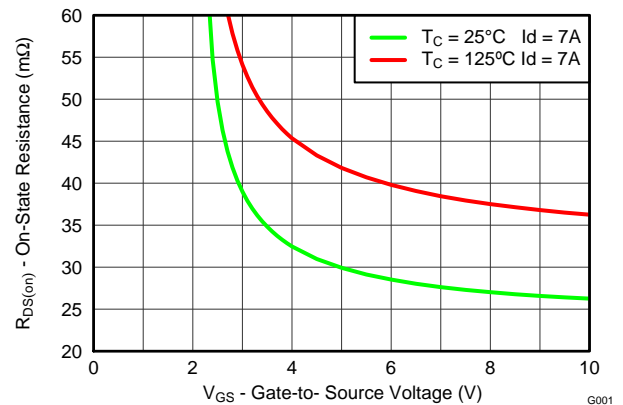
俯视图



电路图象



V<sub>GS</sub>与 R<sub>DDon</sub>间的关系



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10/-8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.8	1.0	1.3	V
$R_{DD(on)}$	Drain to Drain On Resistance (Q1 + Q2)	$V_{GS} = 4.5V, I_D = 7A$		31	38	$m\Omega$
		$V_{GS} = 8V, I_D = 7A$		27	33	$m\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_D = 7A$		39		S
<b>Dynamic Characteristics<sup>(1)</sup></b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		960	1250	pF
$C_{oss}$	Output Capacitance			190	247	pF
$C_{riss}$	Reverse Transfer Capacitance			12	16	pF
$R_G$	Series Gate Resistance			5	10	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_D = 7A$		6.3	8.2	nC
$Q_{gd}$	Gate Charge Gate to Drain			0.7		nC
$Q_{gs}$	Gate Charge Gate to Source			1.9		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			1.0		nC
$Q_{oss}$	Output Charge	$V_{DS} = 15V, V_{GS} = 0V$		4.0		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 7A, R_G = 2\Omega$		7.8		ns
$t_r$	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			17		ns
$t_f$	Fall Time			2.9		ns
<b>Diode Characteristics<sup>(1)</sup></b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 7A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 15V, I_F = 7A, di/dt = 300A/\mu s$		5.3		nC
$t_{rr}$	Reverse Recovery Time			12.2		ns

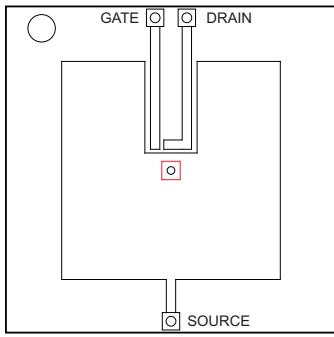
(1) All Dynamic and Diode Characteristics were measured with respect to one of the two drains, with the other left floating.

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

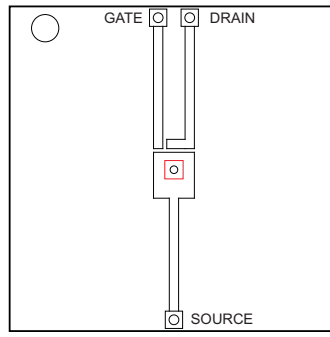
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			4.2	$^\circ\text{C}/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			63	$^\circ\text{C}/W$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 63^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of 2-  
oz. (0.071-mm thick)  
Cu.

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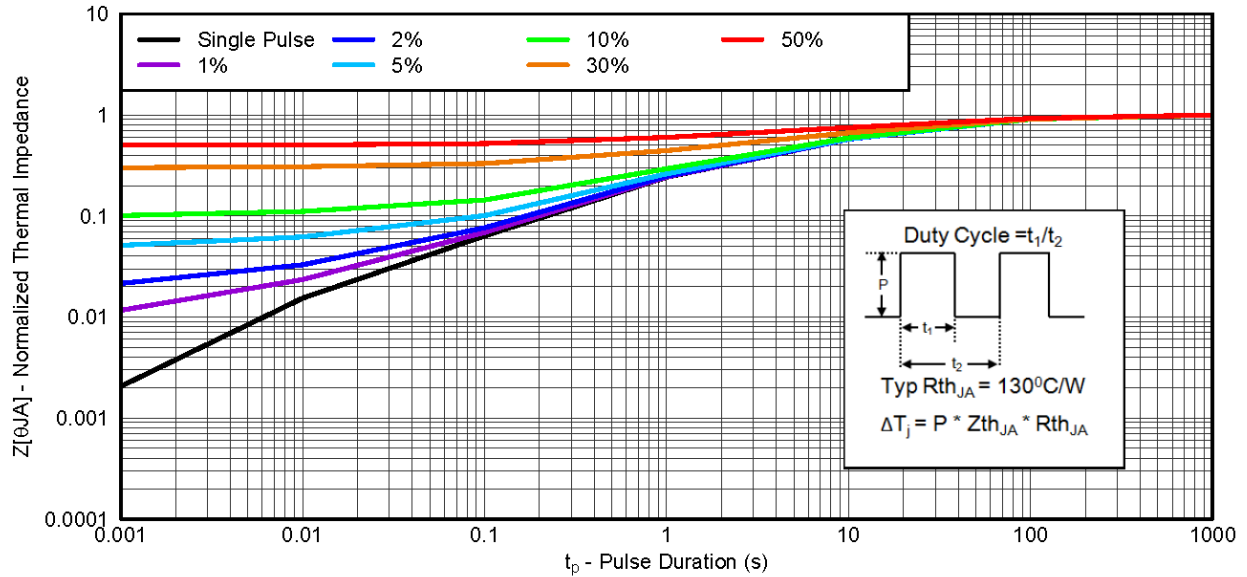


Max  $R_{\theta JA} = 165^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

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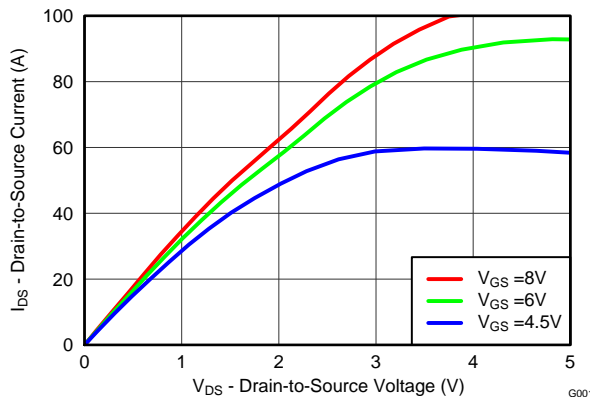
**TYPICAL MOSFET CHARACTERISTICS**

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



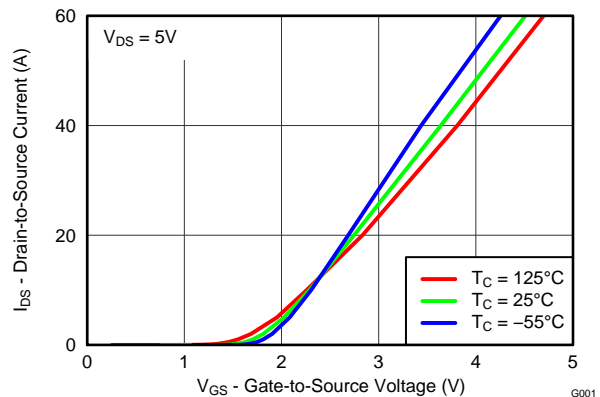
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Figure 1. Transient Thermal Impedance



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Figure 2. Saturation Characteristics

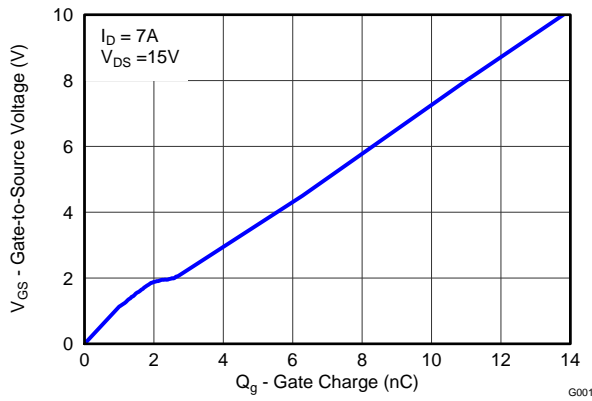


G001

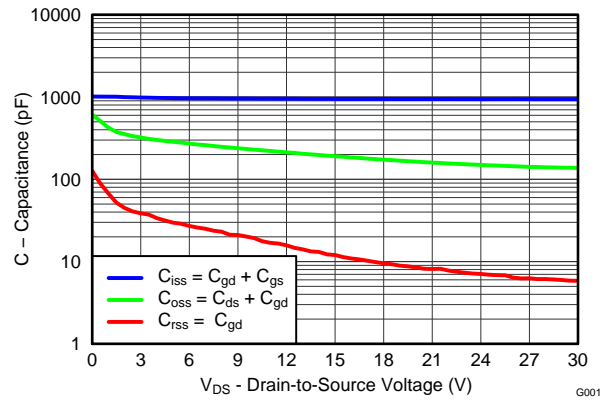
Figure 3. Transfer Characteristics

**TYPICAL MOSFET CHARACTERISTICS (continued)**

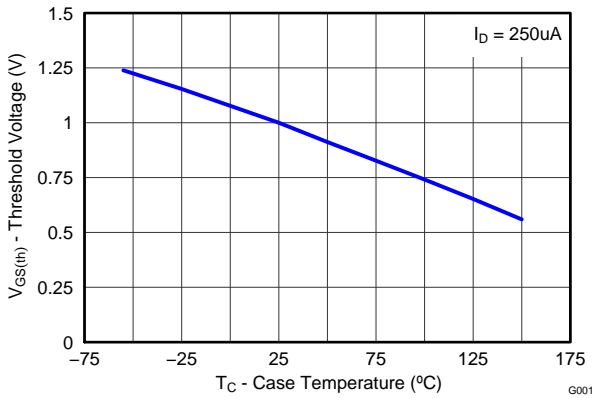
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



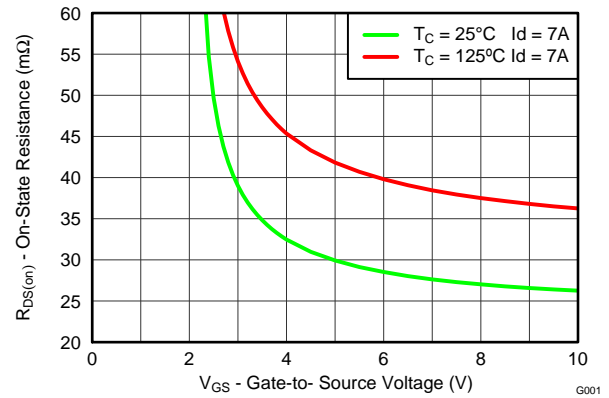
**Figure 4. Gate Charge**



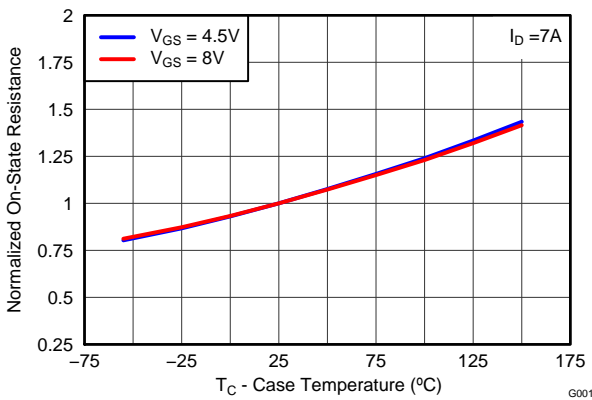
**Figure 5. Capacitance**



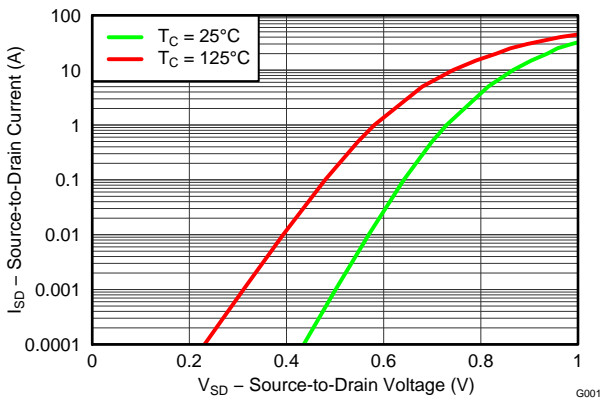
**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**



**Figure 8. Normalized On-State Resistance vs. Temperature**



**Figure 9. Typical Diode Forward Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

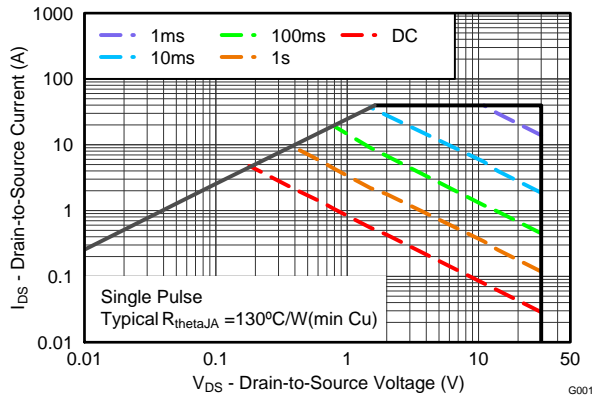


Figure 10. Maximum Safe Operating Area

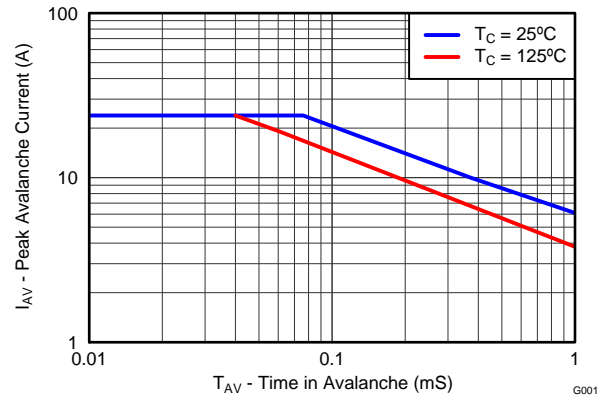


Figure 11. Single Pulse Unclamped Inductive Switching

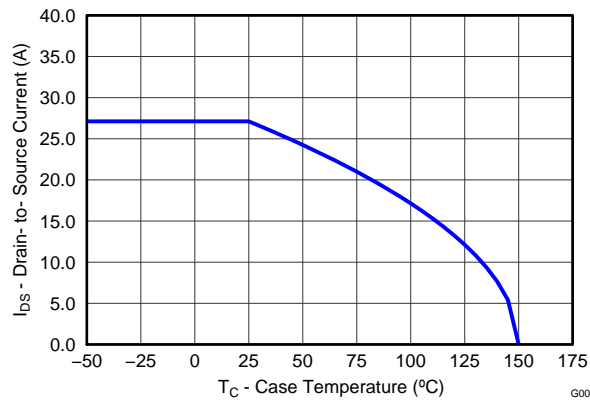
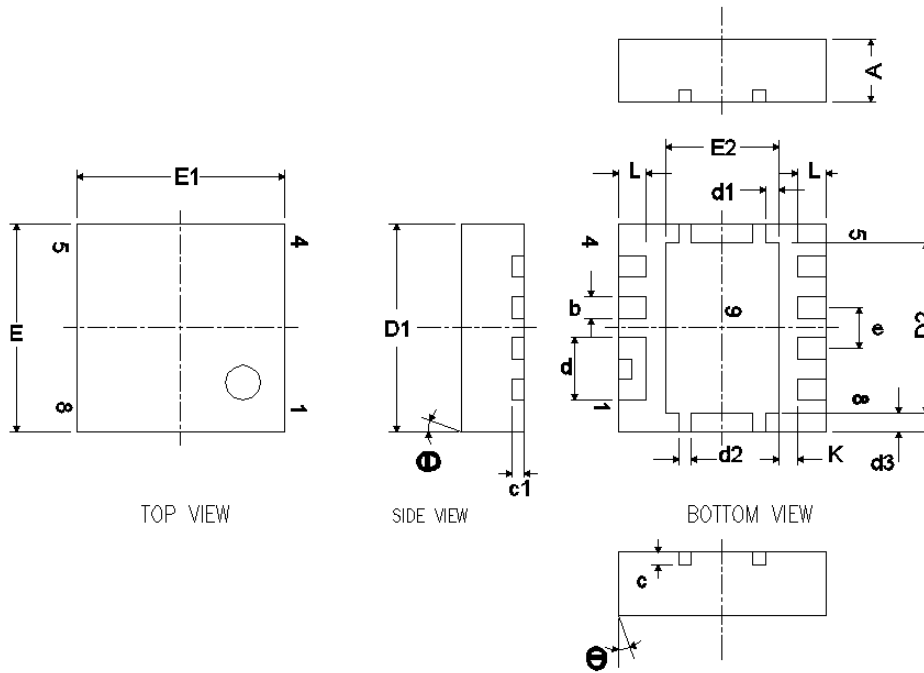


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q3E Package Dimensions

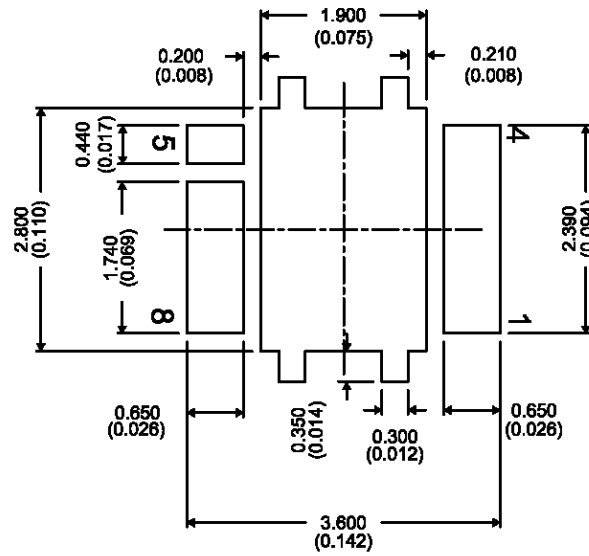


DIM	MILLIMETERS	
	MIN	MAX
A	0.850	1.050
b	0.280	0.400
c	0.150	0.250
c1	0.150	0.250
d	0.940	1.040
d1	0.160	0.260
d2	0.150	0.250
d3	0.250	0.350
D1	3.200	3.400
D2	2.650	2.750
E	3.200	3.400
E1	3.200	3.400
E2	1.750	1.850
e	0.650 TYP	
L	0.400	0.500
$\theta$	0°	-
K	0.300 Typ	

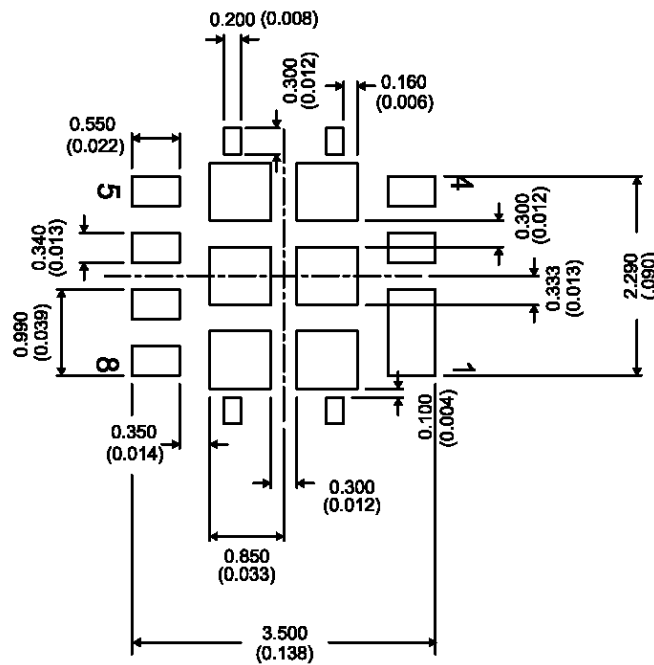
Notes:

1. Pin 1-4: Drain 1
2. Pin 5: Gate
3. Pin 6-8: Drain 2
4. Pin 9: Source

### Recommended PCB Pattern

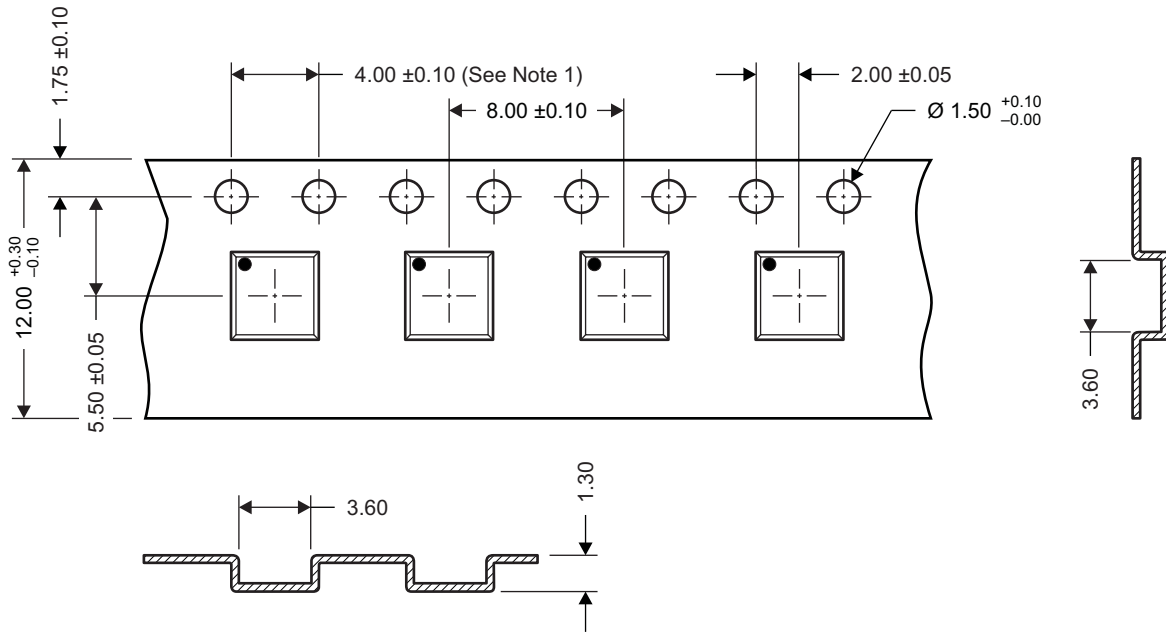


### Recommended Stencil Opening



For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

**Q3E Tape and Reel Information**



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**Notes:**

1. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness:  $0.30 \pm 0.05$ mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87312Q3E	ACTIVE	VSON-CLIP	DPB	8	2500	RoHS-Exempt & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87312E	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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