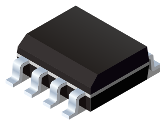


CSD88539ND，双路 60V N 通道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 雪崩额定值
- 无铅
- 符合 RoHS 环保标准
- 无卤素

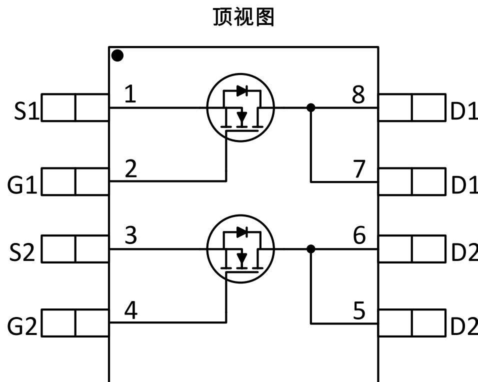
2 应用范围

- 用于电机控制的半桥
- 同步降压转换器

3 说明

这款双路小外形尺寸 (SO)-8，60V，23mΩ NexFET™ 功率 MOSFET 被设计运行为低电流电机控制应用中的半桥。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	60		V
Q_g	栅极电荷总量 (10V)	7.2		nC
Q_{gd}	栅漏栅极电荷	1.1		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	27	mΩ
		V_{GS} = 10V	23	mΩ
$V_{GS(th)}$	阀值电压	3.0		V

订购信息

器件	数量	介质	封装	出货
CSD88539ND	2500	13 英寸卷带	SO-8 塑料封装	卷带封装
CSD88539NDT	250	7 英寸卷带		

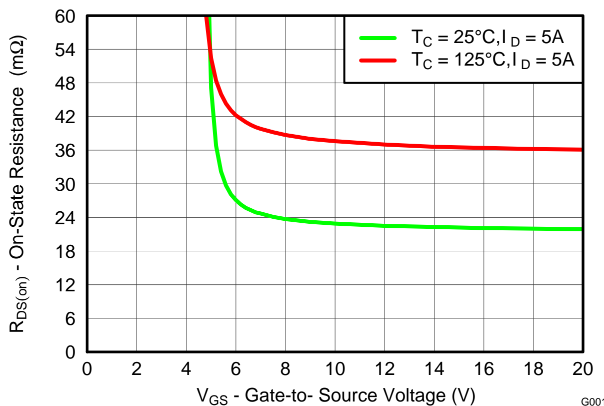
最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	60	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	15	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	11.7	
	持续漏极电流(1)	6.3	
I_{DM}	脉冲漏极电流 (2)	46	A
P_D	功率耗散(1)	2.1	W
T_J，T_{STG}	运行结温和储存温度范围	-55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 22A，L = 0.1mH，R_G = 25Ω	24	mJ

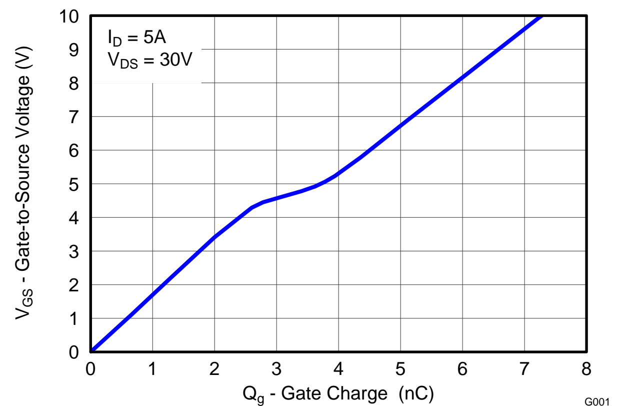
(1) $R_{\theta JA}$ = 60°C/W，这是在一个厚度 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司 的铜过渡垫片上测得的典型值

(2) 脉冲持续时间 ≤ 300μs，占空比 ≤ 2%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 μA	60			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 48 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.6	3.0	3.6	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V, I_D = 5 A		27	34	mΩ
		V_{GS} = 10 V, I_D = 5 A		23	28	mΩ
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 5 A		19		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		570	741	pF
C_{oss}	Output Capacitance			70	91	pF
C_{rss}	Reverse Transfer Capacitance			2.0	2.6	pF
R_G	Series Gate Resistance			6.6	13.2	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 30 V, I_D = 5 A		7.2	9.4	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			2.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.8		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		9.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 5 A, R_G = 0 Ω		5		ns
t_r	Rise Time			9		ns
$t_{d(off)}$	Turn Off Delay Time			14		ns
t_f	Fall Time			4		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD} = 5 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30 V, I_F = 5A, di/dt = 300A/μs		37		nC
t_{rr}	Reverse Recovery Time			21		ns

4.2 Thermal Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{θJL}$	Junction-to-Lead Thermal Resistance(1)			20	°C/W
$R_{θJA}$	Junction-to-Ambient Thermal Resistance(1)(2)			75	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

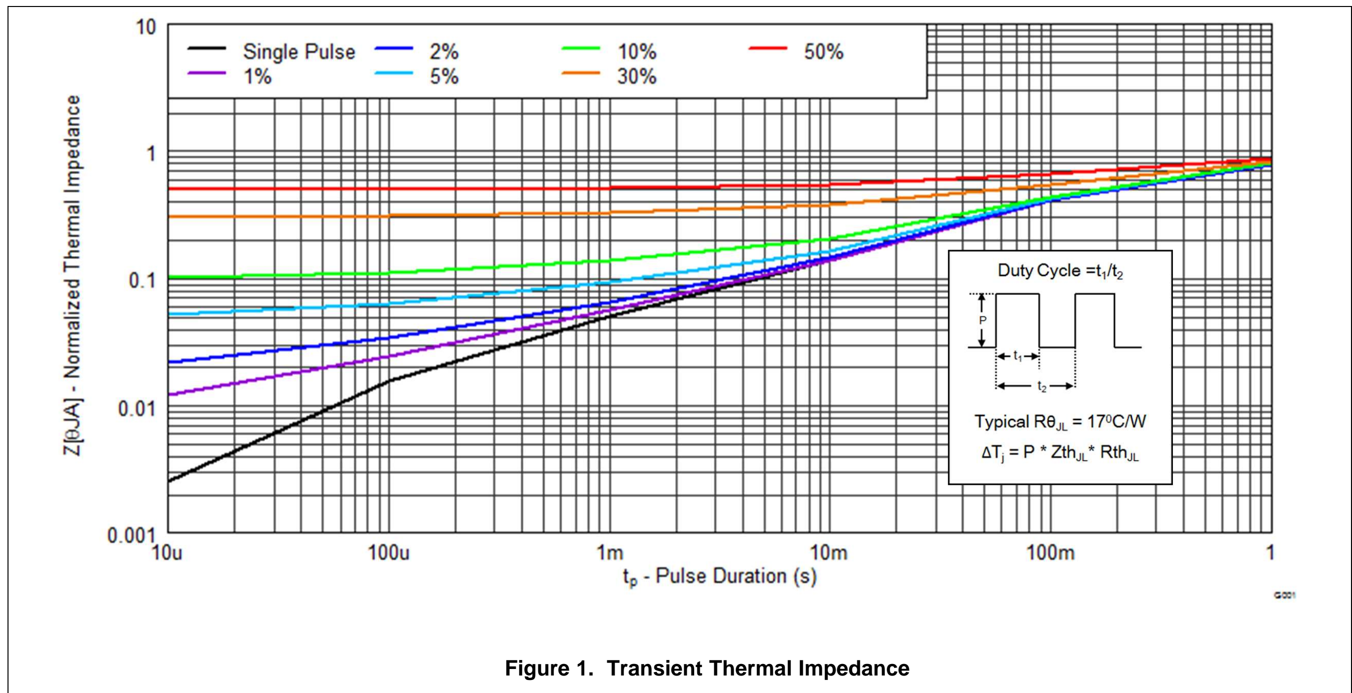

Figure 1. Transient Thermal Impedance

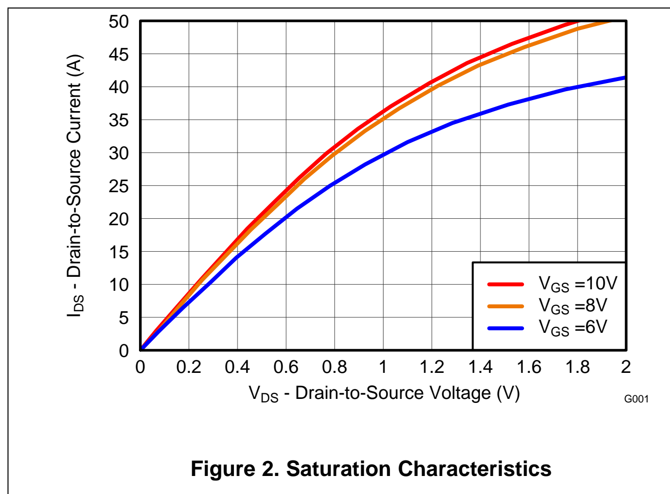

Figure 2. Saturation Characteristics

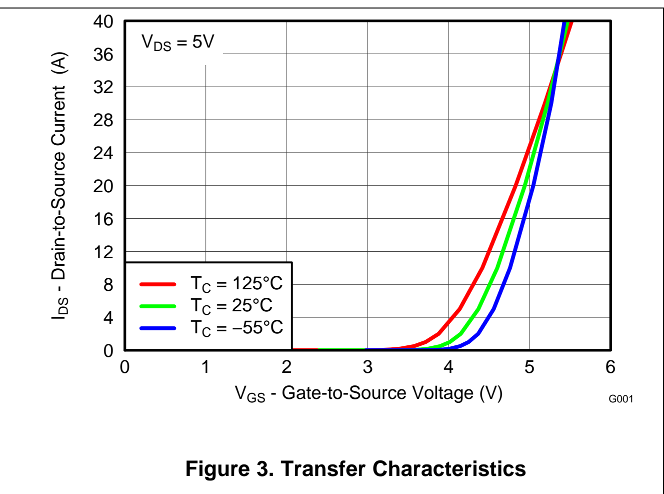

Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

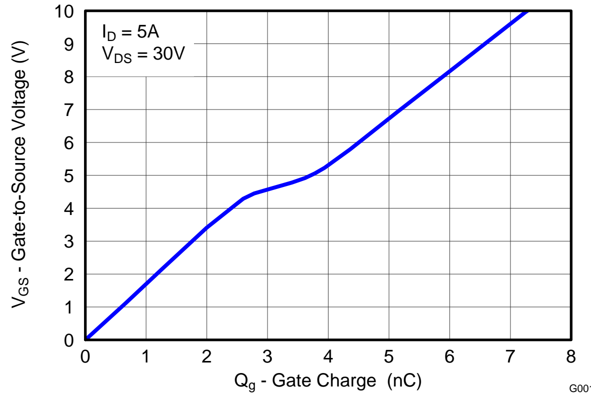

Figure 4. Gate Charge

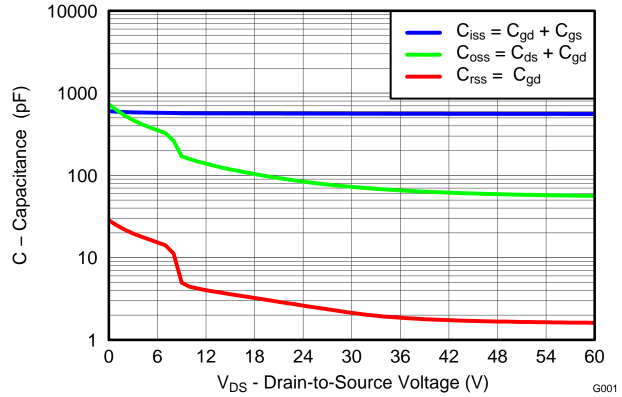

Figure 5. Capacitance

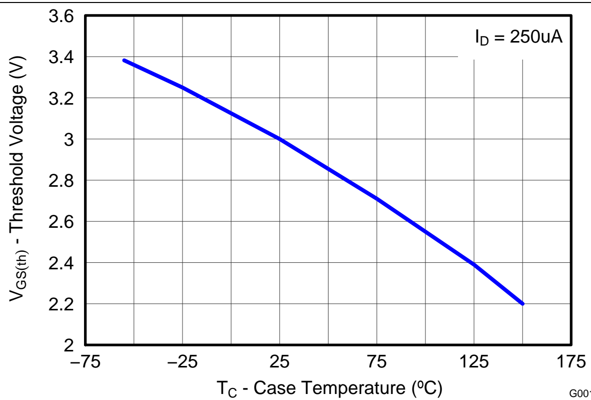

Figure 6. Threshold Voltage vs Temperature

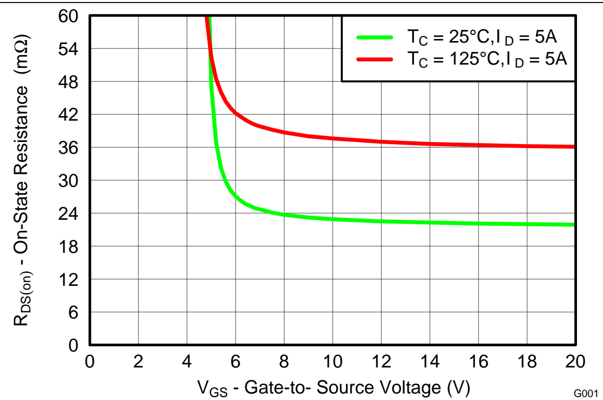

Figure 7. On-State Resistance vs Gate-to-Source Voltage

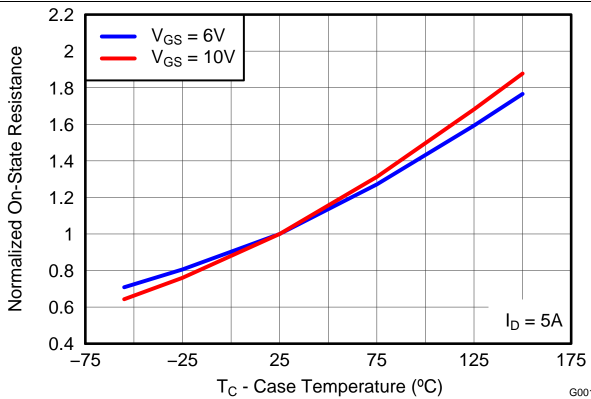

Figure 8. Normalized On-State Resistance vs Temperature

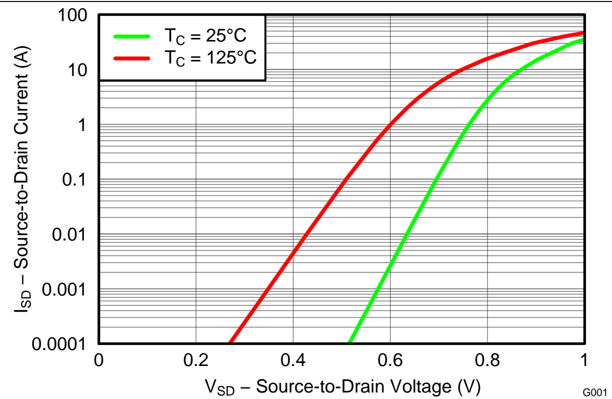

Figure 9. Typical Diode Forward Voltage

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Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

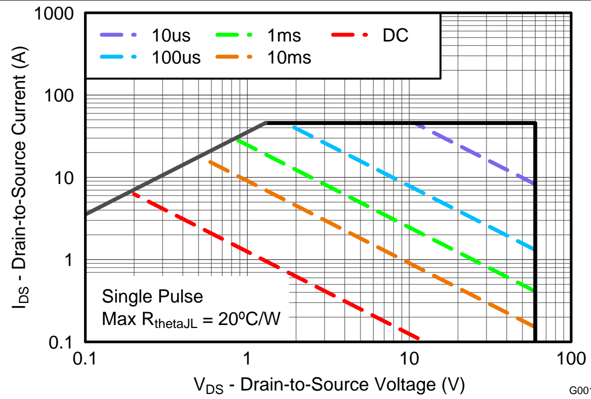


Figure 10. Maximum Safe Operating Area

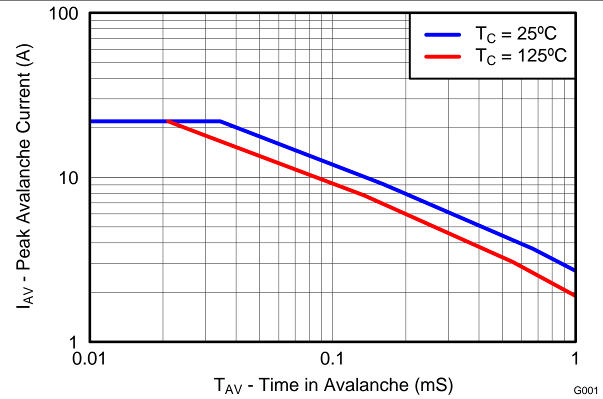


Figure 11. Single Pulse Unclamped Inductive Switching

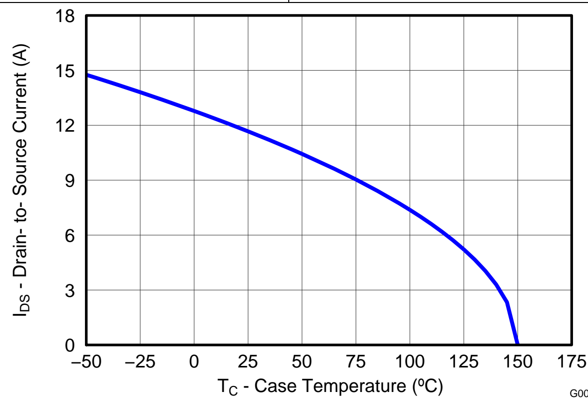
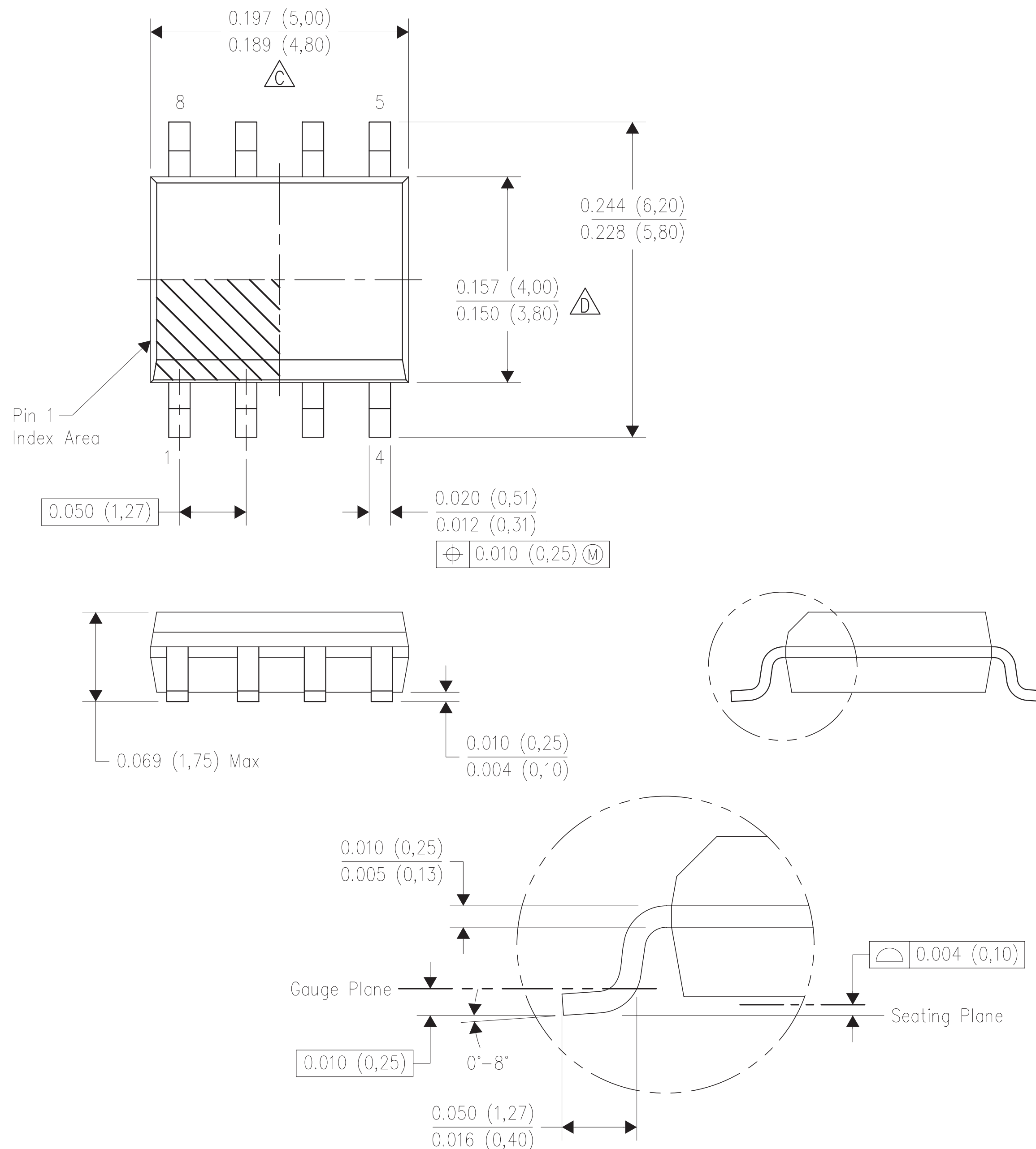


Figure 12. Maximum Drain Current vs Temperature

5 Mechanical Data

5.1 SO-8 Package Dimensions



1. All linear dimensions are in inches (millimeters).
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
4. Body width does not include interlead flash. Interlead flas shall not exceed 0.017 (0,43) each side.
5. Reference JEDEC MS-012 variation AA.

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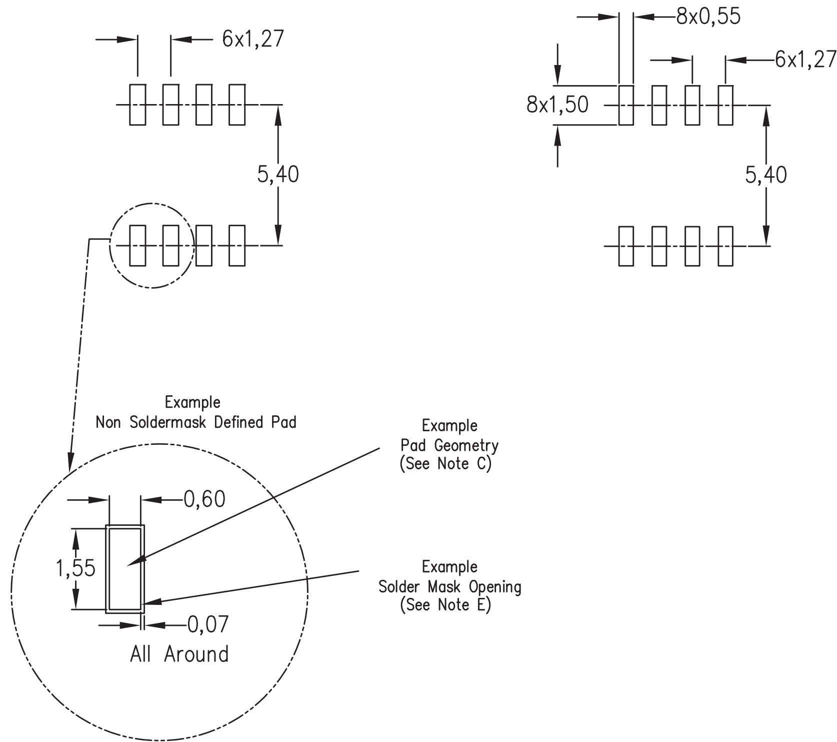
5.2 Recommended PCB Pattern and Stencil Opening



1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Publication IPC-7351 is recommended for alternate designs.
4. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
5. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD88539ND	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N	Samples
CSD88539NDT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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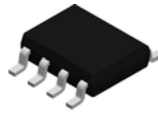


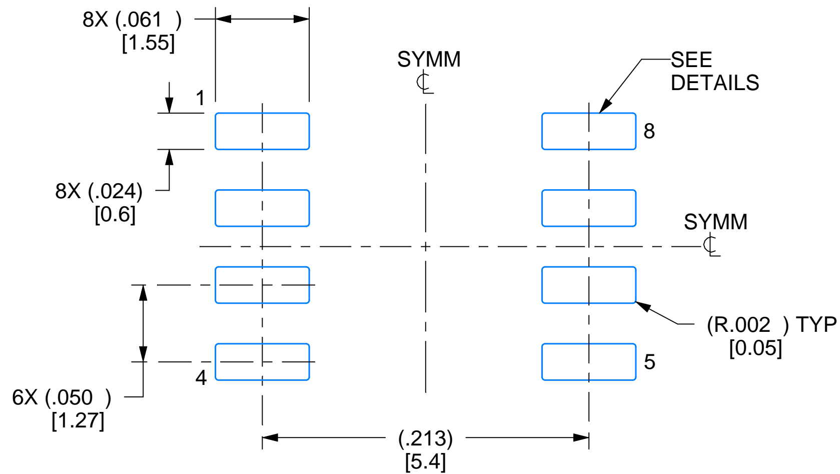
PACKAGE OUTLINE

SOIC - 1.75 mm max height

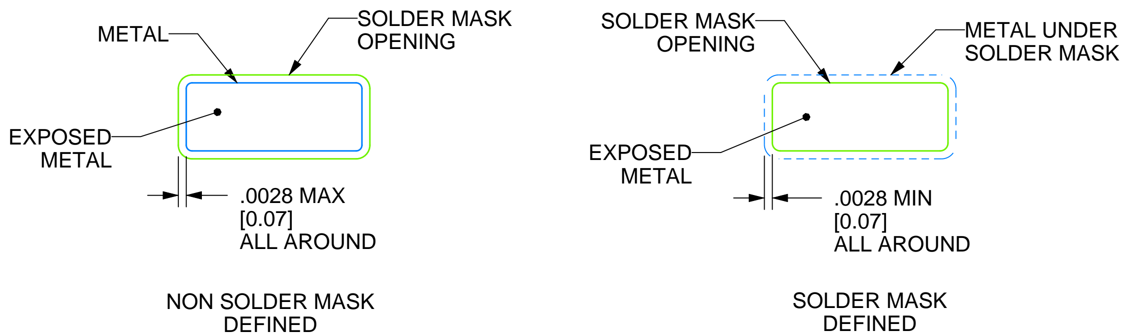
SMALL OUTLINE INTEGRATED CIRCUIT

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

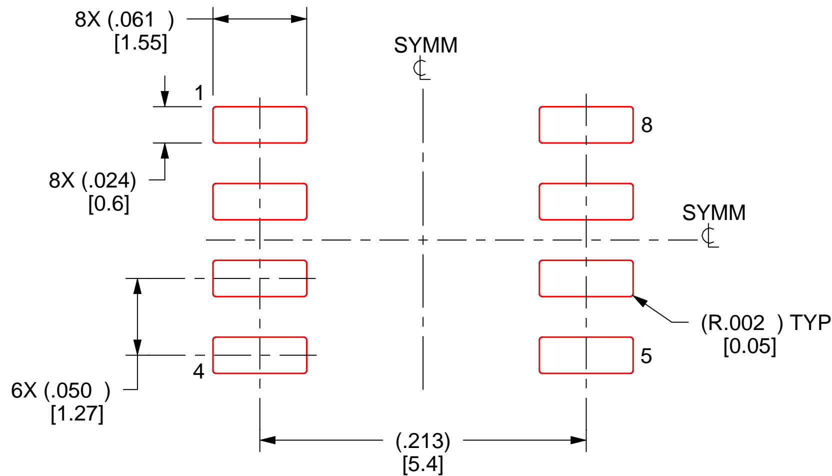


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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