DS92LV16 16-Bit Bus LVDS Serializer/Deserializer - 25 - 80 MHz

Check for Samples: DS92LV16

FEATURES

- **25–80 MHz 16:1/1:16 Serializer/Deserializer (2.56Gbps Full Duplex Throughput)**
- **Independent Transmitter and Receiver Operation With Separate Clock, Enable, Power Down Pins**
- **Hot Plug Protection (Power Up High Impedance) and Synchronization (Receiver Locks To Random Data)**
- **Wide +/−5% Reference Clock Frequency Tolerance for Easy System Design Using Locally-Generated Clocks**
- **Line and Local Loopback Modes**
- **Robust BLVDS Serial Transmission Across Backplanes and Cables for Low EMI**
- **No External Coding Required**
- **Internal PLL, No External PLL Components Required**
- **Single +3.3V Power Supply**
- **Low Power: 104mA (typ) Transmitter, 119mA (typ) Receiver at 80MHz**
- **±100mV Receiver Input Threshold**
- **Loss of Lock Detection and Reporting Pin**
- **Industrial −40 to +85°C Temperature Range**
- **>2.5kV HBM ESD**
- **Compact, Standard 80-Pin LQFP Package**

DESCRIPTION

The DS92LV16 Serializer/Deserializer (SERDES) pair transparently translates a 16–bit parallel bus into a BLVDS serial stream with embedded clock information. This single serial stream simplifies transferring a 16-bit, or less bus over PCB traces and cables by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

This SERDES pair includes built-in system and device test capability. The line loopback and local loopback features provide the following functionality: the local loopback enables the user to check the integrity of the transceiver from the local parallel-bus side and the system can check the integrity of the data transmission line by enabling the line loopback.

The DS92LV16 incorporates BLVDS signaling on the high-speed I/O. BLVDS provides a low power and low noise environment for reliably transferring data over a serial transmission path. The equal and opposite currents through the differential data path control EMI by coupling the resulting fringing fields together.

Block Diagram

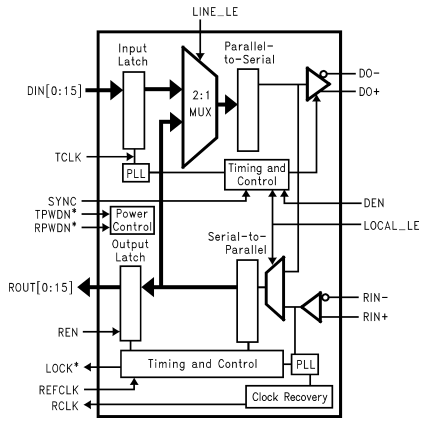

Figure 1. DS92LV16

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS/LVTTL Input Voltage	−0.3V to (V_{CC} +0.3V)
LVCMOS/LVTTL Output Voltage	−0.3V to (V_{CC} +0.3V)
Bus LVDS Receiver Input Voltage	−0.3V to +3.9V
Bus LVDS Driver Output Voltage	−0.3V to +3.9V
Bus LVDS Output Short Circuit Duration	10ms
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	+260°C
Maximum Package Power Dissipation Capacity Package Derating:	23.2 mW/°C above
LQFP	+25°C
θ_{JA}	43°C/W
θ_{JC}	11.1°C/W
ESD Rating (HBM)	>2.5kV

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of ELECTRICAL CHARACTERISTICS specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.15	3.3	3.45	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Clock Rate	25		80	MHz

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ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
LVCMOS/LVTTL DC Specifications							
V_{IH}	High Level Input Voltage		TCLK_R/$\overline{F}$,DEN, TCLK, $\overline{TPWDN}$, DIN, SYNC, RCLK_R/$\overline{F}$, REN, $\overline{REFCLK}$, $\overline{PWRDN}$	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			-0.7	−1.5	V
I_{IN}	Input Current	V_{IN} = 0V or 3.6V		−10	±2	+10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −9 mA	R_{OUT}, RCLK, LOCK	2.3	3.0	V_{CC}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 9 mA		GND	0.33	0.5	V
I_{OS}	Output Short Circuit Current	VOUT = 0V		−15	−48	−85	mA
I_{OZ}	TRI-STATE Output Current	$\overline{PWRDN}$ or REN = 0.8V, V_{OUT} = 0V or VCC	R_{OUT}, RCLK,	−10	±0.4	+10	µA
Bus LVDS DC specifications							
VTH	Differential Threshold High Voltage	VCM = +1.1V	RI+, RI-			+100	mV
VTL	Differential Threshold Low Voltage			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V or 0V		−10	±5	+10	µA
		V_{IN} = 0V, V_{CC} = 3.6V or 0V		−10	±5	+10	µA
V_{OD}	Output Differential Voltage (DO+) - (DO-)	RL = 100Ω, See Figure 18	DO+, DO-	350	500	550	mV
ΔV_{OD}	Output Differential Voltage Unbalance				2	15	mV
V_{OS}	Offset Voltage			1.05	1.2	1.25	V
ΔV_{OS}	Offset Voltage Unbalance				2.7	15	mV
I_{OS}	Output Short Circuit Current	DO = 0V, Din = H, $\overline{TXPWDN}$ and DEN = 2.4V		-35	-50	-70	mA
I_{OZ}	Tri-State Output Current	$\overline{TXPWDN}$ or DEN = 0.8V, DO = 0V OR VDD		-10	± 1	10	µA
I_{OX}	Power-Off Output Current	VDD = 0V, DO = 0V or 3.6V		-10	± 1	10	µA
SER/DES SUPPLY CURRENT (DVDD, PVDD and AVDD pins)							
I_{CCT}	Total Supply Current (includes load current)	C_L = 15 pF, R_L = 100 Ω	f = 80 MHz, PRBS15 pattern		209		mA
		C_L = 15 pF, R_L = 100 Ω	f = 80 MHz, Worse case pattern (Checker-board pattern)		225	320	mA
I_{CCX}	Supply Current Powerdown	$\overline{PWRDN}$ = 0.8V, REN = 0.8V			0.35	1.0	mA

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SERIALIZER TIMING REQUIREMENTS FOR TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TCP}	Transmit Clock Period		12.5	T	40	ns
t_{TCIH}	Transmit Clock High Time		0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit Clock Low Time		0.4T	0.5T	0.6T	ns
t_{CLKT}	TCLK Input Transition Time			3	6	ns
t_{JIT}	TCLK Input Jitter				80	ps (rms)

SERIALIZER SWITCHING CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LLHT}	Bus LVDS Low-to-High Transition Time	R_L = 100Ω See Figure 4 C_L=10pF to GND		0.2	0.4	ns
t_{LHLT}	Bus LVDS High-to-Low Transition Time			0.2	0.4	ns
t_{DIS}	DIN (0-15) Setup to TCLK	R_L = 100Ω See Figure 7 C_L=10pF to GND	2.4			ns
t_{DIH}	DIN (0-15) Hold from TCLK		0			ns
t_{HZD}	DO ± HIGH to TRI-STATE Delay	R_L = 100Ω See Figure 8(1) C_L=10pF to GND		2.3	10	ns
t_{LZD}	DO ± LOW to TRI-STATE Delay			1.9	10	ns
t_{ZHD}	DO ± TRI-STATE to HIGH Delay			1.0	10	ns
t_{ZLD}	DO ± TRI-STATE to LOW Delay			1.0	10	ns
t_{SPW}	SYNC Pulse Width	R_L = 100Ω See Figure 9	$5*t_{TCP}$		$6*t_{TCP}$	ns
t_{PLD}	Serializer PLL Lock Time		$510*t_{TCP}$		$513*t_{TCP}$	ns
t_{SD}	Serializer Delay	R_L = 100Ω See Figure 10	t_{TCP} + 1.0	t_{TCP} + 2.0	t_{TCP} + 4.0	ns
t_{RJIT}	Random Jitter			10		ps (rms)
t_{DJIT}	Deterministic Jitter See Figure 16	35 MHz	-240		140	ps
		80 MHz	-75		100	ps

(1) Due to TRI-STATE of the Serializer, the Deserializer will lose PLL lock and have to resynchronize before data transfer.

DESERIALIZER TIMING REQUIREMENTS FOR REFCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RFCP}	REFCLK Period		12.5	T	40	ns
t_{RFDC}	REFCLK Duty Cycle		40	50	60	%
t_{RFCP} / t_{TCP}	Ratio of REFCLK to TCLK		0.95		1.05	
t_{RFTT}	REFCLK Transition Time				6	ns

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DESERIALIZER SWITCHING CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{RCP}	Receiver out Clock Period	$t_{RCP} = t_{TCP}$ See Figure 10	RCLK	12.5		40	ns
t_{RDC}	RCLK Duty Cycle		RCLK	45	50	55	%
t_{CLH}	CMOS/TTL Low-to-High Transition Time	CL = 15 pF See Figure 5	Rout(0-9), $\overline{LOCK}$, RCLK		2	4	ns
t_{CHL}	CMOS/TTL High-to-Low Transition Time				2	4	ns
t_{ROS}	ROUT (0-9) Setup Data to RCLK	See Figure 12		$0.35*t_{RCP}$	$0.5*t_{RCP}$		ns
t_{ROH}	ROUT (0-9) Hold Data to RCLK			$-0.35*t_{RCP}$	$-0.5*t_{RCP}$		ns
t_{HZR}	HIGH to TRI-STATE Delay	See Figure 13	Rout(0-9), $\overline{LOCK}$		2.2	10	ns
t_{LZR}	LOW to TRI-STATE Delay				2.2	10	ns
t_{ZHR}	TRI-STATE to HIGH Delay				2.3	10	ns
t_{ZLR}	TRI-STATE to LOW Delay				2.9	10	ns
t_{DD}	Deserializer Delay		RCLK	$1.75*t_{RCP} + 2$	$1.75*t_{RCP} + 5$	$1.75*t_{RCP} + 7$	ns
t_{DSR1}	Deserializer PLL Lock Time from PWRDWN (with SYNCPAT)	See (1)	35MHz		3.7	10	µs
			80 MHz		1.9	4	µs
t_{DSR2}	Deserializer PLL Lock time from SYNCPAT		35MHz		1.5	5	µs
			80 MHz		0.9	2	µs
t_{RNMI-R}	Ideal Deserializer Noise Margin Right	See Figure 17 (2)	35 MHz			+630	ps
			80 MHz			+230	ps
t_{RNMI-L}	Ideal Deserializer Noise Margin Left	See Figure 17 (2)	35 MHz	−630			ps
			80 MHz	−230			ps

(1) Sync pattern is a fixed pattern with 8-bit of data high followed by 8-bit of data low.
(2) tRNMI is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. It is a measurement in reference with the ideal bit position, please see TI's AN-1217(SNLA053) for detail.

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AC TIMING DIAGRAMS AND TEST CIRCUITS

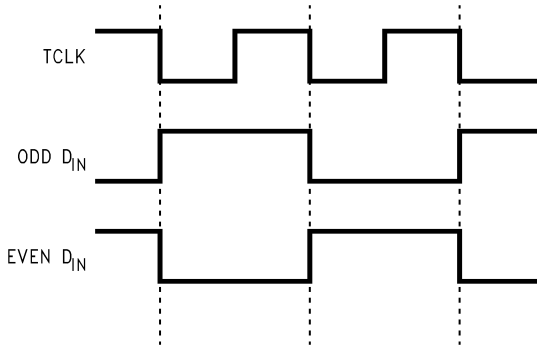

Figure 2. "Worst Case" Serializer ICC Test Pattern

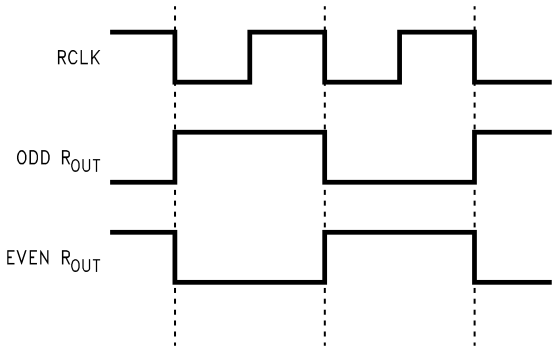

Figure 3. "Worst Case" Deserializer ICC Test Pattern

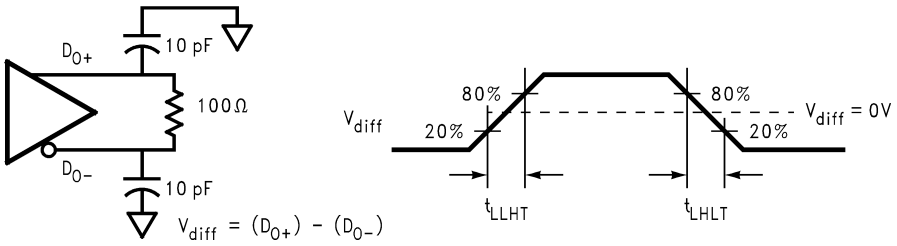

Figure 4. Serializer Bus LVDS Output Load and Transition Times

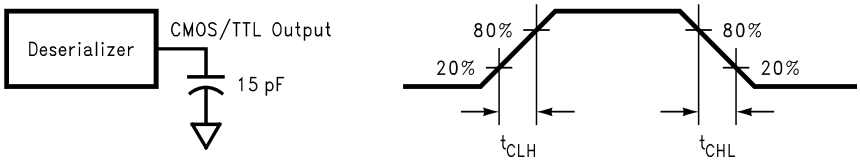

Figure 5. Deserializer CMOS/TTL Output Load and Transition Times

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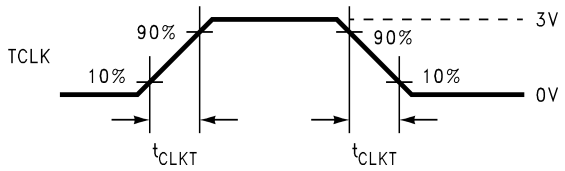

Figure 6. Serializer Input Clock Transition Time

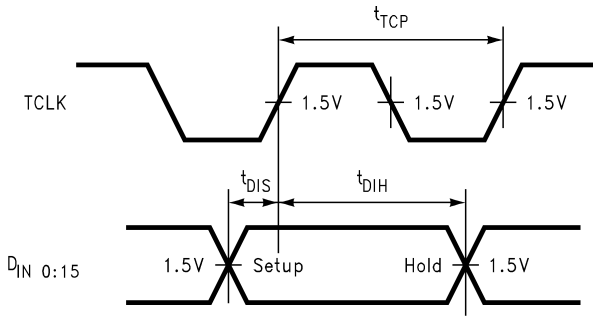

Figure 7. Serializer Setup/Hold Times

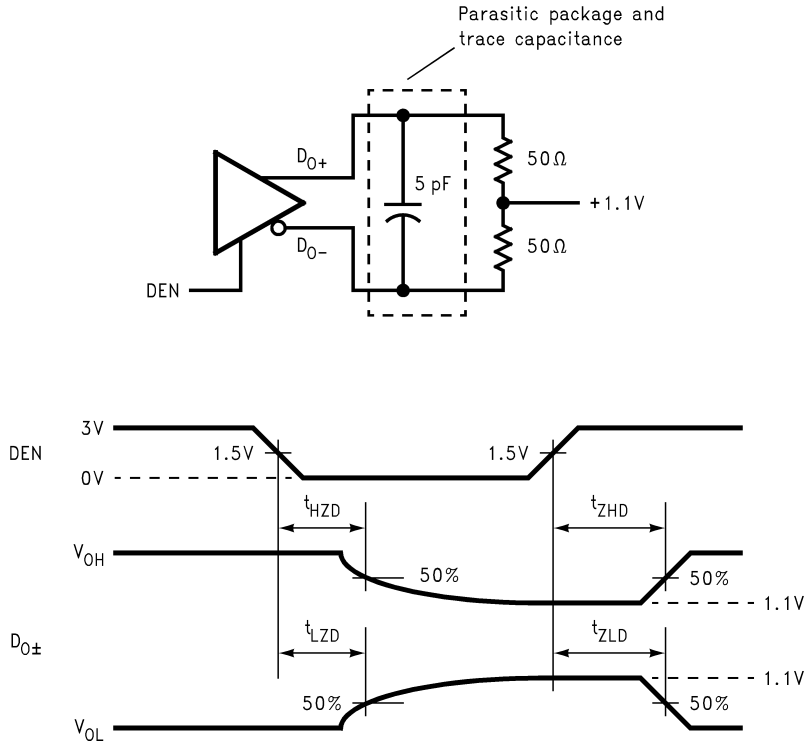

Figure 8. Serializer TRI-STATE Test Circuit and Timing

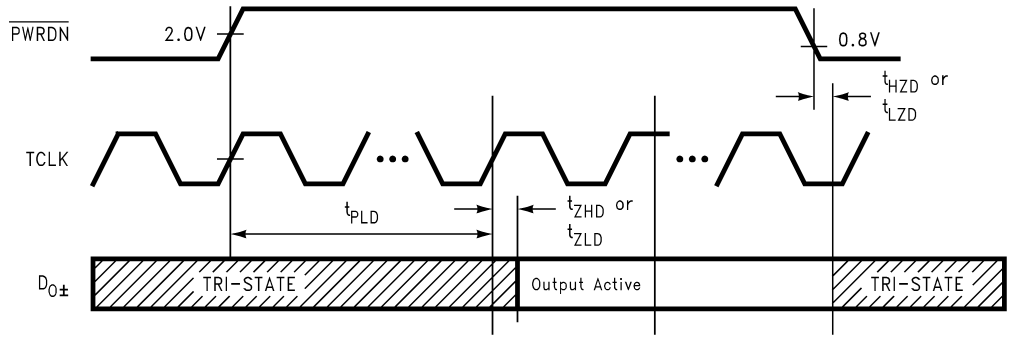

Figure 9. Serializer PLL Lock Time, SYNC Timing and $\overline{\text{PWRDN}}$ TRI-STATE Delays

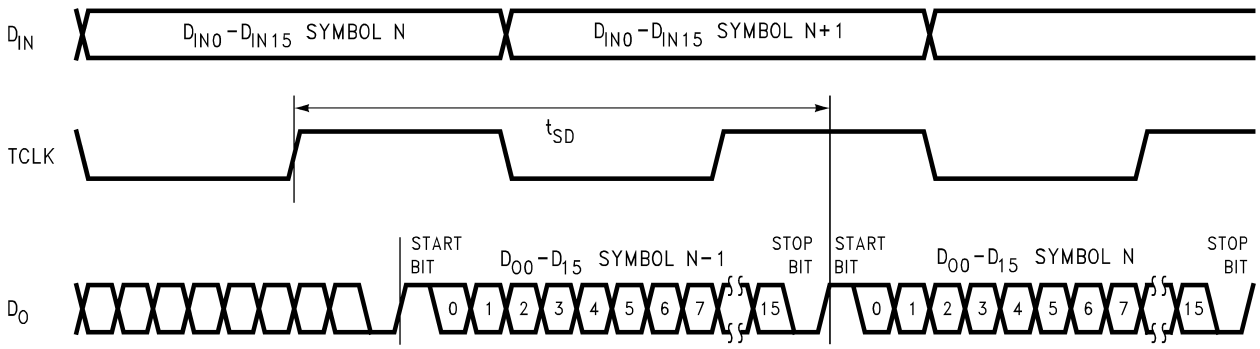

Figure 10. Serializer Delay

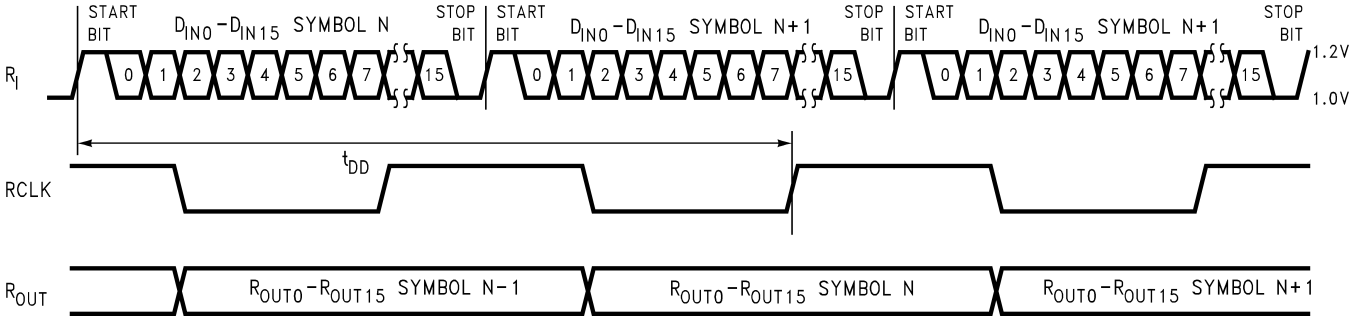

Figure 11. Deserializer Delay

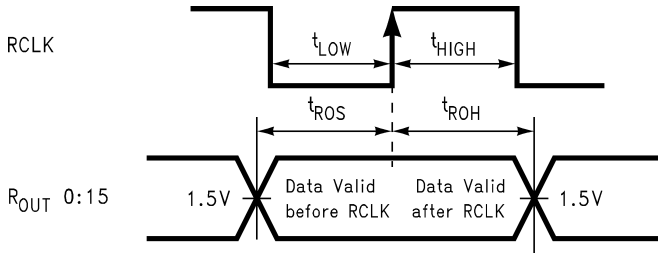

Figure 12. Deserializer Setup and Hold Times

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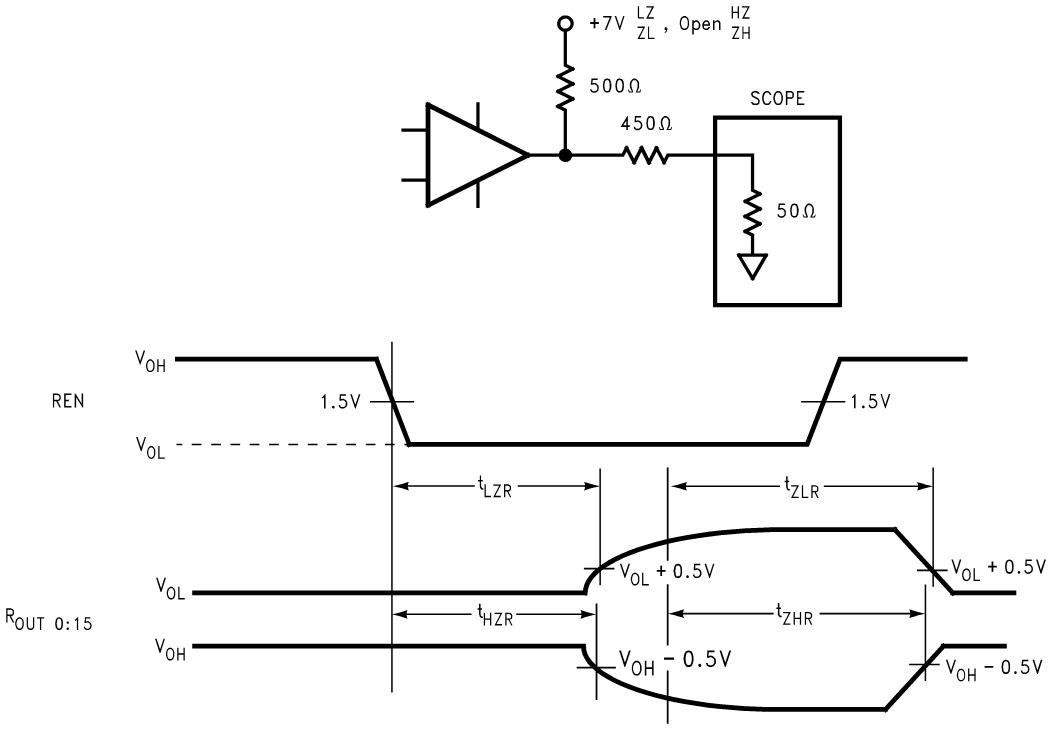

Figure 13. Deserializer TRI-STATE Test Circuit and Timing

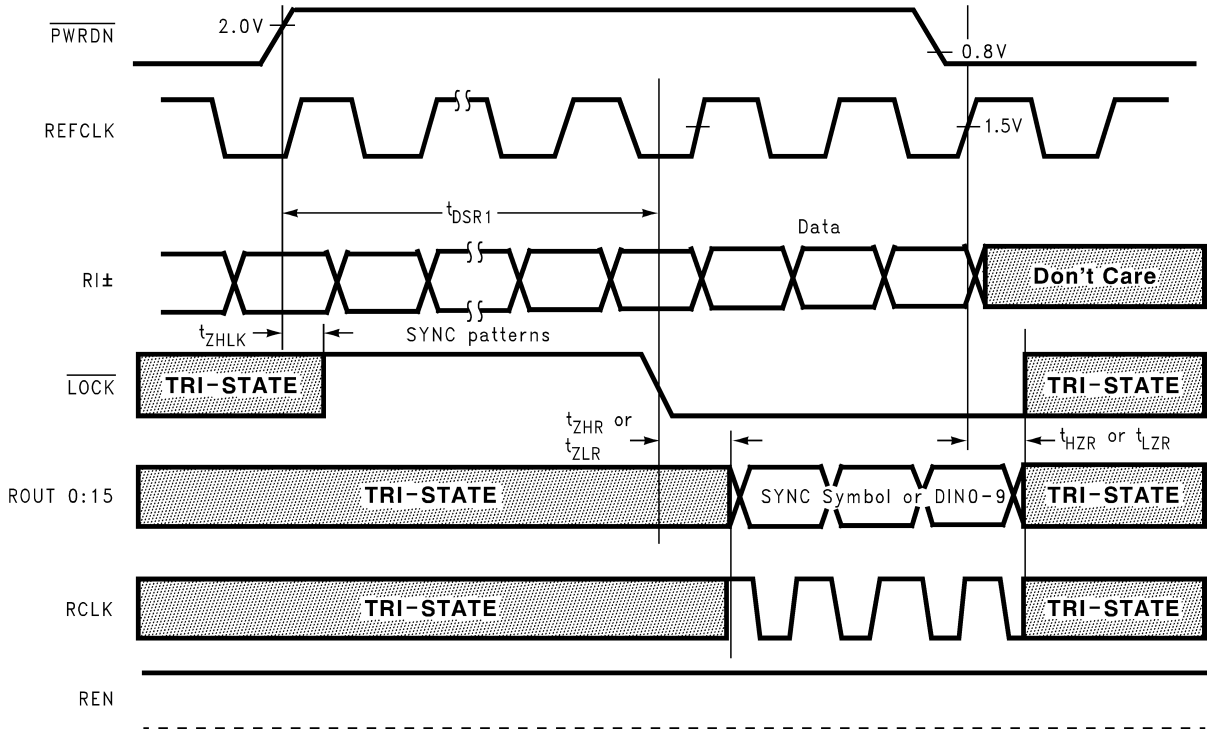

Figure 14. Deserializer PLL Lock Times and $\overline{\text{PWRDN}}$ TRI-STATE Delays

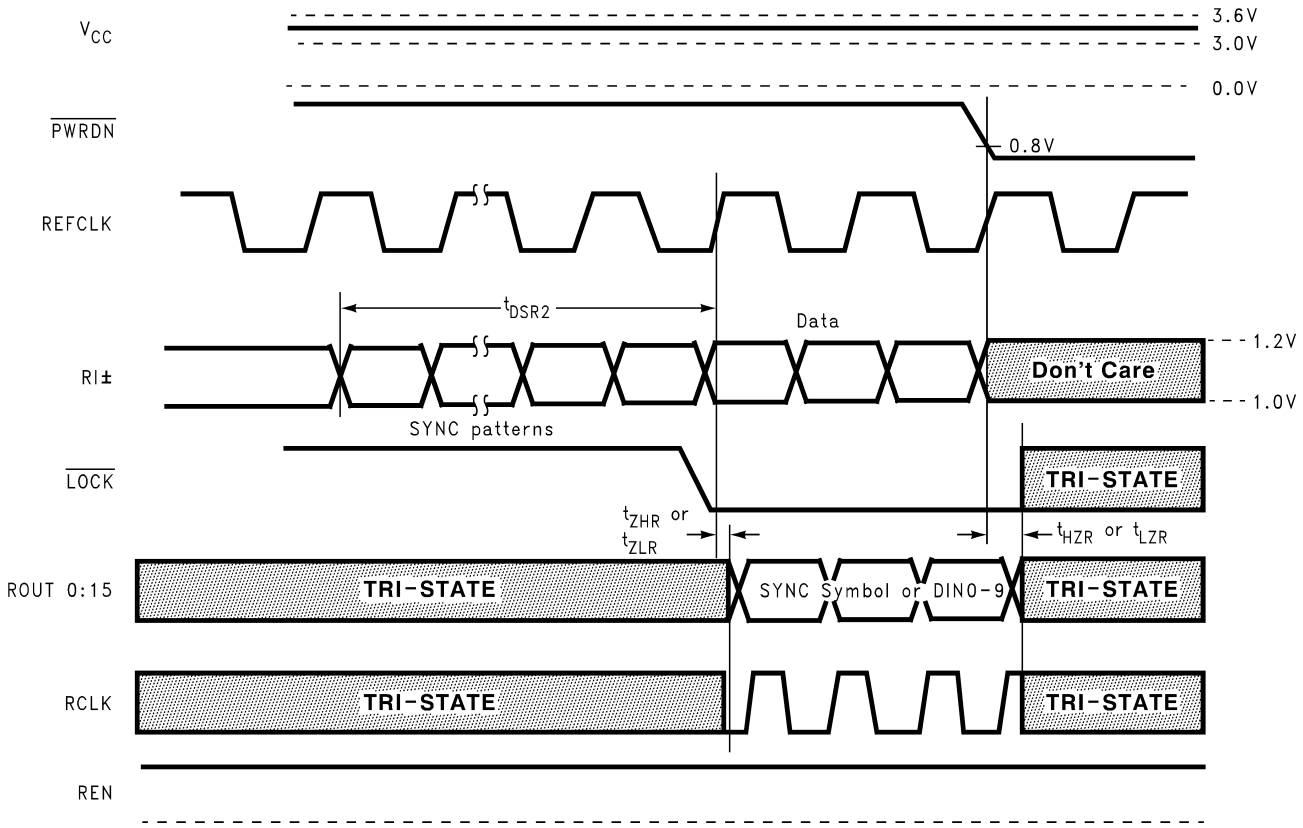

Figure 15. Deserializer PLL Lock Time from SyncPAT

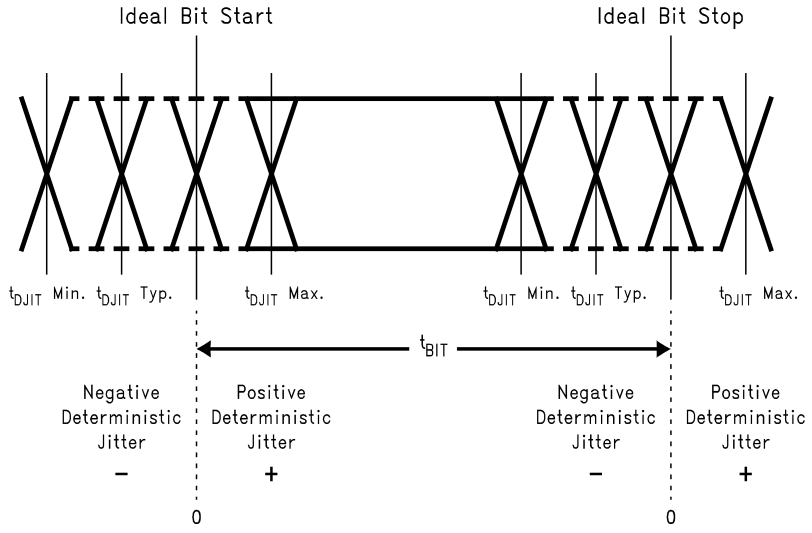

Figure 16. Deterministic Jitter and Ideal Bit Position

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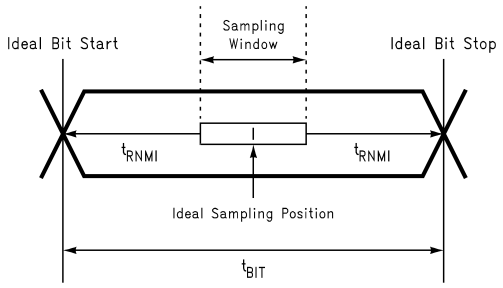
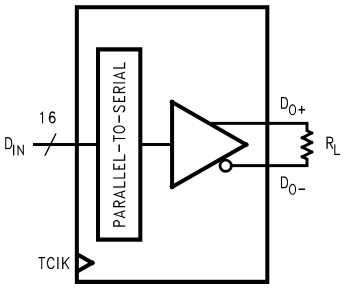


$$\text{Ideal Sampling Position} = \frac{(t_{BIT})}{2}$$

t_{RNMI-L} is the noise margin on the left of the above figure. It is a negative value to indicate early with respect to ideal.
t_{RNMI-R} is the noise margin on the right of the above figure. It is a positive value to indicate late with respect to ideal.

Figure 17. Deserializer Noise Margin (t_{RNMI}) and Sampling window



V_{OD} = (DO^+)–(DO^-).
Differential output signal is shown as (DO+)–(DO−), device in Data Transfer mode.

Figure 18. V_{OD} Diagram

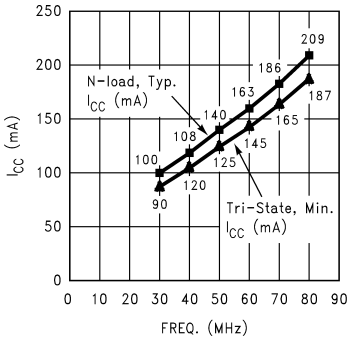


Figure 19. Icc vs Freq

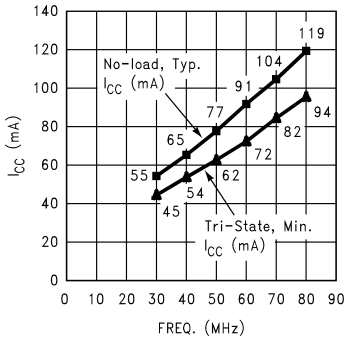


Figure 20. Icc vs Freq (Rx only)

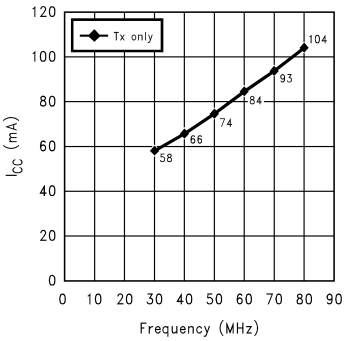


Figure 21. Icc vs Freq (Tx only)

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FUNCTIONAL DESCRIPTION

The DS92LV16 combines a serializer and deserializer onto a single chip. The serializer accepts a 16-bit LVCMOS or LVTTL data bus and transforms it into a BLVDS serial data stream with embedded clock information. The deserializer then recovers the clock and data to deliver the resulting 16-bit wide words to the output.

The device has a separate Transmit block and Receive block that can operate independent of each other. Each has a power down control to enable efficient operation in various applications. For example, the transceiver can operate as a standby in a redundant data path but still conserve power. The part can be configured as a Serializer, Deserializer, or as a Full Duplex SER/DES.

The DS92LV16 serializer and deserializer blocks each has three operating states. They are the Initialization, Data Transfer, and Resynchronization states. In addition, there are two passive states: Powerdown and TRI-STATE.

The following sections describe each operation mode and passive state.

INITIALIZATION

Before the DS92LV16 sends or receives data, it must initialize the links to and from another DS92LV16. Initialization refers to synchronizing the Serializer's and Deserializer's PLL's to local clocks. The local clocks must be the same frequency or within a specified range if from different sources. After the Serializers synchronizes to the local clocks, the Deserializers synchronize to the Serializers as the second and final initialization step.

Step 1: When V_{CC} is applied to both Serializer and/or Deserializer, the respective outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When V_{CC} reaches V_{CC} OK (2.2V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock, TCLK. For the Deserializer, the local clock is applied to the REFCLK pin. A local on-board oscillator or other source provides the specified clock input to the TCLK and REFCLK pin.

The Serializer outputs are held in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer block is now ready to send data or synchronization patterns. If the SYNC pin is high, then the Serializer block generates and sends the synchronization patterns (sync-pattern).

The Deserializer output will remain TRI-STATE while its PLL locks to the REFCLK. Also, the Deserializer $\overline{\text{LOCK}}$ output will remain high until its PLL locks to an incoming data or sync-pattern on the RIN pins.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. The Serializer that is generating the stream to the Deserializer must send random (non-repetitive) data patterns or sync-patterns during this step of the Initialization State. The Deserializer will lock onto sync-patterns within a specified amount of time. The lock to random data depends on the data patterns and therefore, the lock time is unspecified.

In order to lock to the incoming LVDS data stream, the Deserializer identifies the rising clock edge in a sync-pattern and after 150 clock cycles will synchronize. If the Deserializer is locking to a random data stream from the Serializer, then it performs a series of operations to identify the rising clock edge and locks to it. Because this locking procedure depends on the data pattern, it is not possible to specify how long it will take. At the point where the Deserializer's PLL locks to the embedded clock, the $\overline{\text{LOCK}}$ pin goes low and valid data appears on the output. Note that the $\overline{\text{LOCK}}$ signal is synchronous to valid data appearing on the outputs.

The user's application determines whether sync-pattern or lock to random data is the preferred method for synchronization. If sync-patterns are preferred, the associated deserializers $\overline{\text{LOCK}}$ pin is a convenient way to provide control of the SYNC pin.

DATA TRANSFER

After initialization, the DS92LV16 Serializer is able to transfer data to the Deserializer. The serial data stream includes a start bit and stop bit appended by the serializer, which frame the sixteen data bits. The start bit is always high and the stop bit is always low. The start and stop bits also function as clock bits embedded in the serial stream.

The Serializer block accepts data from the DIN0-DIN15 parallel inputs. The TCLK signal latches the incoming data on the rising edge. If the SYNC input is high for 6 TCLK cycles, the DS92LV16 does not latch data on the DIN0-DIN15.

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The Serializer transmits the data and clock bits (16+2 bits) at 18 times the TCLK frequency. For example, if TCLK is 60 MHz, the serial rate is 60 X 18 = 1080 Mbps. Since only 16 bits are from input data, the serial 'payload' rate is 16 times the TCLK frequency. For instance, if TCLK = 60 MHz, the payload data rate is 60 X 16 = 960 Mbps. TCLK is provided by the data source and must be in the range of 25 MHz to 80 MHz.

When the Deserializer channel synchronizes to the input from a Serializer, it drives its $\overline{\text{LOCK}}$ pin low and synchronously delivers valid data on the output. The Deserializer locks to the embedded clock, uses it to generate multiple internal data strobes, and then drives the recovered clock on the RCLK pin. The RCLK is synchronous to the data on the ROUT[0:15] pins. While $\overline{\text{LOCK}}$ is low, data on ROUT[0:15] is valid. Otherwise, ROUT[0:15] is invalid.

ROUT[0:15], $\overline{\text{LOCK}}$, and RCLK signals will drive a minimum of three CMOS input gates (15pF total load) at a 80 MHz clock rate. This drive capacity allows bussing outputs of multiple Deserializers and multiple destination ASIC inputs. REN controls TRI-STATE of the all outputs.

The Deserializer input pins are high impedance during Receiver Powerdown (RPWDN* low) and power-off (VCC = 0V).

RESYNCHRONIZATION

Whenever the Deserializer loses lock, it will automatically try to resynchronize. For example, if the embedded clock edge is not detected two times in succession, the PLL loses lock and the $\overline{\text{LOCK}}$ pin is driven high. The Deserializer then enters the operating mode where it tries to lock to random a data stream. It looks for the embedded clock edge, identifies it and then proceeds through the synchronization process.

The logic state of the $\overline{\text{LOCK}}$ signal indicates whether the data on ROUT is valid; when it is low, the data is valid. The system must monitor the $\overline{\text{LOCK}}$ pin to determine whether data on the ROUT is valid. Because there is a short delay in the $\overline{\text{LOCK}}$ signals response to the PLL losing synchronization to the incoming data stream, the system must determine the validity of data for the cycles before the $\overline{\text{LOCK}}$ signal goes high.

The user can choose to resynchronize to the random data stream or to force fast synchronization by pulsing the Serializer SYNC pin. Since lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. The primary constraint on the "random" lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. An advantage of using the SYNC pattern to force synchronization is the ability for user to predict the delay for PLL to regain lock. This scheme is left up to the user discretion. One recommendation is to provide a feedback loop using the $\overline{\text{LOCK}}$ pin itself to control the sync request of the Serializer, which is the SYNC pin.

If a specific pattern is repetitive, the Deserializer's PLL will not lock in order to prevent the Deserializer to lock to the data pattern rather than the clock. We refer to such pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes places in a clock cycle over multiple cycles. This occurs when any bit, except DIN 15, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. The internal circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the $\overline{\text{LOCK}}$ output from becoming active until the RMT pattern changes. Once the RMT pattern changes and the internal circuitry recognized the clock bits in the serial data stream, the PLL of the Deserializer will lock, which will drive the $\overline{\text{LOCK}}$ output to low and the output data ROUT will become valid.

POWERDOWN

The Powerdown state is a low power sleep mode that the Serializer and Deserializer will occupy while waiting for initialization. You can also use TPWDN* and RPWDN* to reduce power when there are no pending data transfers. The Deserializer enters Powerdown when RPWDN* is driven low. In Powerdown, the PLL stops and the outputs go into TRI-STATE, which reduces supply current to the µA range.

To bring the Deserializer block out of the Powerdown state, the system drives RPWDN* high. When the Deserializer exits Powerdown, it automatically enters the Initialization state. The system must then allow time for Initialization before data transfer can begin.

The TPWDN* driven to a low condition forces the Serializer block into low power consumption where the supply current is in the µA range. The Serializer PLL stops and the output goes into a TRI-STATE condition.

To bring the Serializer block out of the Powerdown state, the system drives TPWDN* high. When the Serializer exits Powerdown, its PLL must lock the TCLK before it is ready for the Initialization state. The system must then allow time for Initialization before data transfer can begin.

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LOOPBACK TEST OPERATION

The DS92LV16 includes two Loopback modes for testing the device functionality and the transmission line continuity. Asserting the Line Loopback control signal connects the serial data input (RIN+/−) to the serial data output (DO+/−) and to the parallel data output (ROUT[0:15]). The serial data goes through deserializer and serializer blocks.

Asserting the Local Loopback control signal connects the parallel data input (DIN[0:15]) back to the parallel data output (ROUT[0:15]). The connection route includes all the functional blocks of the SER/DES Pair. The serial data output (DO+/−) is automatically disabled during the Local Loopback operating mode.

TRI-STATE

When the system drives the REN pin low, the Deserializer output enter TRI-STATE. This will TRI-STATE the receiver output pins (ROUT[0:15]) and RCLK. When the system drives REN high, the Deserilaizer will return to the previous state as long as all other control pins remain static (RPWDN*).

When the system drives the DEN pin low, the Serializer output enters TRI-STATE. This will TRI-STATE the LVDS output. When the system drives the DEN signal high, the Serializer output will return to the previous state as long as all other control and data input pins remain in the same condition as when the DEN was driven low.

APPLICATION INFORMATION

Using the DS92LV16

The DS92LV16 combines a Serializer and a Deserializer into a single chip that sends 16 bits of parallel TTL data over a serial Bus LVDS link up to 1.28 Gbps. Serialization of the input data is accomplished using an onboard PLL at the Serializer which embeds two clock bits with the data. The Deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and deserialize the data. The Deserializer monitors the incoming clock information to determine lock status and will indicate loss of lock by raising the $\overline{\text{LOCK}}$ output.

Power Considerations

All CMOS design of the Serializer and Deserializer makes them inherently low power devices. Additionally, the constant current source nature of the LVDS outputs minimize the slope of the speed vs. I_{CC} curve of CMOS designs.

Powering Up the Deserializer

The REFCLK input can be running before the Deserializer is powered up and it must be running in order for the Deserializer to lock to incoming data. The Deserializer outputs will remain in TRI-STATE until the Deserializer detects data transmission at its inputs and locks to the incoming stream.

Noise Margin

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

- **Serializer:** TCLK jitter, V_{CC} noise (noise bandwidth and out-of-band noise)
- **Media:** ISI, V_{CM} noise
- **Deserializer:** V_{CC} noise

For typical receiver noise margin, please see Figure 17.

Recovering from LOCK Loss

In the case where the Serializer loses lock during data transmission up to 5 cycles of data that was previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 2 times in a row to indicate loss of lock. Since clock information has been lost it is possible that data was also lost during these cycles. When the Deserializer $\overline{\text{LOCK}}$ pin goes low, data from at least the previous 5 cycles should be resent upon regaining lock.

Lock can be regained at the Deserializer by causing the Serializer to resend SYNC patterns as described above or by random lock which can take more time depending upon the data patterns being received.

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Input Failsafe

In the event that the Deserializer is disconnected from the Serializer, the failsafe circuitry is designed to reject certain amount of noise from being interpreted as data or clock. The outputs will be tri-stated and the Deserializer will lose lock.

Hot Insertion

All the LVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground.

PCB Layout and Power System Considerations

Circuit board layout and stack-up for the BLVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitic, especially proven effective at high frequencies above approx 50MHz, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

It is a recommended practice to use two vias at each power pin as well as at all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components. Locate RF capacitors as close as possible to the supply pins, and use wide low impedance traces (not 50 Ohm traces). Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pin straight to the power and ground plane, with the bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pin to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. User must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30MHz range. To provide effective bypassing, very often, multiple capacitors are used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two via from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate CMOS (TTL) swings away from the LVDS lines to prevent coupling from the CMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ohms are typically recommended for LVDS interconnect. The closely-coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. Also the tight coupled lines will radiate less.

Termination of the LVDS interconnect is required. For point-to-point applications termination should be located at the load end. Nominal value is 100 Ohms to match the line's differential impedance. Place the resistor as close to the receiver inputs as possible to minimize the resulting stub between the termination resistor and receiver.

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: http://www.ti.com/ww/en/analog/interface/lvds.shtml

Specific guidance for this device is provided next:

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DS92LV16 BLVDS SER/DES PAIR

General device specific guidance is given below. Exact guidance can not be given as it is dictated by other board level /system level criteria. This includes the density of the board, power rails, power supply, and other integrated circuit power supply needs.

DVDD = Digital section power supply

These pins supply the digital portion of the device and also receiver output buffers. The TX DVDD is less critical. The RX DVDD requires more bypass to power the outputs under synchronous switching conditions. The receiver DVDD pins power 4 outputs from each DVDD pin. An estimate of local capacitance required indicates a minimum of 22nF is required. This is calculated by taking 4 times the maximum short current (4 X 70 = 280mA) multiplying by the rise time of the part (4ns) and dividing by the maximum allowed droop in VDD (assume 50mV) yields 22.4nF. Rounding up to a standard value, 0.1uF is selected for each DVDD pin.

PVDD = PLL section power supply

The PVDD pin supplies the PLL circuit. Note that the DS92LV16 has two separate PLLs and supply pins. The PLL(s) require clean power for the minimization of Jitter. A supply noise frequency in the 300kHZ to 1MHz range can cause increased output jitter. Certain power supplies may have switching frequencies or high harmonic content in this range. If this is the case, filtering of this noise spectrum may be required. A notch filter response is best to provide a stable VDD, suppression of the noise band, and good high-frequency response (clock fundamental). This may be accomplished with a pie filter (CRC or CLC). If employed, a separate pie filter is recommended for each PLL to minimize drop in potential due to the series resistance. The pie filter should be located close to the PVDD power pin. Separate power planes for the PVDD pins is typically not required.

AVDD = LVDS section power supply

The AVDD pin supplies the LVDS portion of the circuit. The DS92LV16 has four AVDD pins. Due to the nature of the design, current draw is not excessive on these pins. A 0.1uF capacitor is sufficient for these pins. If space is available it 0.01uF may be used in parallel with the 0.1uF capacitor for additional high frequency filtering.

GROUNDs

The AGND pin should be connected to the signal common in the cable for the return path of any common-mode current. Most of the LVDS current will be odd-mode and return within the interconnect pair. A small amount of current may be even-mode due to coupled noise, and driver imbalances. This current should return via a low impedance known path.

A solid ground plane is recommended for both DVDD, PVDD or AVDD. Using a split plane may have potential problem of ground loops, or difference in ground potential at various ground pins of the device.

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PIN DIAGRAM

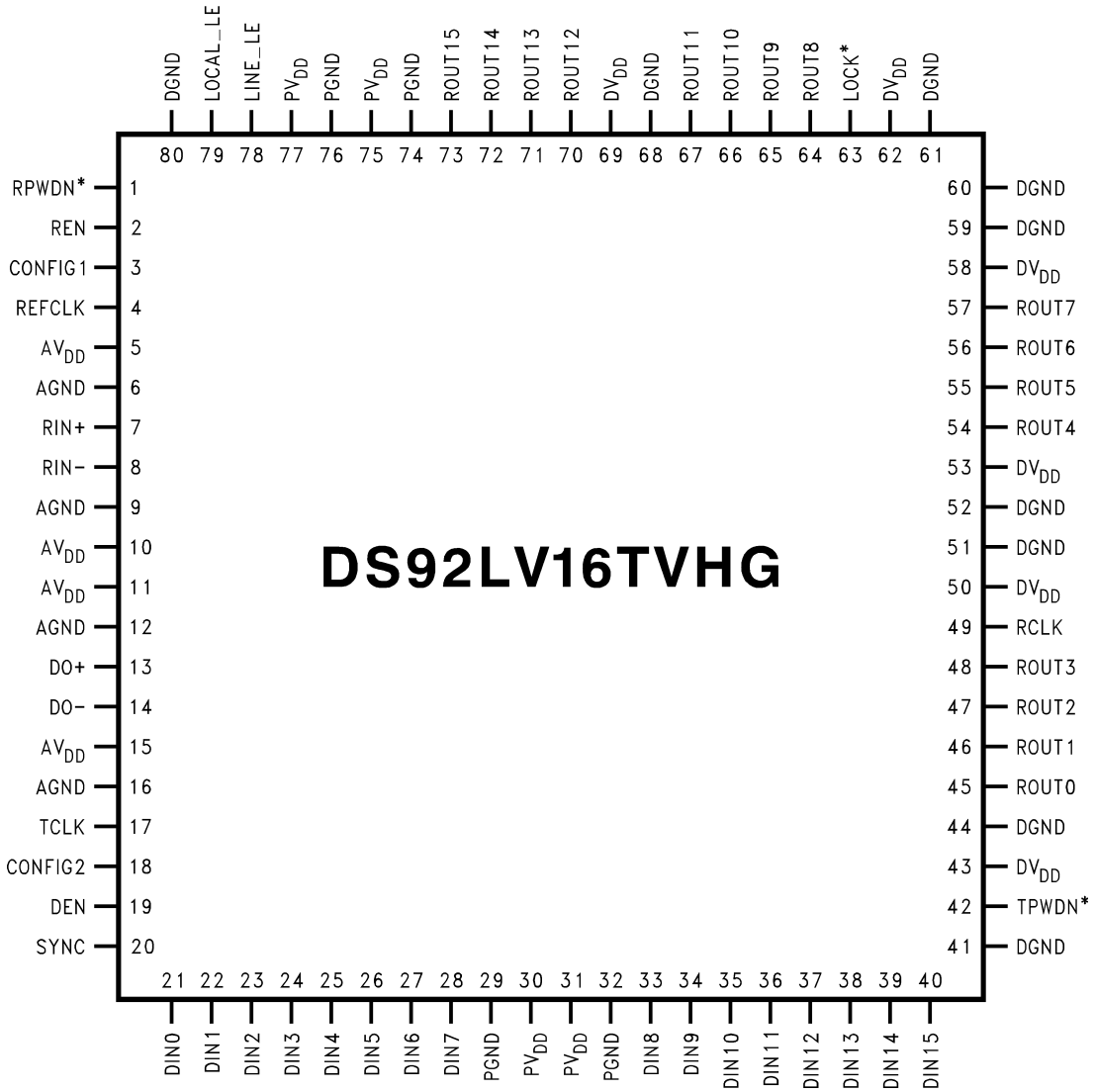

Figure 22. DS92LV16TVHG (Top View)

PIN DESCRIPTIONS

Pin #	Pin Name	I/O	Description
1	RPWDN*	CMOS, I	RPWDN* = Low will put the Receiver in low power, stand-by, mode. Note: The Receiver PLL will lose lock.(1)
2	REN	CMOS, I	REN = Low will disable the Receiver outputs. Receiver PLL remains locked. (See $\overline{\text{LOCK}}$ pin description)(1)
3	CONFIG1		Configuration pin - strap or tie this pin to High with pull-up resistor. No-connect or Low reserved for future use.
4	REFCLK	CMOS, I	Frequency reference clock input for the receiver.
5, 10, 11, 15	AVDD		Analog Voltage Supply
6,9,12,16	AGND		Analog Ground
7	RIN+	LVDS, I	Receiver LVDS True Input
8	RIN-	LVDS, I	Receiver LVDS Inverting Input
13	DO+	LVDS, O	Transmitter LVDS True Output

(1) Input defaults to "low" state when left open due to internal pull-device.

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PIN DESCRIPTIONS (continued)

Pin #	Pin Name	I/O	Description
14	DO-	LVDS, O	Transmitter LVDS Inverting Output
17	TCLK	CMOS, I	Transmitter reference clock. Used to strobe data at the DIN Inputs and to drive the transmitter PLL. See SERIALIZER TIMING REQUIREMENTS FOR TCLK
18	CONFIG2		Configuration pin - strap or tie this pin to High with pull-up resistor. No-connect or Low reserved for future use.
19	DEN	CMOS, I	DEN = Low will disable the Transmitter outputs. The transmitter PLL will remain locked. (1)
20	SYNC	CMOS, I	SYNC = High will cause the transmitter to ignore the data inputs and send SYNC patterns to provide a locking reference to receiver(s). See Functional Description. (1)
21, 22, 23, 24, 25, 26, 27, 28, 33, 34, 35, 36, 37, 38, 39, 40	DIN (0:15)	CMOS, I	Transmitter data inputs. (1)
29,32	PGND		PLL Ground.
30,31	PVDD		PLL Voltage supply.
41, 44, 51, 52, 59, 60, 61, 68, 80	DGND		Digital Ground.
42	TPWDN*	CMOS, I	TPWDN* = Low will put the Transmitter in low power, stand-by mode. Note: The transmitter PLL will lose lock. (2)
43, 50, 53, 58, 62, 69	DVDD		Digital Voltage Supplies.
45, 46, 47, 48, 54, 55, 56, 57, 64, 65, 66, 67, 70, 71, 72, 73	ROUT (0:15)	CMOS, O	Receiver Outputs.
49	RCLK	CMOS, O	Recovered Clock. Parallel data rate clock recovered from embedded clock. Used to strobe ROUT (0:15). LVCMOS Level output.
63	LOCK*	CMOS, O	LOCK* indicates the status of the receiver PLL. $\overline{\text{LOCK}}$ = H - receiver PLL is unlocked, $\overline{\text{LOCK}}$ = L - receiver PLL is locked.
74,76	PGND		PLL Grounds.
75,77	PVDD		PLL Voltage Supplies.
78	LINE_LE	CMOS, I	LINE_LE = High enables the receiver loopback mode. Data received at the RIN+/- inputs is fed back through the DO+/- outputs. (2)
79	LOCAL_LE	CMOS, I	LOCAL_LE = High enables the transmitter loopback mode. Date received at the DIN inputs is fed back through the ROUT outputs. (2)

(2) Input defaults to "low" state when left open due to internal pull-device.

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REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS92LV16TVHG	NRND	LQFP	PN	80	119	Non-RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DS92LV16TVHG >B	
DS92LV16TVHG/NOPB	ACTIVE	LQFP	PN	80	119	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	DS92LV16TVHG >B	Samples
DS92LV16TVHGX/NOPB	ACTIVE	LQFP	PN	80	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	DS92LV16TVHG >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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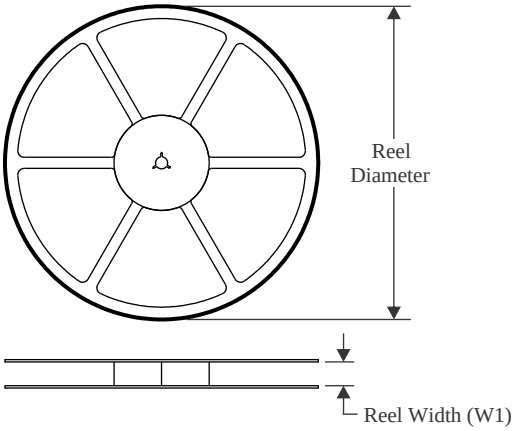
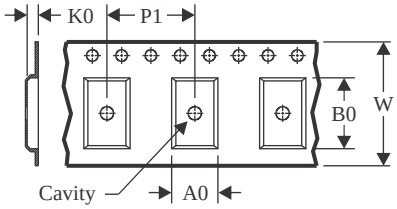
TAPE AND REEL INFORMATION

REEL DIMENSIONS

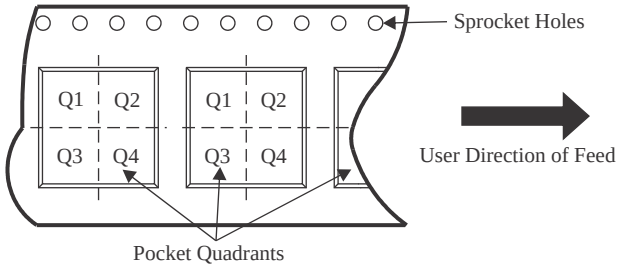


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

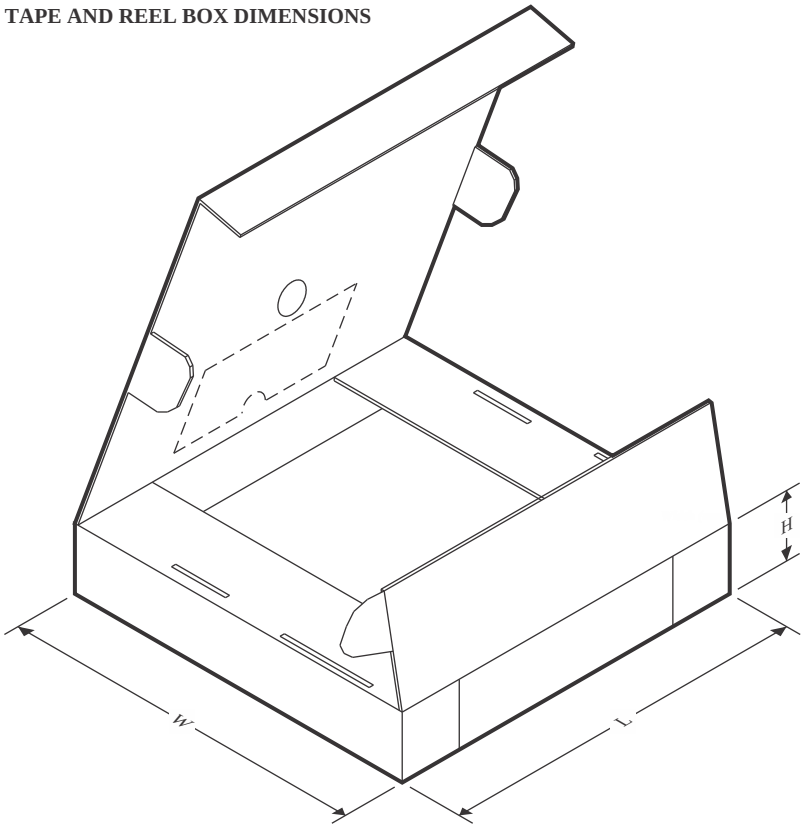
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV16TVHGX/NOPB	LQFP	PN	80	1000	330.0	24.4	14.65	14.65	2.15	24.0	24.0	Q2

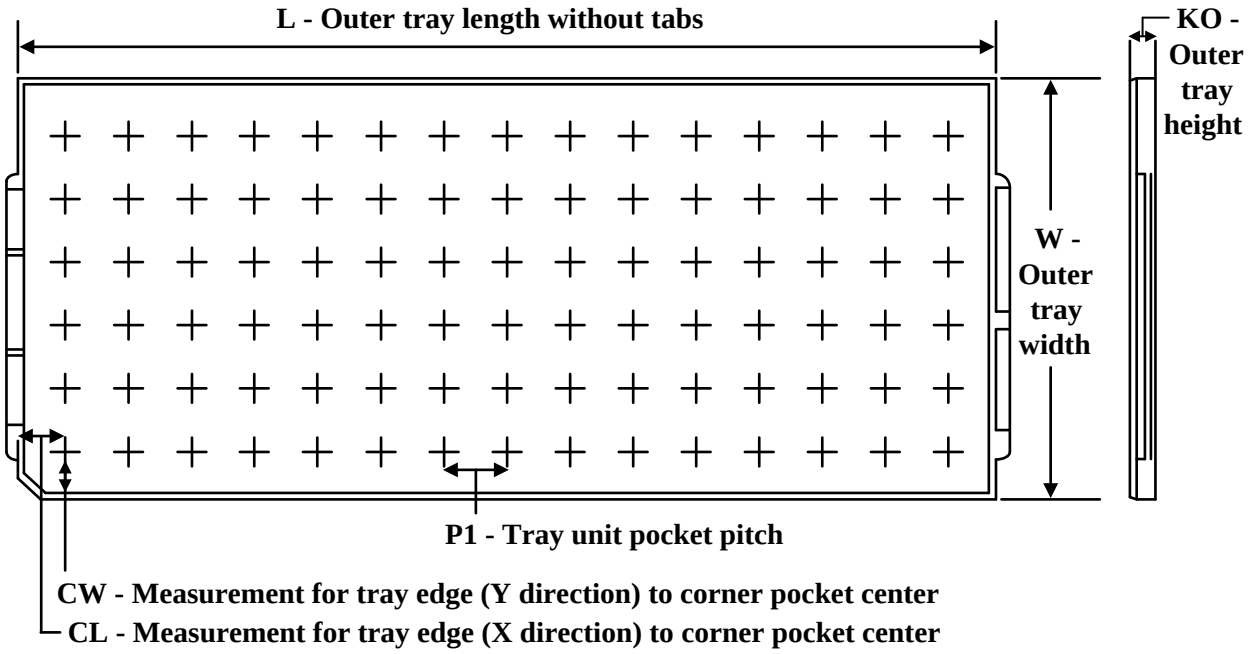
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV16TVHGX/NOPB	LQFP	PN	80	1000	367.0	367.0	45.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

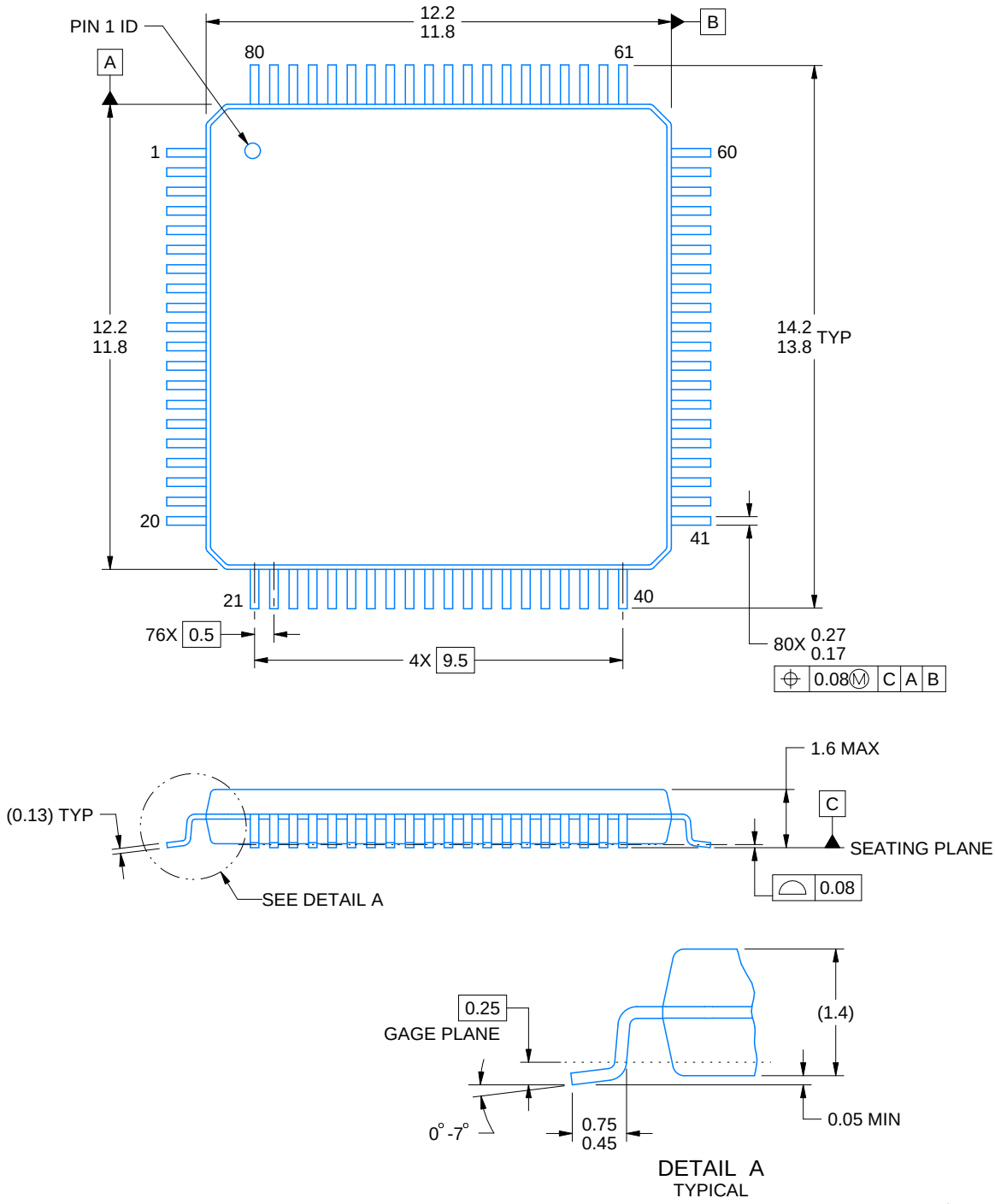
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS92LV16TVHG	PN	LQFP	80	119	7 X 17	150	322.6	135.9	7620	17.9	14.3	13.95
DS92LV16TVHG	PN	LQFP	80	119	7 X 17	150	322.6	135.9	7620	17.9	14.3	13.95
DS92LV16TVHG/NOPB	PN	LQFP	80	119	7 X 17	150	322.6	135.9	7620	17.9	14.3	13.95

PACKAGE OUTLINE

PN0080A

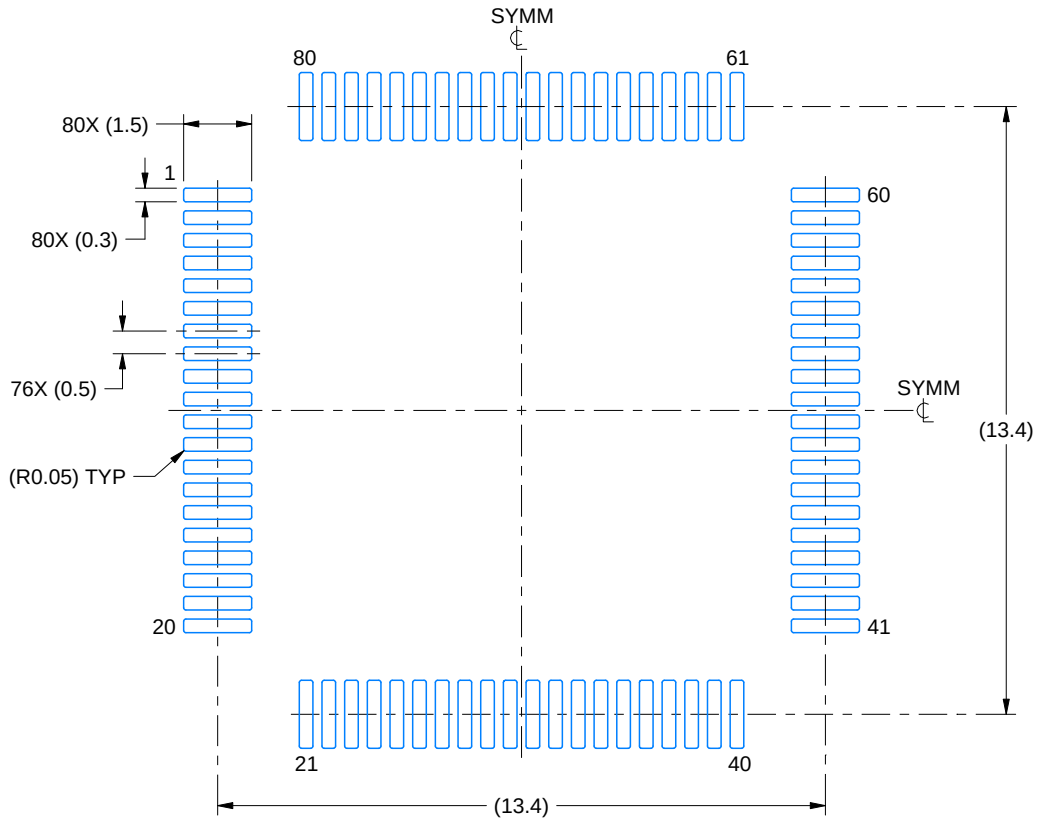
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

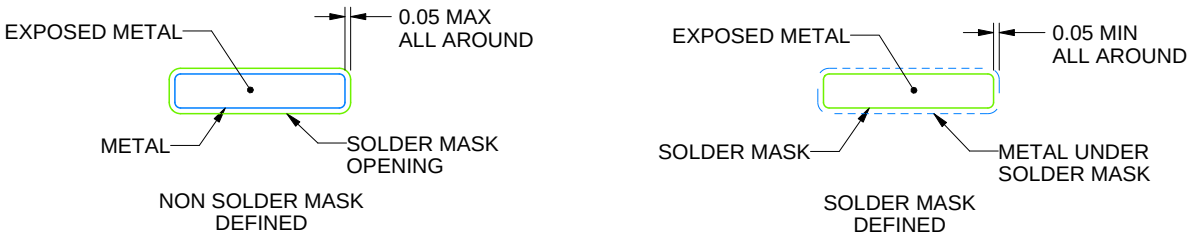


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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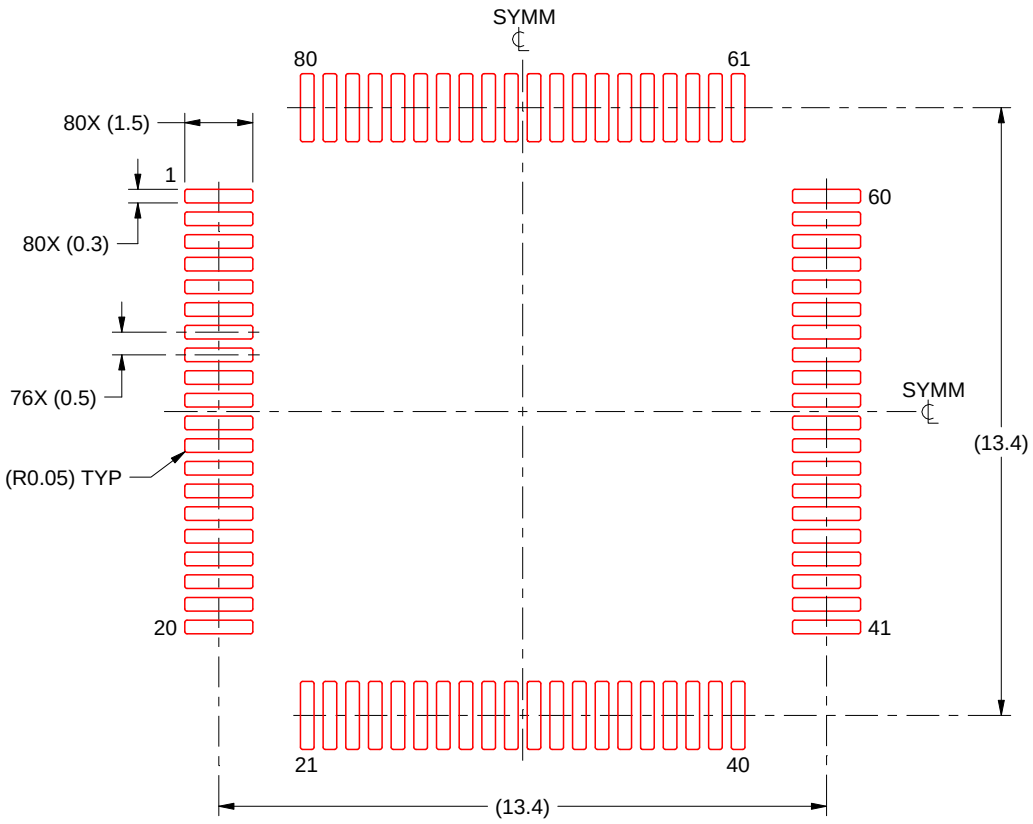
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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