INA333-Q1 汽车零偏移微功率仪表放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C ≤ T_A ≤ +125°C
- 低失调电压：25µV（最大值），G ≥ 100
- 低温漂：0.1µV/°C，G ≥ 100
- 低噪声：50nV/√Hz，G ≥ 100
- 高 CMRR：100dB（最小值），G ≥ 10
- 低输入偏置电流：200pA（最大值）
- 电源电压范围：1.8V 至 5.5V
- 输入电压：(V–) + 0.1V 至 (V+) – 0.1V
- 输出范围：(V–) + 0.05V 至 (V+) – 0.05V
- 低静态电流：50µA
- 工作温度：–40°C 至 +125°C
- RFI 滤波输入
- 封装：8 引脚 VSSOP

2 应用

- 动力总成扭矩传感器
- 动力总成压力传感器
- 动力总成温度传感器
- 动力总成爆震传感器
- 车辆乘员检测传感器
- 驾驶员生命体征监测

3 说明

INA333-Q1 是一款具备出色精度的低功耗精密仪表放大器。该器件采用多功能三级运算放大器设计，尺寸小巧，非常适合各种汽车 应用（使用电阻式电桥传感器）。

可通过单个外部电阻器在 1 到 1000 范围内设置增益。INA333-Q1 设计为采用符合业界通用的增益公式：G = 1 + (100kΩ/R_G)。

INA333-Q1 提供极低的失调电压（25µV，G ≥ 100）、出色的失调电压漂移（0.1µV/°C，G ≥ 100）和高共模抑制（G ≥ 10 时为 100dB）。该器件采用低至 1.8V (±0.9V) 的电源电压，静态电流仅 50µA，因此非常适合电池供电系统。自动校准技术可在工业温度范围内保持出色的精度。INA333-Q1 还提供向下扩展至直流的超低噪声密度 (50nV/√Hz)。

INA333-Q1 器件采用 8 引脚 VSSOP 封装，额定温度范围 T_A = –40°C 至 +125°C。

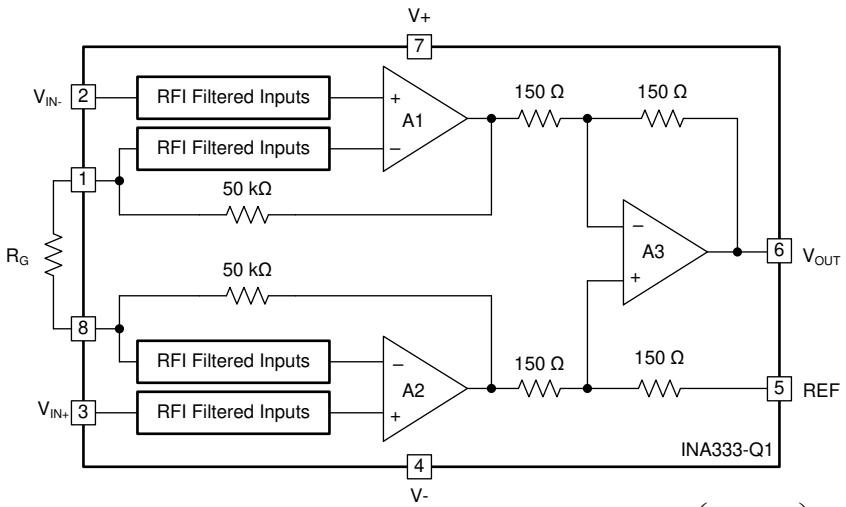
器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA333-Q1	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

ADVANCE INFORMATION

简化原理图



$$G = 1 + \left(\frac{100\ k\Omega}{R_G}\right)$$

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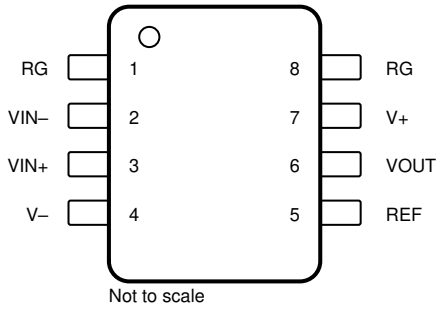
4 修订历史记录

日期	修订版本	说明
2019 年 10 月	*	初始发行版。

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
RG	1, 8	—	Gain setting pins. For gains greater than 1, place a gain resistor between pins 1 and 8.
V+	7	—	Positive supply
V–	4	—	Negative supply
VIN+	3	I	Positive input
VIN–	2	I	Negative input
VOUT	6	O	Output

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage		7	V
	Analog input voltage(2)	(V–) – 0.3	(V+) + 0.3	V
	Output short-circuit(3)	Continuous		
T_A	Operating temperature	–40	150	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA333-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

at V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT(1)							
V_{OSI}	Offset voltage, RTI(2)				±10 ±25/G	±25 ±75/G	µV
PSRR	Power-supply rejection ratio				±1 ±5/G	±5 ±15/G	µV/V
		T_A = –40°C to +125°C				±0.1 ±0.5/G	µV/°C
	Long-term stability				See (3)		
	Turn on time to specified V_{OSI}	T_A = –40°C to +125°C			See *Typical Characteristics*		
Z_{IN}	Input impedance	Differential			100 || 3		GΩ || pF
		Common-mode			100 || 3		
V_{CM}	Common-mode voltage	V_O = 0 V		(V–) + 0.1		(V+) – 0.1	V
CMRR	Common-mode rejection ratio	DC to 60 Hz, V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	G = 1	80	90		dB
			G = 10	100	110		
			G = 100	100	115		
			G = 1000	100	115		
INPUT BIAS CURRENT							
I_B	Input bias current				±70	±200	pA
		T_A = –40°C to +125°C			See Figure 26		pA/°C
I_{OS}	Input offset current				±50	±200	pA
		T_A = –40°C to +125°C			See Figure 28		pA/°C
INPUT VOLTAGE NOISE							
e_{NI}	Input voltage noise	G = 100, R_S = 0 Ω	f = 10 Hz		50		nV/√Hz
			f = 100 Hz		50		
			f = 1 kHz		50		
			f = 0.1 Hz to 10 Hz		1		$µV_{PP}$
i_N	Input current noise	f = 10 Hz			100		fA/√Hz
		f = 0.1 Hz to 10 Hz			2		pA_{PP}
GAIN							
	Gain equation				1 + (100 kΩ/R_G)		V/V
G	Gain			1		1000	V/V
	Gain error	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV	G = 1		±0.01%	±0.1%	
			G = 10		±0.05%	±0.25%	
			G = 100		±0.07%	±0.25%	
			G = 1000		±0.25%	±0.5%	
	Gain drift error	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV, T_A = –40°C to +125°C	G = 1		±1	±5	ppm/°C
			G > 1(4)		±15	±50	ppm/°C
	Gain nonlinearity	V_S = 5.5 V, (V–) + 100 mV ≤ V_O ≤ (V+) – 100 mV, R_L = 10 kΩ			10		ppm
OUTPUT							
	Output voltage swing from rail	V_S = 5.5 V, R_L = 10 kΩ			See Figure 29	50	mV
	Capacitive load drive				500		pF
I_{SC}	Short-circuit current	Continuous to common	Source		5		mA
			Sink		–40		

(1) Total V_{OS}, referred-to-input = (V_{OSI}) + (V_{OSO} / G).
(2) RTI = Referred-to-input.
(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.
(4) Does not include effects of external resistor R_G.

ADVANCE INFORMATION

Electrical Characteristics (continued)

at V_S = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ, V_{REF} = V_S / 2, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
	Bandwidth, –3 dB	G = 1		150		kHz
		G = 10		35		
		G = 100		3.5		
		G = 1000		350		Hz
SR	Slew rate	V_S = 5 V, V_O = 4-V step, G = 1		0.16		V/µs
		V_S = 5 V, V_O = 4-V step, G = 100		0.05		
t_S	Settling time to 0.01%	V_{STEP} = 4 V, G = 1		50		µs
		V_{STEP} = 4 V, G = 100		400		
	Settling time to 0.001%	V_{STEP} = 4 V, G = 1		60		
		V_{STEP} = 4 V, G = 100		500		
	Overload recovery	50% overdrive		75		µs
REFERENCE INPUT						
R_{IN}	Input impedance			300		kΩ
	Reference input voltage		V–		V+	V
POWER SUPPLY						
I_Q	Quiescent current	V_{IN} = V_S / 2		50	75	µA
		V_{IN} = V_S / 2, T_A = –40°C to +125°C			80	

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6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

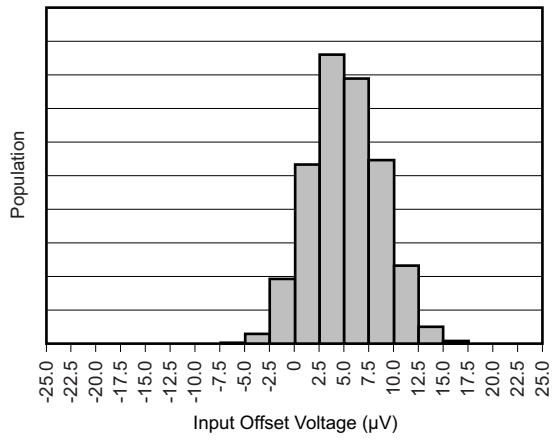


Figure 1. Input Offset Voltage

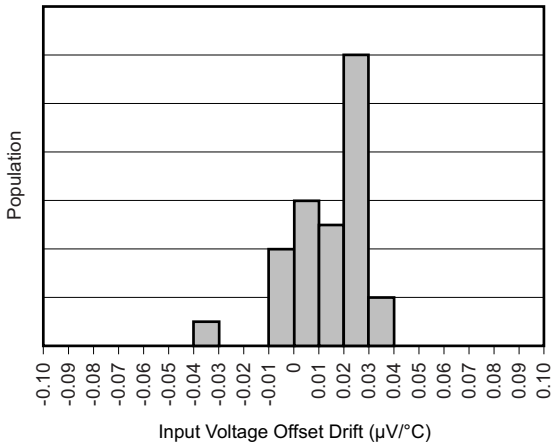


Figure 2. Input Voltage Offset Drift (–40°C to 125°C)

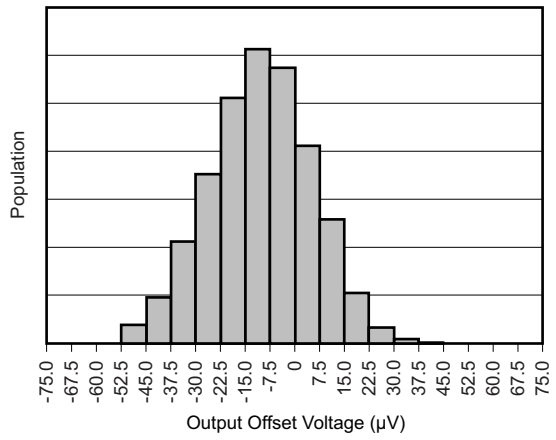


Figure 3. Output Offset Voltage

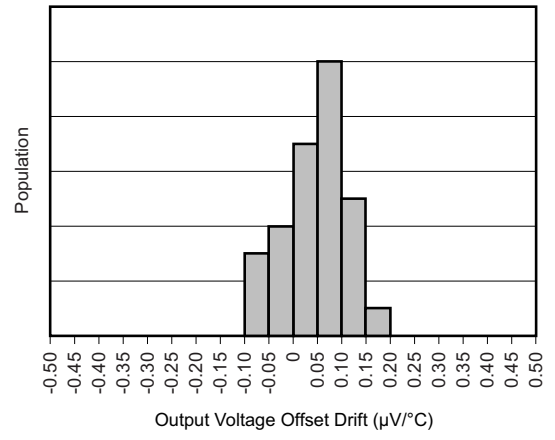


Figure 4. Output Voltage Offset Drift (–40°C to 125°C)

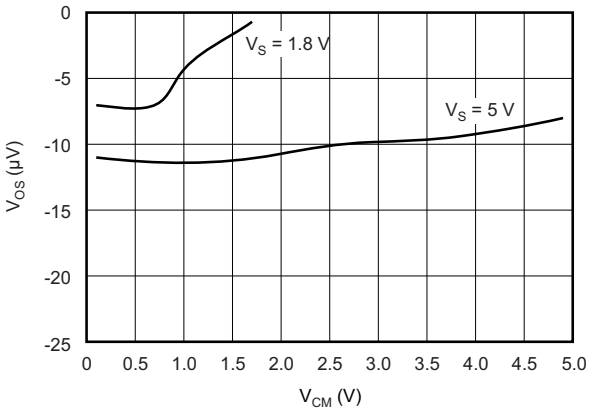


Figure 5. Offset Voltage vs Common-Mode Voltage

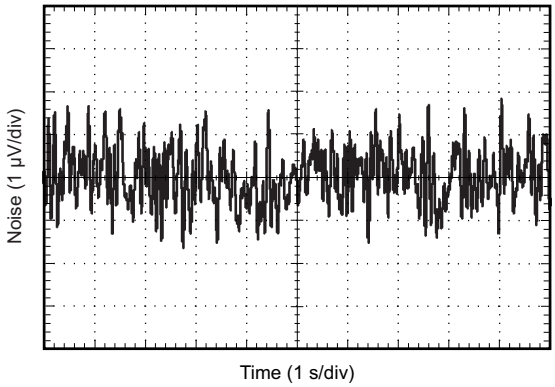


Figure 6. 0.1-Hz to 10-Hz Noise

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

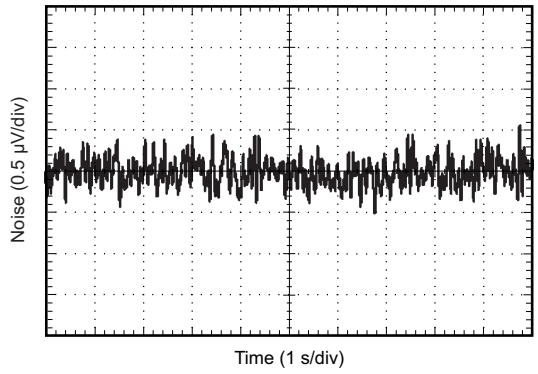


Figure 7. 0.1-Hz to 10-Hz Noise

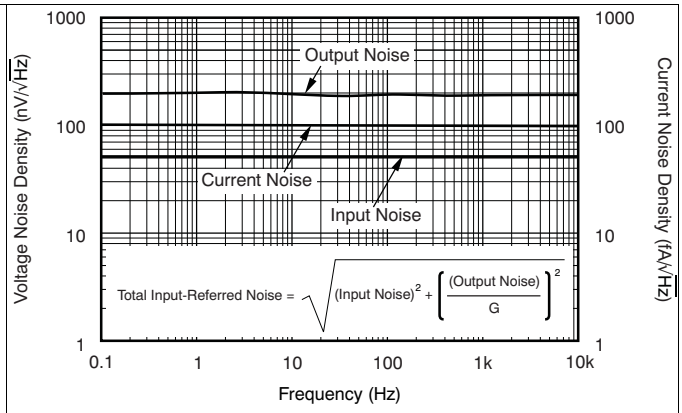


Figure 8. Spectral Noise Density

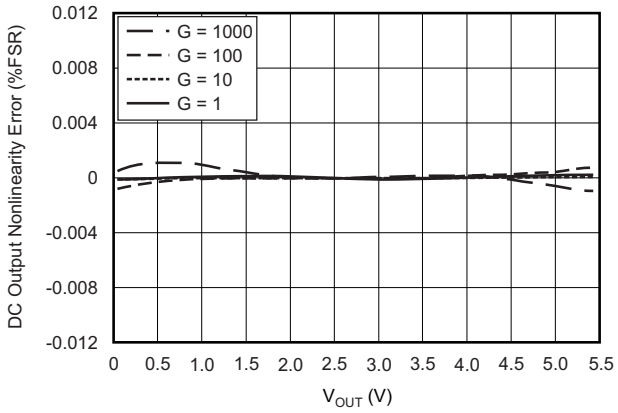


Figure 9. Nonlinearity Error

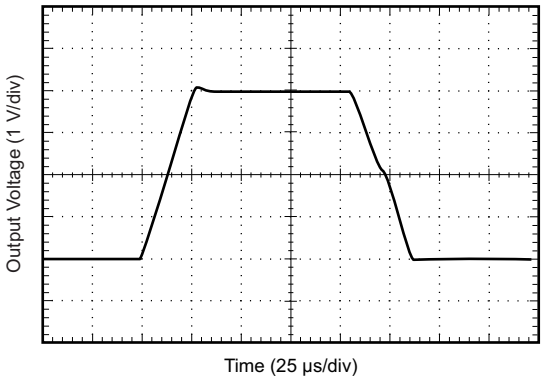


Figure 10. Large Signal Response

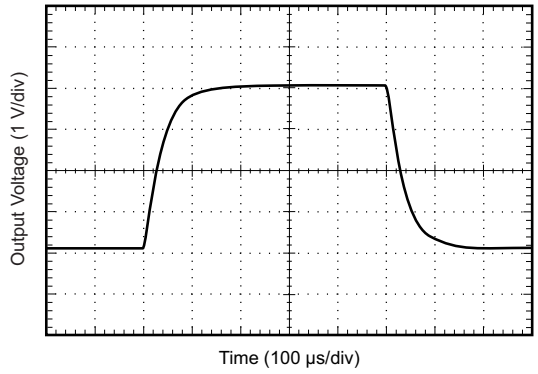


Figure 11. Large-Signal Step Response

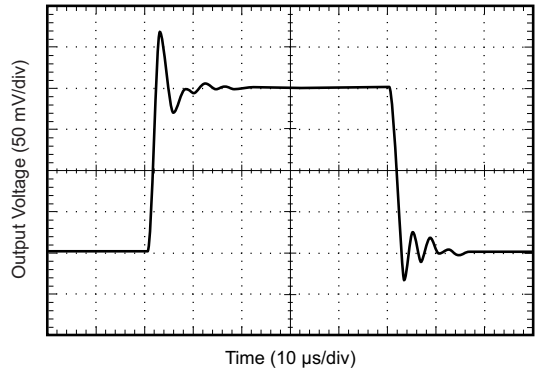


Figure 12. Small-Signal Step Response

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

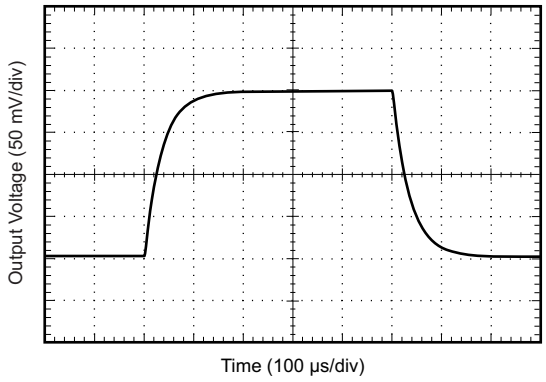


Figure 13. Small-Signal Step Response

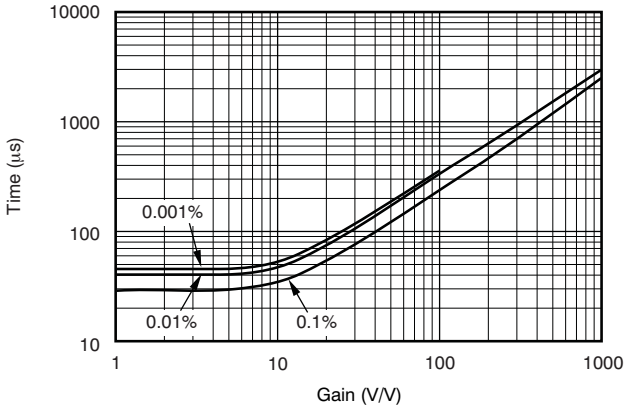


Figure 14. Settling Time vs Gain

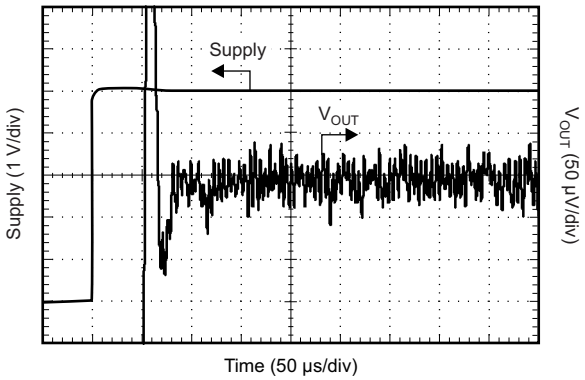


Figure 15. Start-Up Settling Time

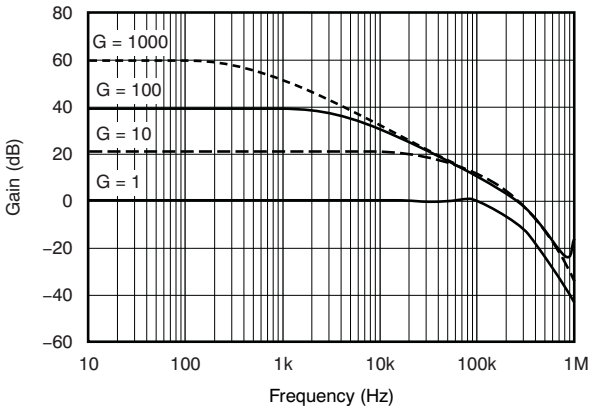


Figure 16. Gain vs Frequency

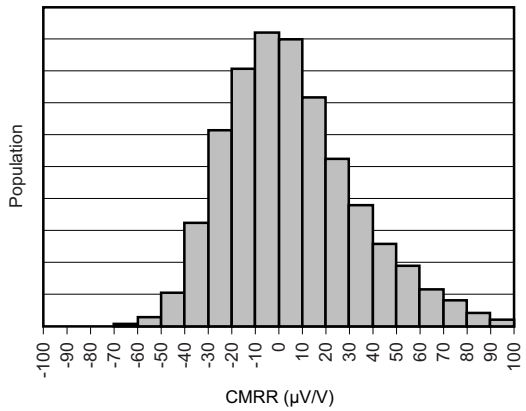


Figure 17. Common-Mode Rejection Ratio

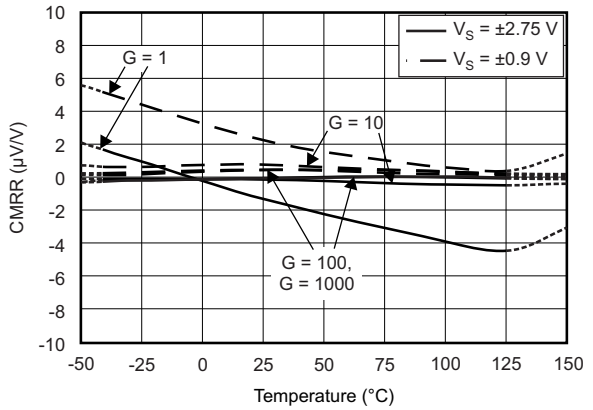


Figure 18. Common-Mode Rejection Ratio vs Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

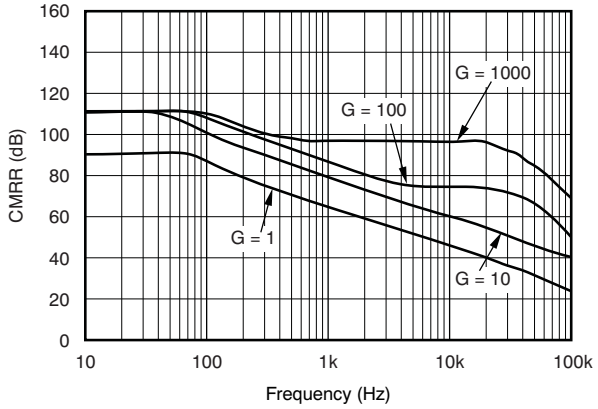


Figure 19. Common-Mode Rejection Ratio vs Frequency

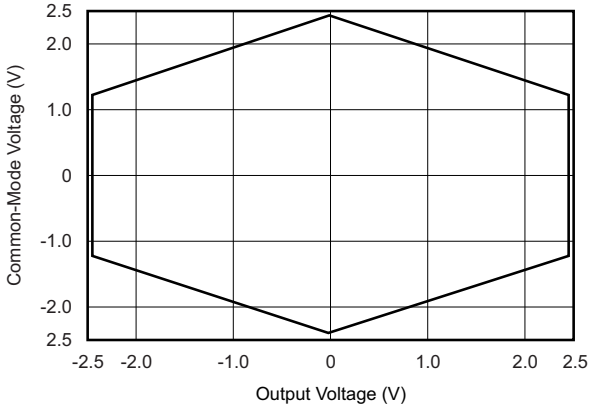


Figure 20. Typical Common-Mode Range vs Output Voltage

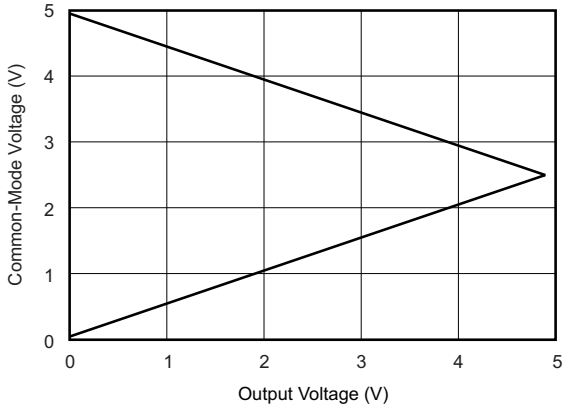


Figure 21. Typical Common-Mode Range vs Output Voltage

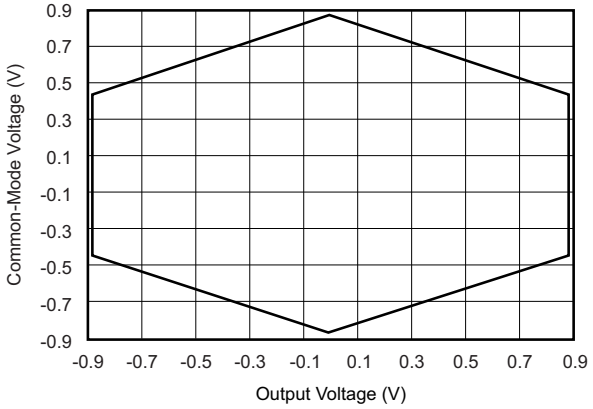


Figure 22. Typical Common-Mode Range vs Output Voltage

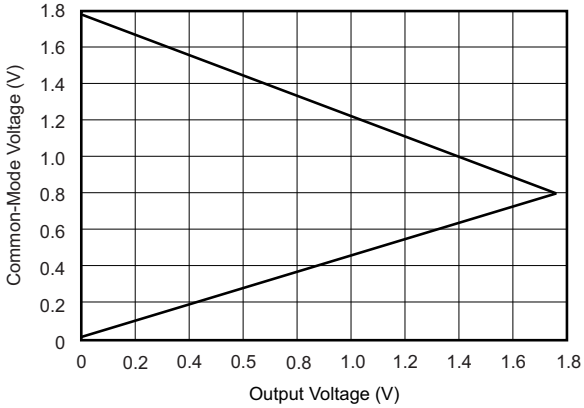


Figure 23. Typical Common-Mode Range vs Output Voltage

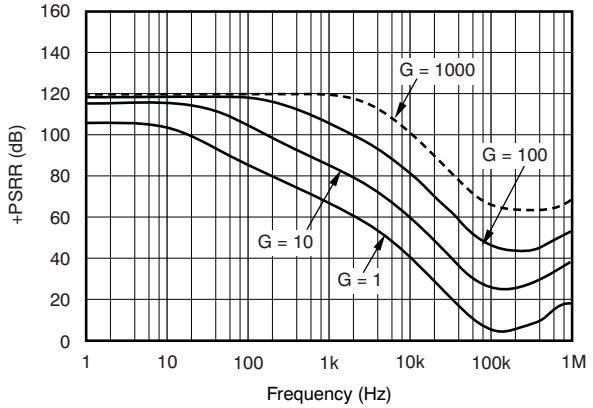


Figure 24. Positive Power-Supply Rejection Ratio

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

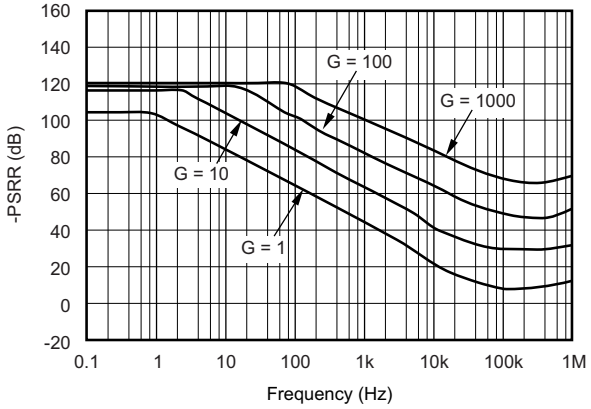


Figure 25. Negative Power-Supply Rejection Ratio

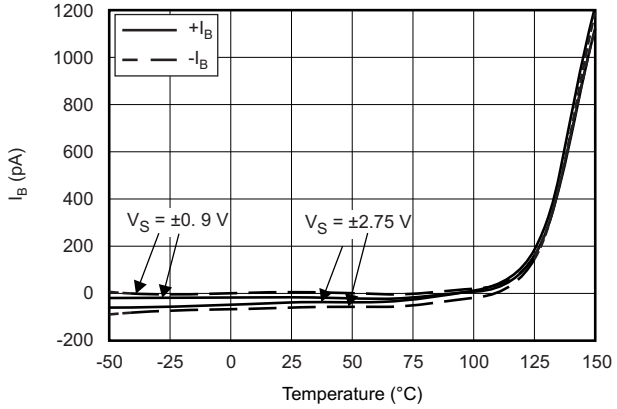


Figure 26. Input Bias Current vs Temperature

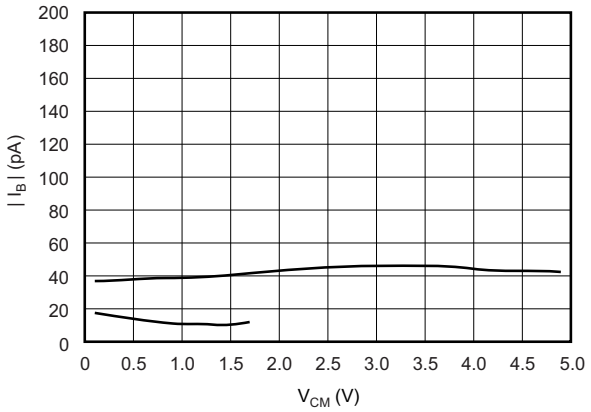


Figure 27. Input Bias Current vs Common-Mode Voltage

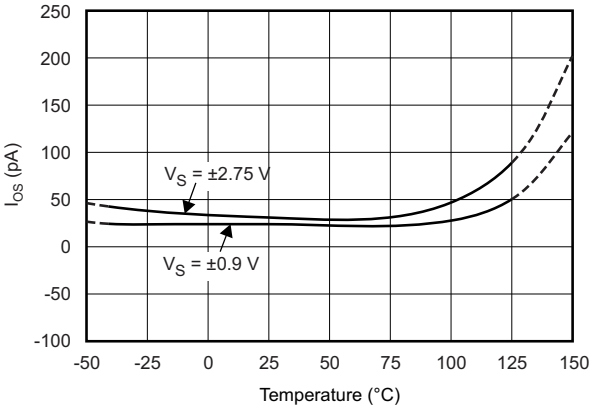


Figure 28. Input Offset Current vs Temperature

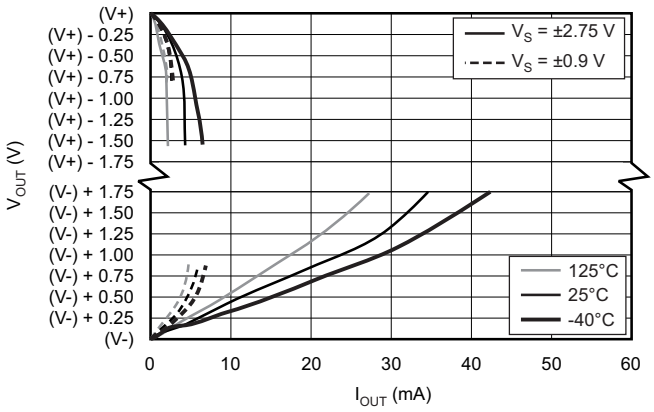


Figure 29. Output Voltage Swing vs Output Current

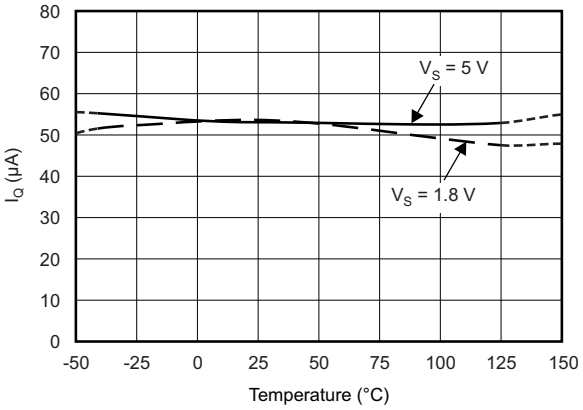


Figure 30. Quiescent Current vs Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, V_{REF} = midsupply, and G = 1 (unless otherwise noted)

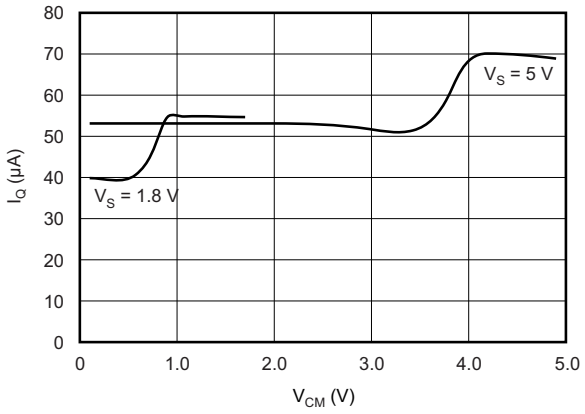


Figure 31. Quiescent Current vs Common-Mode Voltage

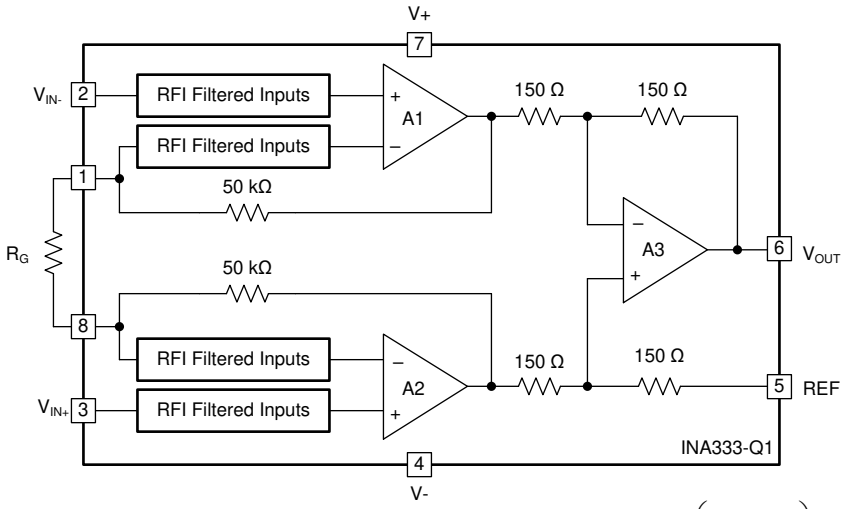
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The INA333-Q1 is a monolithic instrumentation amplifier (INA) based on the precision zero-drift INA333-Q1 (operational amplifier) core. The INA333-Q1 also integrates laser-trimmed resistors to maintain excellent common-mode rejection and low gain error. The combination of the zero-drift amplifier core and the precision resistors allows this device to achieve outstanding dc precision, and makes the INA333-Q1 an excellent choice for many 3.3-V and 5-V automotive applications.

7.2 Functional Block Diagram



$$G = 1 + \left(\frac{100\ k\Omega}{R_G} \right)$$

7.3 Feature Description

7.3.1 Operating Voltage

The INA333-Q1 operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages greater than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

7.3.2 Internal Offset Correction

The INA333-Q1 internal operational amplifiers use an auto-calibration technique with a time-continuous, 350-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. At power up, the amplifier requires approximately 100 µs to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.3 Input Protection

The input pins of the INA333-Q1 are protected with internal diodes connected to the power-supply rails. These diodes clamp and prevent the applied signal from damaging the input circuitry. If the input signal voltage exceeds the power supplies by greater than 0.3 V, limit the input signal current to less than 10 mA to protect the internal clamp diodes. This current limiting is generally done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

7.4 Device Functional Modes

The INA333-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 1.8 V. The recommended maximum specified power-supply voltage for the INA333-Q1 is 5.5 V.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA333-Q1 measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high input impedance makes the INA333-Q1 a great choice for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

8.1.1 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA333-Q1 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A1 and A2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage; see Figure 20 to Figure 23 in the *Typical Characteristics* section.

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333-Q1 is near 0 V even though both inputs are overloaded.

8.2 Typical Application

Figure 32 shows the basic connections required for operation of the INA333-Q1. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333-Q1 is referred to the output reference (REF) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. Although 15 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

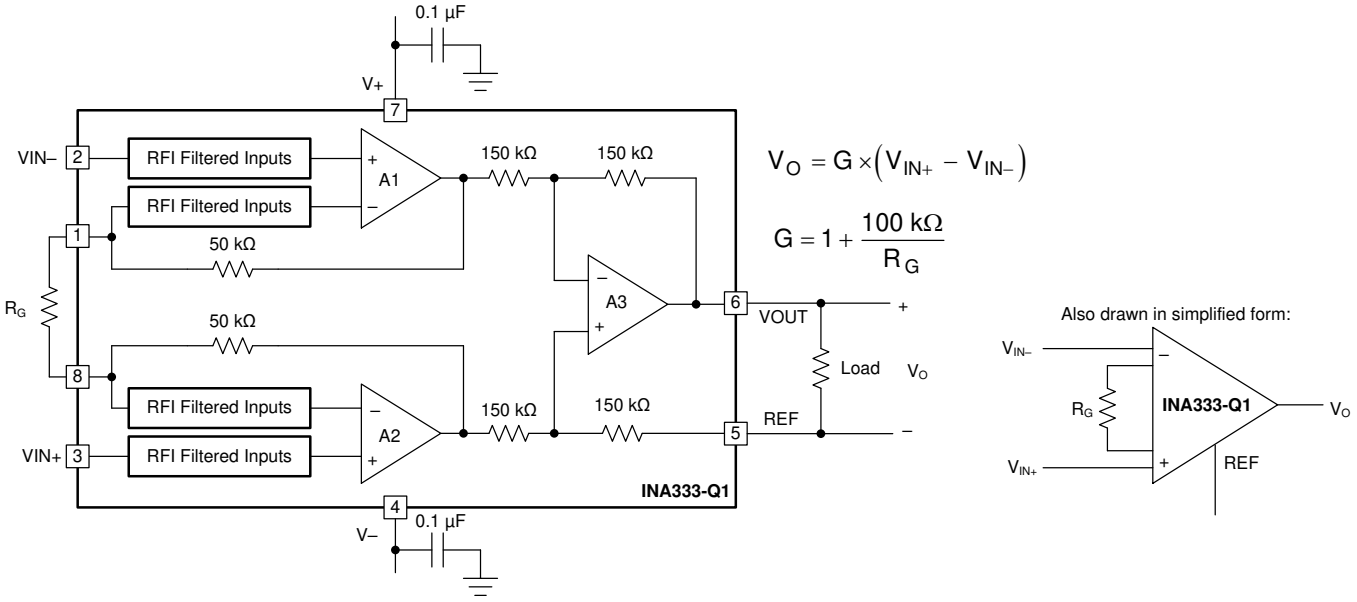


Figure 32. Basic Connections

8.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor RG. The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground. When the input signal increases, the output voltage at the OUT pin increases, too.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Gain

Gain of the INA333-Q1 is set by a single external resistor, R_G, connected between pins 1 and 8. The value of R_G is selected according to Equation 1:

$$G = 1 + (100\ k\Omega / R_G) \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 100 kΩ in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333-Q1.

ADVANCE INFORMATION

Typical Application (continued)

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To maintain stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

(1) NC denotes no connection. When using the SPICE model, the simulation will not converge unless a resistor is connected to the R_G pins; use a very large resistor value.

8.2.2.2 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF pin. Figure 33 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF pin is summed at the output. The operational amplifier buffer provides low impedance at the REF pin to preserve good common-mode rejection.

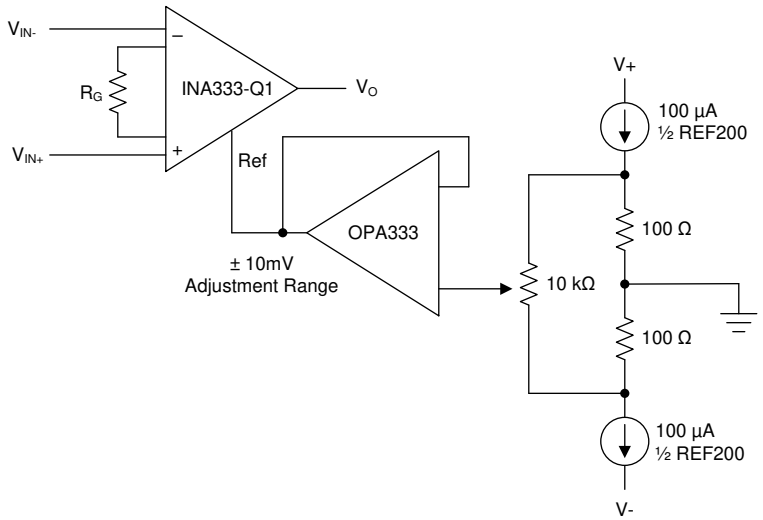


Figure 33. Optional Trimming of Output Offset Voltage

ADVANCE INFORMATION

8.2.2.3 Noise Performance

The auto-calibration technique used by the INA333-Q1 results in reduced low frequency noise, typically only 50 nV/√Hz (G = 100). The spectral noise density is shown in detail in Figure 8. The low-frequency noise of the INA333-Q1 is approximately 1 μV_{PP} measured from 0.1 Hz to 10 Hz (G = 100).

8.2.2.4 Input Bias Current Return Path

The input impedance of the INA333-Q1 is extremely high; approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically ±70 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 34 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA333-Q1, and the input amplifiers will saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 34). With higher source impedance, use two equal resistors to provide a balanced input with the possible advantages of a lower input offset voltage as a result of bias current, and improved high-frequency common-mode rejection.

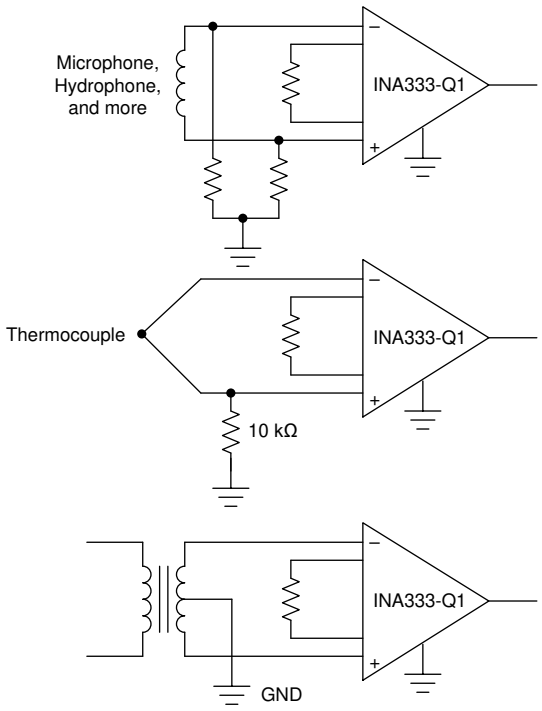


Figure 34. Providing an Input Common-Mode Current Path

ADVANCE INFORMATION

8.2.2.5 Low Voltage Operation

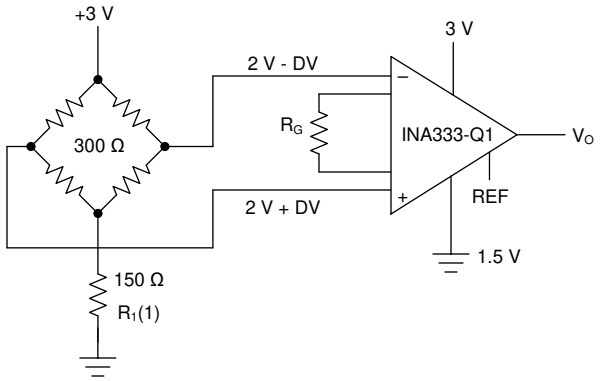
The INA333-Q1 can be operated on power supplies as low as ±0.9 V. Most parameters vary only slightly throughout this supply voltage range; see the *Typical Characteristics* section. Operation at very-low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. Figure 20 to Figure 23 show the range of linear operation for various supply voltages and gains.

8.2.2.6 Single-Supply Operation

The INA333-Q1 can be used on single power supplies of 1.8 V to 5.5 V. Figure 35 shows a basic single-supply circuit. The output REF pin is connected to midsupply. Zero differential input voltage demands an output voltage of midsupply. Actual output voltage swing is limited to approximately 50 mV more than ground, when the load is referred to ground, as shown. Figure 29 shows how the output voltage swing varies with output current.

With single-supply operation, V_{IN+} and $V_{IN–}$ must both be 0.1 V greater than ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

To show the issues affecting low voltage operation, consider the circuit in Figure 35 that shows the INA333-Q1 operating from a single 3-V supply. A resistor in series with the low side of the bridge makes sure that the bridge output voltage is within the common-mode range of the amplifier inputs.



(1) R_1 creates proper common-mode voltage, only for low-voltage operation; see the *Single-Supply Operation* section.

Figure 35. Single-Supply Bridge Amplifier

ADVANCE INFORMATION

8.2.3 Application Curves

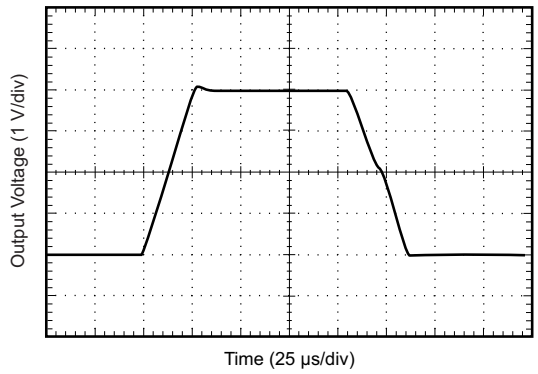


Figure 36. Large Signal Response

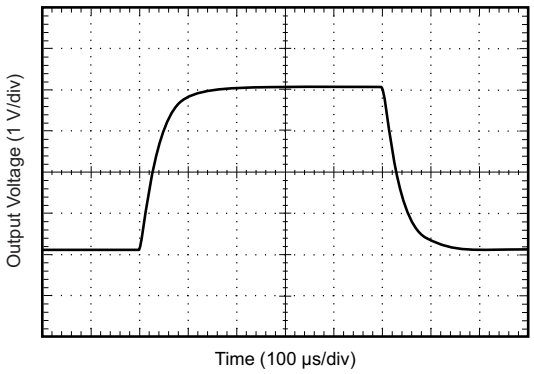


Figure 37. Large-Signal Step Response

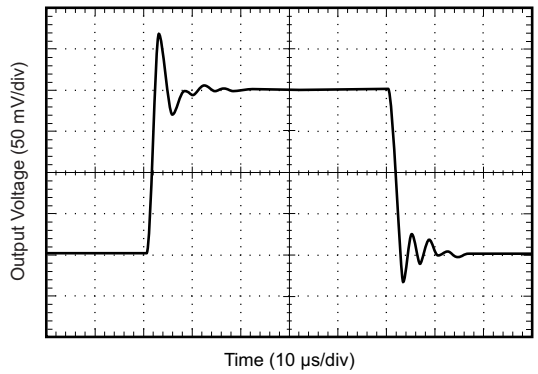


Figure 38. Small-Signal Step Response

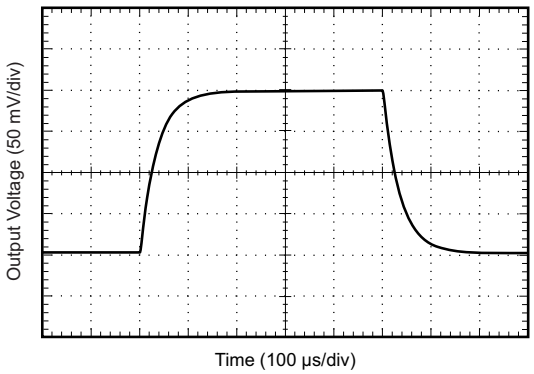


Figure 39. Small-Signal Step Response

ADVANCE INFORMATION

9 Power Supply Recommendations

The minimum power supply voltage for INA333-Q1 is 1.8 V, and the maximum power supply voltage is 5.5 V; for specified performance, 3.3 V to 5 V is recommended. Add a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10 Layout

10.1 Layout Guidelines

Attention to good layout practices is always recommended.

- Keep traces short.
- When possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible.
- Place a 0.1-μF bypass capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance, and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The INA333-Q1 has been specifically designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the V_{IN+} and $V_{IN–}$ inputs. As a result, the INA333-Q1 demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields may continue to cause varying offset levels, however, and may require additional shielding.

10.2 Layout Example

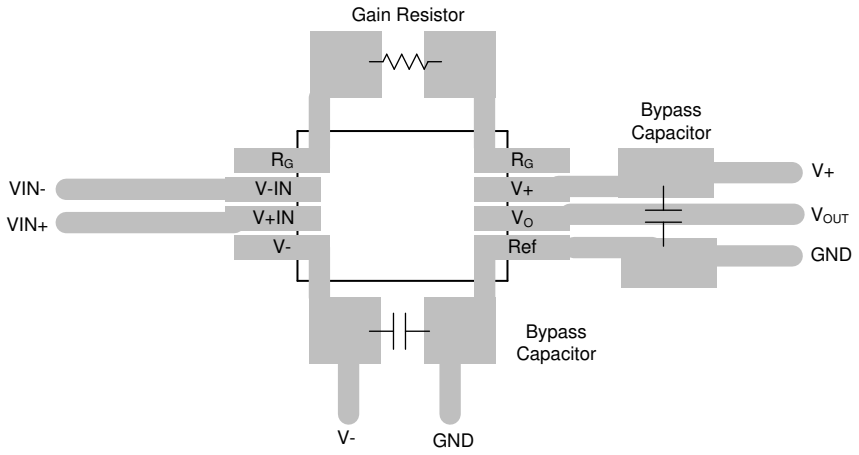


Figure 40. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI（免费下载软件）

TINA-TI 基于 SPICE 的模拟仿真程序（适用于 INA333）-Q1

TINA 是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。它提供所有传统的 SPICE 直流、瞬态和频域分析以及其他设计功能。

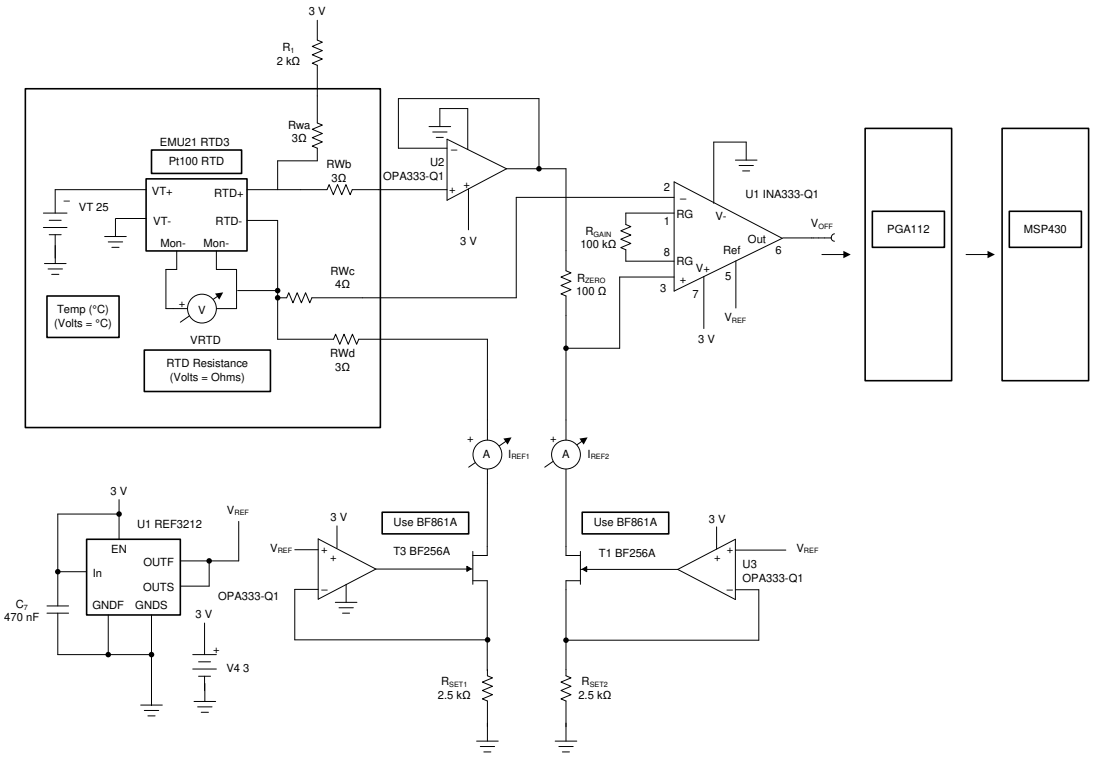
TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。

虚拟仪器为用户提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

图 41 显示了适用于 INA333-Q1 器件的示例 TINA-TI 电路，该电路可用于开发、修改和评估特定应用的电路 设计。下面给出了这些仿真文件的下载链接。

注

必须安装 TINA 软件（从 DesignSoft）或者 TINA-TI 软件后才能使用这些文件。请从 TINA-TI 文件夹中下载免费的 TINA-TI 软件。



RWa、RWb、RWc 和 RWd 用于仿真线电阻。包含这些电阻是为了展示四线传感技术对线不匹配问题的抗扰性。此方法假定使用四线 RTD。

图 41. 具有可编程增益采集系统的四线、3V PT100 RTD 调节器

通过以下链接下载该电路的 TINA-TI 仿真文件：*PT100 RTD*。

ADVANCE INFORMATION

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《OPA188-Q1 高精度、低噪声、轨至轨输出、36V、零漂移、汽车级运算放大器》数据表*
- 德州仪器 (TI)，*《OPA333-Q1 1.8V 微功耗 CMOS 运算放大器零漂移系列》数据表*
- 德州仪器 (TI)，*《电路板布局技巧》*

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

重要声明和免责声明

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA333QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	333Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

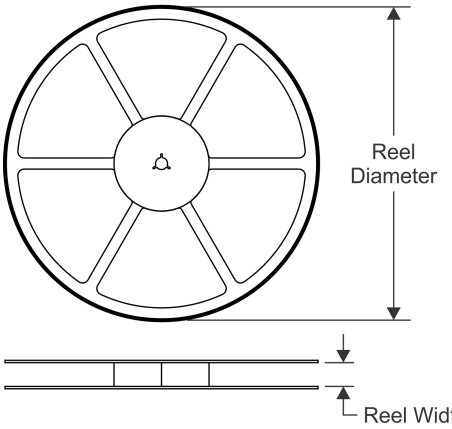
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

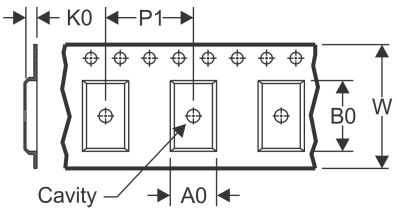
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

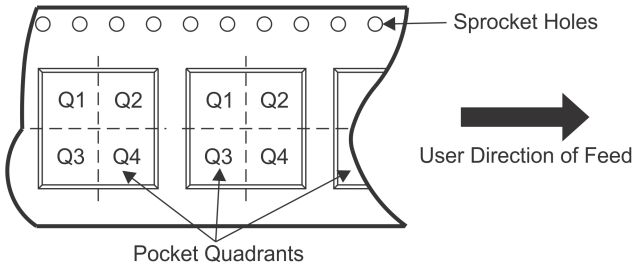


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

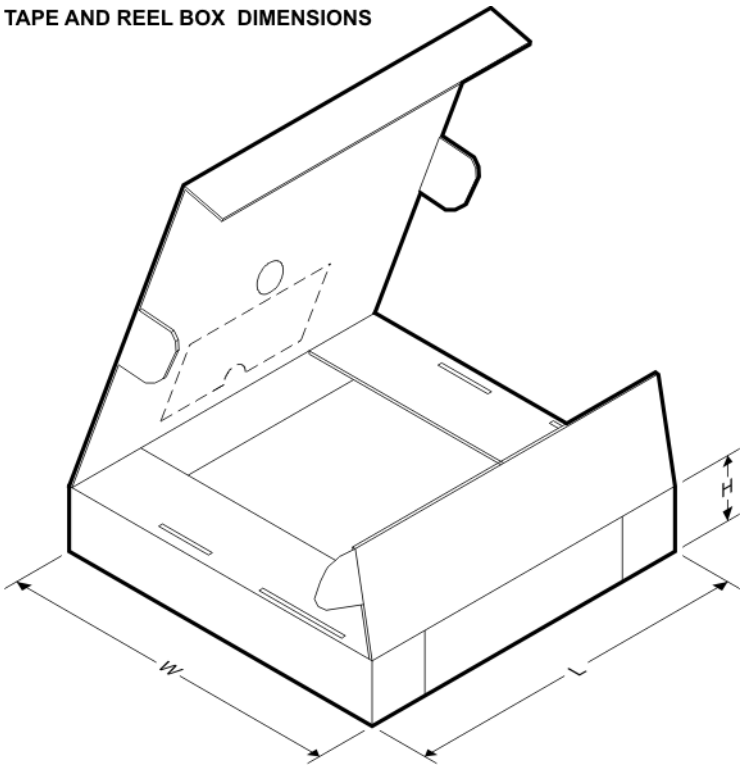
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA333QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

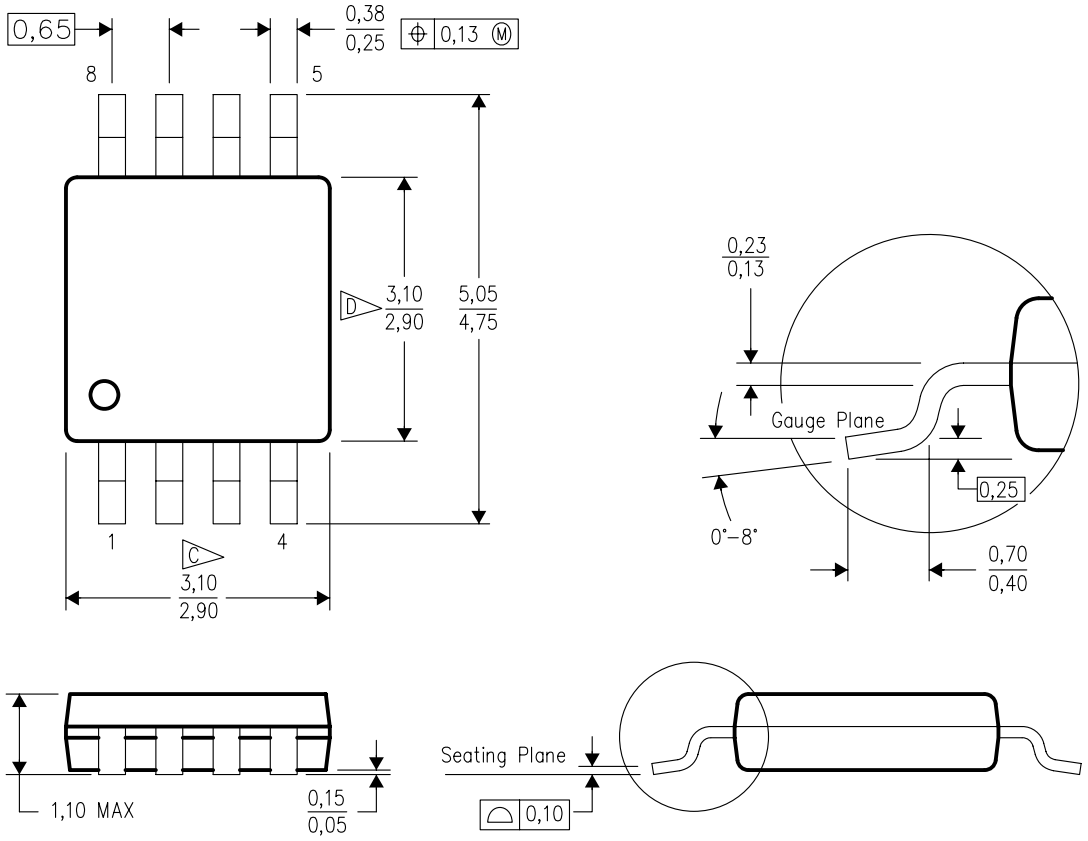
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA333QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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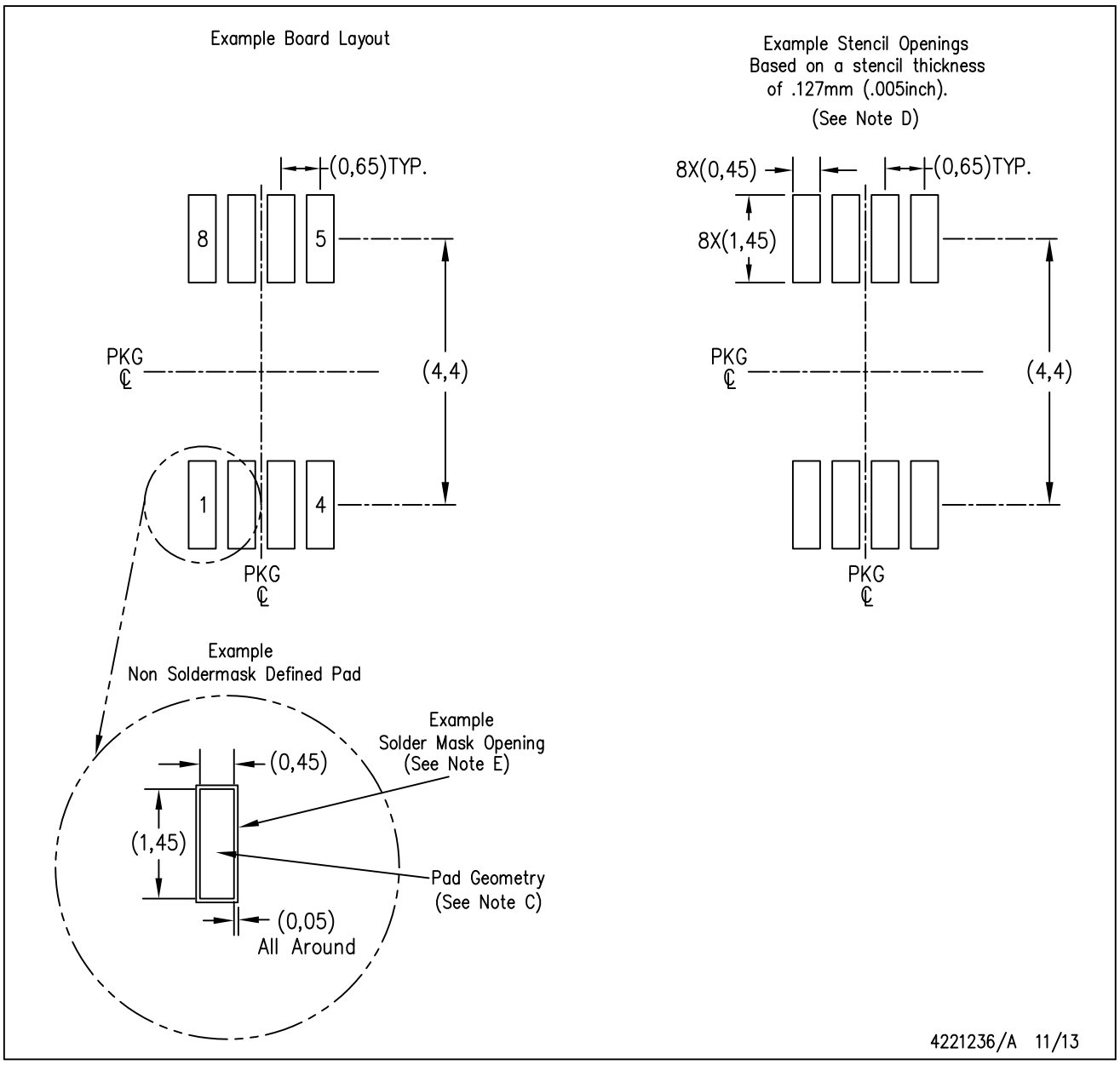
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122