

ISOUSB211 高速/全速/低速隔离式 USB 转发器

1 特性

- 符合 USB 2.0 要求
- 支持低速 (1.5 Mbps)、全速 (12 Mbps) 和高速 (480 Mbps) 信号传输
- 自动速度和连接检测
- 可编程均衡，用于补偿高速模式中的板迹线损耗
- 下游端 CDP 广播
- 对侧电源正常指示
- 支持自动角色交换
- 高 CMTI : 100 kV/μs
- V_{BUS} 电压范围：4.25 V 至 5.5 V
 - 3.3 V 和 1.8 V 内部 LDO
- 符合 CISPR32 B 类辐射限制
- 环境温度范围：-40°C 至 +125°C
- 小尺寸 28-SSOP 封装
- 安全相关认证：
 - 符合 DIN VDE V 0884-11 标准的 8000V_{PK} V_{IOTM} 和 2121V_{PK} V_{IORM} (增强型和基础型选项)
 - 符合 UL 1577 标准且长达 1 分钟的 5700V_{RMS} 隔离
 - IEC 62368-1、IEC 60601-1 和 IEC 61010-1 认证
 - CQC、TUV 和 CSA 认证
 - 所有认证已计划

2 应用

- USB 集线器、主机、外设和电缆隔离
- 医疗
- 工厂自动化
- 电机驱动器
- 电网基础设施
- 电力输送

增强型和基础型隔离选项

特性	ISOUSB211	ISOUSB211B
保护级别	增强型	基本型
浪涌测试电压	12800 V _{PK}	6000V _{PK}
隔离额定值	5700 V _{RMS}	3000 V _{RMS}
工作电压	1500V _{RMS} / 2121V _{PK}	1500V _{RMS} / 2121V _{PK}

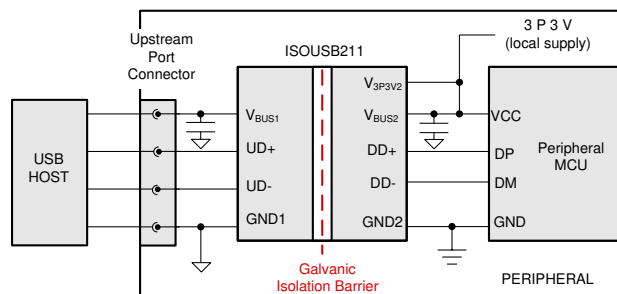
3 说明

ISOUSB211 是一款兼容 USB 2.0 的电气隔离式中继器，支持低速 (1.5Mbps)、全速 (12Mbps) 和高速 (480Mbps) 信号传输速率。该器件支持自动连接和速度检测、上拉/下拉反射以及链路电源管理，因而能够实现插入式 USB 集线器、主机、外设和电缆隔离。该器件还支持自动角色交换。如果连接断开后在上行端口上检测到新的连接，上行和下行端口定义将会调换。ISOUSB211 内置可编程的均衡功能，能够消除板迹线导致的信号损失，从而帮助满足 USB2.0 高速 TX 和 RX 眼图模板的要求。该器件采用二氧化硅 (SiO₂) 绝缘隔栅，可承受高达 5700V_{RMS} 的电压和 1500V_{RMS} 的工作电压。此器件与隔离式电源一同使用，可抵御高电压冲击，并防止总线的噪声电流进入局部接地层。ISOUSB211 器件提供基础型和增强型隔离 (请参阅 [增强型和基础型隔离选项](#))。该器件支持 -40°C 至 +125°C 的宽环境温度范围，并采用小尺寸 SSOP-28 (28-DP) 封装。

器件信息

器件型号 ⁽¹⁾	封装	封装尺寸 (标称值)
ISOUSB211	SSOP (28) DP	10.30mm × 7.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



应用示意图



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (November 2021) to Revision A (March 2022)	Page
• T _A Max value updated to 125°C.....	5
• Updated Thermal Considerations section.....	28

5 Pin Configuration and Functions

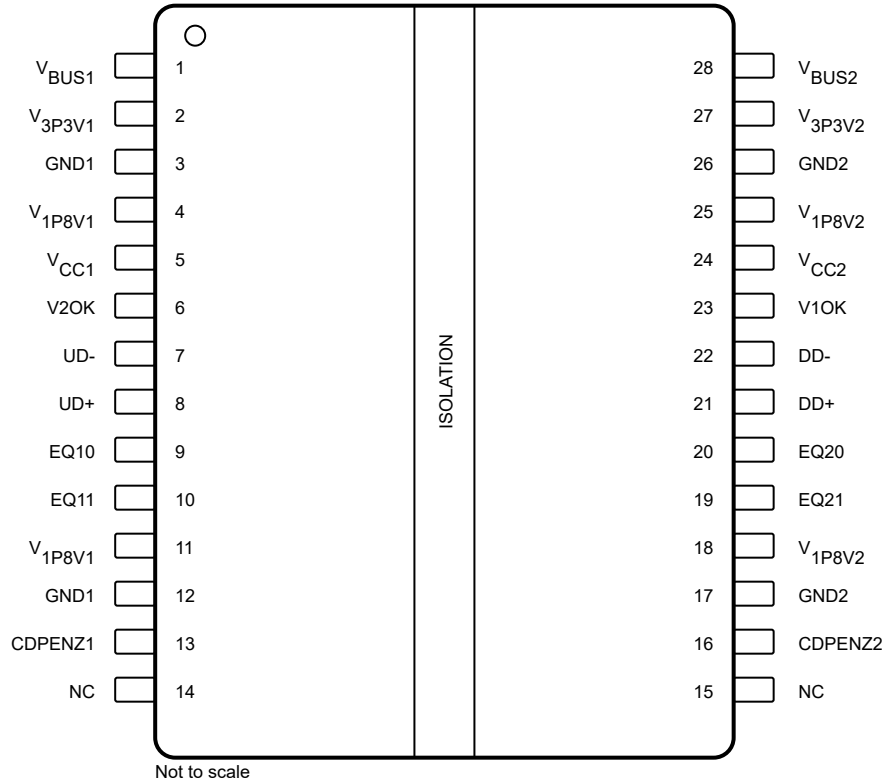


图 5-1. DP Package 28-Pin SSOP Top View

表 5-1. Pin Functions—28 Pins

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V _{BUS1}	—	Input Power Supply for Side 1. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V _{BUS1} . In this case an internal LDO generates V _{3P3V1} . Else, connect V _{BUS1} and V _{3P3V1} to an external 3.3 V power supply.
2	V _{3P3V1}	—	Power Supply for Side 1. If a 4.25 V to 5.5 V supply is connected to V _{BUS1} connect a bypass capacitor between V _{3P3V1} and GND1. In this case an internal LDO generates V _{3P3V1} . Else, connect V _{BUS1} and V _{3P3V1} to an external 3.3 V power supply.
3	GND1	—	Ground 1. Ground reference for Isolator Side 1.
4	V _{1P8V1}	—	Power Supply for Side 1. If a 2.35 V to 5.5 V supply is connected to V _{CC1} connect a bypass capacitor between V _{1P8V1} and GND1. In this case an internal LDO generates V _{1P8V1} . Else, connect V _{CC1} and V _{1P8V1} to an external 1.8 V power supply.
5	V _{CC1}	—	Input Power Supply for Side 1. If a 2.35 V to 5.5 V (example USB power bus, or a DC-DC supply derived from USB power bus) supply is available connect it to V _{CC1} . In this case an internal LDO generates V _{1P8V1} . Else, connect V _{CC1} and V _{1P8V1} to an external 1.8 V power supply.
6	V2OK	O	High level on this pin indicates that side 2 is powered up.
7	UD-	I/O	Upstream facing port D-.
8	UD+	I/O	Upstream facing port D+.
9	EQ10	I	Equalization setting for Side 1, LSB. Logic Input.
10	EQ11	I	Equalization setting for Side 1, MSB. Logic Input.
11	V _{1P8V1}	—	Connect pin 11 to pin 4, with local bypass capacitors near pin 11.
12	GND1	—	Ground 1. Ground reference for Isolator Side 1.
13	CDPENZ1	I	Active low singal. Enables CDP advertising on UD+/UD- pins.
14	NC	—	Leave floating or connect to V _{3P3V1} .

表 5-1. Pin Functions—28 Pins (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
15	NC	—	Leave floating or connect to V_{3P3V2} .
16	CDPENZ2	I	Active low signal. Enables CDP advertising on DD+/DD- pins.
17	GND2	—	Ground 2. Ground reference for Isolator Side 2.
18	V_{1P8V2}	—	Connect pin 18 to pin 25, with local bypass capacitors near pin 18.
19	EQ21	I	Equalization setting for Side 2, MSB. Logic Input.
20	EQ20	I	Equalization setting for Side 2, LSB. Logic Input.
21	DD+	I/O	Downstream facing port D+.
22	DD-	I/O	Downstream facing port D-.
23	V1OK	O	High level on this pin indicates that side 1 is powered up.
24	V_{CC2}	—	Input Power Supply for Side 2. If a 2.35 V to 5.5 V (example USB power bus, or a DC-DC supply derived from USB power bus) supply is available connect it to V_{CC2} . In this case an internal LDO generates V_{1P8V2} . Else, connect V_{CC2} and V_{1P8V2} to an external 1.8 V power supply.
25	V_{1P8V2}	—	Power Supply for Side 1. If a 2.35 V to 5.5 V supply is connected to V_{CC2} connect a bypass capacitor between V_{1P8V2} and GND2. In this case an internal LDO generates V_{1P8V2} . Else, connect V_{CC2} and V_{1P8V2} to an external 1.8 V power supply.
26	GND2	—	Ground 2. Ground reference for Isolator Side 2.
27	V_{3P3V2}	—	Power Supply for Side 2. If a 4.25 V to 5.5 V supply is connected to V_{BUS2} connect a bypass capacitor between V_{3P3V2} and GND1. In this case an internal LDO generates V_{3P3V2} . Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.
28	V_{BUS2}	—	Input Power Supply for Side 2. If a 4.25 V to 5.5 V (example USB power bus) supply is available connect it to V_{BUS2} . In this case an internal LDO generates V_{3P3V2} . Else, connect V_{BUS2} and V_{3P3V2} to an external 3.3 V power supply.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{BUS1} , V _{BUS2}	V _{BUS} supply voltage	-0.3	6	V
V _{CC1} , V _{CC2}	V _{CC} supply voltage	-0.3	6	V
V _{3P3V1} , V _{3P3V2}	3.3-V input supply voltage	-0.3	4.25	V
V _{1P8V1} , V _{1P8V2}	1.8-V input supply voltage	-0.3	2.1	V
V _{DPDM}	Voltage on bus pins (UD+, UD-, DD+, DD-) 1000 total number of short events and cumulative duration of 1000 hrs.	-0.3	6	V
V _{IO}	IO voltage range (V*OK, EQ*, CDPENZ*)	-0.3	V _{3P3Vx} +0.3 ⁽³⁾	V
I _O	Output current on output pins (V*OK)	-10	10	mA
T _J	Junction temperature		150	°C
T _{STG}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 4.25 V

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±1500	V
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{BUSx}	V _{BUS} input voltage (inclusive of any ripple)	4.25	5	5.5	V
V _{3P3Vx}	3.3-V input supply voltage (inclusive of any ripple)	3.0	3.3	3.6	V
V _{CCx}	Input voltage to internal 1.8V LDO (inclusive of any ripple)	2.4	3	5.5	V
V _{1P8Vx}	1.8-V input supply voltage (inclusive of any ripple)	1.71	1.8	1.94	V
T _A	Operating free-air temperature	-40		125	°C
T _J	Junction temperature	-55		150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISOUSB211	
		DP (SSOP)	
		28 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISOUSB211						
P_D	Maximum power dissipation (both sides)	$V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $R_L = 50\ \Omega$ each on DD- and DD+ to GNDx, input a 240-MHz 50% duty cycle adifferential 0 to 400mV swing signal on UD- and UD+			1232	mW
P_{D1}	Maximum power dissipation (side-1)	$V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $R_L = 50\ \Omega$ each on DD- and DD+ to GNDx, input a 240-MHz 50% duty cycle adifferential 0 to 400mV swing signal on UD- and UD+			616	mW
P_{D2}	Maximum power dissipation (side-2)	$V_{BUS1} = V_{BUS2} = V_{CC1} = V_{CC2} = 5.5\text{ V}$, $T_J = 150^\circ\text{C}$, $R_L = 50\ \Omega$ each on DD- and DD+ to GNDx, input a 240-MHz 50% duty cycle adifferential 0 to 400mV swing signal on UD- and UD+			616	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFIC ACTIONS	UNIT
			DP-28	
IEC 60664-1				
CLR	External clearance ⁽¹⁾	Side 1 to side 2 distance through air	>8	mm
CPG	External Creepage ⁽¹⁾	Side 1 to side 2 distance across package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	μm
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN VDE V 0884-11:2017-01⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V _{PK}
V _{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (Tddb) test;	1500	V _{RMS}
		DC voltage	2121	V _{DC}
V _{IOTM}	Maximum transient isolation voltage ISOUSB211	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production)	8000	V _{PK}
	Maximum transient isolation voltage ISOUSB211B		4242	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ISOUSB211 ⁽³⁾	Test method per IEC 62368-1, 1.2/50 ms waveform, V _{TEST} = 1.6 × V _{IOSM} = 12800 V _{PK} (qualification)	8000	V _{PK}
	Maximum surge isolation voltage ISOUSB211B ⁽³⁾	Test method per IEC 62368-1, 1.2/50 ms waveform, V _{TEST} = 1.3 × V _{IOSM} = 6000 V _{PK} (qualification)	4615	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; ISOUSB211: V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s; ISOUSB211B: V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s; ISOUSB211: V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s; ISOUSB211B: V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 × sin (2 pft), f = 1 MHz	1	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	> 10 ¹²	W
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Withstand isolation voltage, ISOUSB211	V _{TEST} = V _{ISO} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production)	5700	V _{RMS}
	Withstand isolation voltage, ISOUSB211B		3000	V _{RMS}

- Care must be taken during board design so that the mounting pads of the isolator on the printed-circuit board (PCB) do not reduce creepage and clearance. Inserting grooves, ribs or both can help increase creepage distance on the PCB.
- ISOUSB211 is suitable for safe electrical insulation and ISOUSB211B is suitable for basic electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- Apparent charge is electrical discharge caused by a partial discharge (pd).
- All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Plan to certify according to DIN VDE V 0884-11:2017-01	Plan to certify according to IEC 61010-1, IEC 62368-1 and IEC 60601-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1-2011	Plan to certify according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014
Maximum transient isolation voltage, ISOUSB211: 8000 V _{PK} ISOUSB211B: 4242 V _{PK} Maximum repetitive peak isolation voltage, 2121 V _{PK} ; Maximum surge isolation voltage, ISOUSB211: 8000 V _{PK} (Reinforced) ISOUSB211B: 4615 V _{PK} (Basic)	IEC 62368-1 2nd Ed., for pollution degree 2, material group I ISOUSB211: 800 V _{RMS} reinforced isolation ISOUSB211B: 1000 V _{RMS} basic isolation ----- CSA 60601- 1:14 and IEC 60601-1 Ed. 3.1+A1 ISOUSB211: 2 MOPP (Means of Patient Protection) 250 V _{RMS} (354 V _{PK}) maximum working voltage	Single protection, ISOUSB211: 5700 V _{RMS} ISOUSB211B: 3000 V _{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage	EN 61010-1:2010/A1:2019 ISOUSB211: 600 V _{RMS} reinforced isolation ISOUSB211B: 1000 V _{RMS} basic isolation ----- EN 62368-1:2014 ISOUSB211: 800 V _{RMS} reinforced isolation ISOUSB211B: 1000 V _{RMS} basic isolation
Certificate planned	Certificate planned	Certificate planned	Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DP-28 PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 51°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C			445	mA
		R _{θJA} = 51°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C			680	mA
P _S	Safety input, output, or total power	R _{θJA} = 51°C/W, T _J = 150°C, T _A = 25°C			2450	mW
T _S	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
 The junction-to-air thermal resistance, R_{θJA}, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
 $T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where T_{J(max)} is the maximum allowed junction temperature.
 $P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSx}} = 5\text{ V}$, $V_{3\text{P3Vx}} = 3.3\text{ V}$, $V_{1\text{P8Vx}} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - High Speed (HS) mode	Receive side HS Active (240 MHz signal rate), $\text{EQxx} = 00$, $R_L = 45\ \Omega$ to ground on D+ and D-		10.5	13.5	mA
		Transmit side HS Active (240 MHz signal rate), $\text{EQxx} = 00$, $R_L = 45\ \Omega$ to ground on D+ and D-		10.5	13.5	mA
		HS Idle State, $\text{EQxx} = 00$, $R_L = 45\ \Omega$ to ground on D+ and D-		10.5	13.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6 MHz signal rate), Figure 7-9, $C_L = 50\ \text{pF}$		11.5	14.8	mA
		Transmit side FS Active (6 MHz signal rate), Figure 7-9, $C_L = 50\ \text{pF}$		9.5	13	mA
		Receive side LS Active (750 kHz signal rate), Figure 7-10, $C_L = 450\ \text{pF}$		9.5	13	mA
		Transmit side LS Active (750 kHz signal rate), Figure 7-10, $C_L = 450\ \text{pF}$		9.5	13	mA
		FS/LS Idle State (US side or DS side)		7.4	9.8	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - L1 Sleep mode	Upstream Facing side		7.5	9.8	mA
		Downstream Facing side		7.3	9.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - L2 Suspend mode	Upstream Facing side		1.5	2.05	mA
		Downstream Facing side		5.6	7.5	mA
I_{VBUSx} or I_{V3P3Vx}	V_{BUS} or $V_{3\text{P3V}}$ current consumption - Not attached	Upstream Facing side		6.2	8.5	mA
		Downstream Facing side		6.2	8.9	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - High Speed (HS) mode	Receive side HS Active (240 MHz signal rate), $\text{EQxx} = 00$, $R_L = 45\ \Omega$ to ground on D+ and D-		80	96	mA
		Transmit side HS Active (240 MHz signal rate), $\text{EQxx} = 00$, $R_L = 45\ \Omega$ to ground on D+ and D-		80	96	mA
		HS Idle State, $\text{EQxx} = 00$, $R_L = 45\ \Omega$ to ground on D+ and D-		74	90	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - Full Speed (FS) and Low Speed (LS) modes	Receive side FS Active (6 MHz signal rate), Figure 7-9, $C_L = 50\ \text{pF}$		0.08	0.2	mA
		Transmit side FS Active (6 MHz signal rate), Figure 7-9, $C_L = 50\ \text{pF}$		0.08	0.2	mA
		Receive side LS Active (750 kHz signal rate), Figure 7-10, $C_L = 450\ \text{pF}$		0.08	0.2	mA
		Transmit side LS Active (750 kHz signal rate), Figure 7-10, $C_L = 450\ \text{pF}$		0.08	0.2	mA
		FS/LS Idle State		0.08	0.2	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - L1 Sleep mode	Upstream Facing side		0.08	0.2	mA
		Downstream Facing side		0.08	0.2	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - L2 Suspend mode	Upstream Facing side		0.25	0.45	mA
		Downstream Facing side		0.25	0.45	mA
I_{VCCx} or I_{V1P8Vx}	I_{VCCx} or I_{V1P8Vx} current consumption - Not attached	Upstream Facing side		0.08	0.2	mA
		Downstream Facing side		0.08	0.2	mA
$\text{UV}^+(\text{VBUSx})$ ⁽¹⁾	Under voltage threshold when supply voltage is rising, V_{BUS}				4.0	V

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 Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSx}} = 5\text{ V}$, $V_{3\text{P}3\text{Vx}} = 3.3\text{ V}$, $V_{1\text{P}8\text{Vx}} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UV_{-(V_{\text{BUSx}})}$ (1)	Under voltage threshold when supply voltage is falling, V_{BUS}		3.6			V
$UVHYS_{(V_{\text{BUSx}})}$ (1)	Under voltage threshold hysteresis, V_{BUS}			0.08		V
$UV_{+(V_{3\text{P}3\text{Vx}})}$	Under voltage threshold when supply voltage is rising, $V_{3\text{P}3\text{V}}$				2.95	V
$UV_{-(V_{3\text{P}3\text{Vx}})}$	Under voltage threshold when supply voltage is falling, $V_{3\text{P}3\text{V}}$		1.95			V
$UVHYS_{(V_{3\text{P}3\text{Vx}})}$	Under voltage threshold hysteresis, $V_{3\text{P}3\text{V}}$			0.11		V
$UV_{+(V_{\text{CCx}})}$ (2)	Under voltage threshold when supply voltage is rising, V_{CC}				2.35	V
$UV_{-(V_{\text{CCx}})}$ (2)	Under voltage threshold when supply voltage is falling, V_{CC}		2			V
$UVHYS_{(V_{\text{CCx}})}$ (2)	Under voltage threshold hysteresis, V_{CC}			0.05		V
$UV_{+(V_{1\text{P}8\text{Vx}})}$	Under voltage threshold when supply voltage is rising, $V_{1\text{P}8\text{V}}$				1.66	V
$UV_{-(V_{1\text{P}8\text{Vx}})}$	Under voltage threshold when supply voltage is falling, $V_{1\text{P}8\text{V}}$		1.25			V
$UVHYS_{(V_{1\text{P}8\text{Vx}})}$	Under voltage threshold hysteresis, $V_{1\text{P}8\text{V}}$			0.05		V
DIGITAL INPUTS						
V_{IH}	High-level input voltage		0.7 x $V_{3\text{P}3\text{Vx}}$			V
V_{IL}	Low-level input voltage				0.3 x $V_{3\text{P}3\text{Vx}}$	V
V_{IHYS}	Input transition threshold hysteresis		0.3			V
I_{IH}	High-level input current				1	μA
I_{IL}	Low-level input current				10	μA
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	$I_{\text{O}} = -3\text{ mA}$ for $3.0\text{ V} \leq V_{3\text{P}3\text{Vx}} \leq 3.6\text{ V}$	$V_{3\text{P}3\text{Vx}} - 0.2$			V
V_{OL}	Low-level output voltage	$I_{\text{O}} = 3\text{ mA}$ for $3.0\text{ V} \leq V_{3\text{P}3\text{Vx}} \leq 3.6\text{ V}$			0.2	V
UDx, DDx, INPUT CAPACITANCE AND TERMINATION						
$Z_{\text{INP}_x\text{Dx}}$	Impedance to GND, no pull up/down	$V_{\text{in}}=3.6\text{ V}$, $V_{3\text{P}3\text{Vx}}=3.0\text{ V}$, $T_{\text{J}} < 125^\circ\text{C}$, USB 2.0 Spec Section 7.1.6	300			k Ω
$C_{\text{IO}_x\text{Dx}}$	Capacitance to GND	Measured with VNA at 240MHz, Driver Hi-Z			10	pF
R_{PUI}	Bus Pull up Resistor on Upstream Facing Port (idle)	USB 2.0 Spec Section 7.1.5	0.9	1.1	1.575	k Ω
R_{PUR}	Bus Pull up Resistor on Upstream Facing Port (receiving)	USB 2.0 Spec Section 7.1.5	1.5	2.2	3	k Ω
R_{PD}	Bus Pull-down Resistor on Downstream Facing Port	USB 2.0 Spec Section 7.1.5	14.25	19	24.8	k Ω
V_{TERM}	Termination voltage for Upstream facing port pullup (RPU)	USB 2.0 Spec Section 7.1.5, measured on D+ or D- with pull up enabled on upstream port with external load disconnected.	3		3.6	V
V_{HSTERM}	Termination voltage in high speed	USB 2.0 Spec Section 7.1.6.2, The output voltage in the high-speed idle state	- 10		10	mV

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{BUSx} = 5\text{ V}$, $V_{3P3Vx} = 3.3\text{ V}$, $V_{1P8Vx} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z _{HSTERM}	Driver Output Resistance (which also serves as high-speed termination)	(VOH= 0 to 600mV) USB 2.0 Spec Section 7.1.1.1 and Figure 7-5.	40.5	45	49.5	Ω
UDx, DDx, INPUT LEVELS LS/FS						
V _{IH}	High (driven)	USB 2.0 Spec Section 7.1.4 (measured at connector)	2			V
V _{IHZ}	High (floating)	USB 2.0 Spec Section 7.1.4 (Host downstream port pull down resistor enabled and Device pulled up to 3.0 V - 3.6 V).	2.7		3.6	V
V _{IL}	Low	USB 2.0 Spec Section 7.1.4			0.8	V
V _{DI}	Differential Input Sensitivity	(xD+)-(xD-) ; USB 2.0 Spec Figure 7-19; (measured at connector)	0.2			V
V _{LSFS_HYS}	Differential Input Hysteresis FS/LS	(xD+)-(xD-) ; (measured at connector) V _{CM} = 0.8 V to 2.0 V	25	75	245	mV
V _{CM}	Common Mode Range	Includes VDI range; USB 2.0 Spec Figure 7-19; (measured at connector)	0.8		2.5	V
UDx, DDx, OUTPUT LEVELS LS/FS						
V _{OL}	Low	USB 2.0 Spec Section 7.1.1, (measured at connector with RL of 0.9 kΩ to 3.6 V.)	0		0.3	V
V _{OH}	High (Driven)	USB 2.0 Spec Section 7.1.1 (measured at connector with RL of 14.25 kΩ to GND.)	2.8		3.6	V
V _{OSE1}	SE1	USB 2.0 Spec Section 7.1.1	0.8			V
Z _{FSTERM}	Driver Series Output Resistance	USB 2.0 Spec Section 7.1.1 and Figure 7-4, Measured during VOL or VOH	28		44	Ω
V _{CRS}	Output Signal Crossover Voltage	Measured as in USB 2.0 Spec Section 7.1.1 Figures 7-8, 7-9 and 7-10; Excluding the first transition from the Idle state	1.3		2	V
UDx, DDx, INPUT LEVELS HS						
V _{HSSQ}	High-speed squelch/no-squelch detection threshold	USB 2.0 Spec Section 7.1.7.2 (specification refers to peak differential signal amplitude), measured at 240MHz with increasing amplitude, V _{CM} =-50mV to 500mV	100	116	150	mV
V _{HSDSC}	High-speed disconnect detection threshold _{HSDC} typical values	USB 2.0 Spec Section 7.1.7.2 (specification refers to differential signal amplitude). V _{CM} = -50 mV to 500 mV	525	575	625	mV
V _{CHIRP_TH}	Chirp detection threshold	Chirp detection threshold (measured as peak differential signal amplitude). V _{CM} = -50 mV to 500 mV	100	215	365	mV
V _{HSRX}	High-speed differential input signaling levels data sensitivity	Peak-to-peak at 240 MHz			100	mV
V _{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	USB 2.0 Spec Section 7.1.4.2, receiver should be able to receive with this common mode range	- 50	200	500	mV
UDx, DDx, OUTPUT LEVELS HS						
V _{HSDH}	High-speed data signaling high	USB 2.0 Spec Section 7.1.7.2, measured single ended peak voltage per USB 2.0 test measurement spec, EQxx = 00, Test load is an ideal 45 Ω to GND on D+ and D-	360	400	440	mV

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSx}} = 5\text{ V}$, $V_{3\text{P3Vx}} = 3.3\text{ V}$, $V_{1\text{P8Vx}} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HSOL}	High-speed data signaling low	USB 2.0 Spec Section 7.1.7.2, measured single ended peak voltage per USB 2.0 test measurement spec, EQxx = 00, Test load is an ideal $45\ \Omega$ to GND on D+ and D-.	- 10		10	mV
V_{HSOI}	High-speed data signaling idle, driver is off termination is on (measured single ended)	USB 2.0 Spec Section 7.1.7.2, PE disabled, Test load is an ideal $45\ \Omega$ to GND on D+ and D-.	- 10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load is an ideal $45\ \Omega$ to GND on D+ and D-, with $1.5\text{ k}\Omega$ pull-up to 3.3 V on D+.	700	900	1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)	USB 2.0 Spec Section 7.1.7.2, EQxx = 00, Test load is an ideal $45\ \Omega$ to GND on D+ and D-, with $1.5\text{ k}\Omega$ pull-up to 3.3 V on D+.	- 900	- 700	- 500	mV
$U2_TX_{\text{CM}}$	High-speed TX DC Common Mode	Test load is an ideal $45\ \Omega$ to GND on D+ and D-.	- 50	200	500	mV
EQUALIZATION AND PRE-EMPHASIS						
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=low, 240MHz	-0.24	0.46	0.75	dB
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=float, 240MHz	0.27	0.98	1.5	dB
EQ_{HS}	High-speed RX Equalization	EQ1=low, EQ0=high, 240MHz	0.70	1.50	2.2	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=low, 240MHz	1.04	2.00	2.81	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=float, 240MHz	1.45	2.68	3.8	dB
EQ_{HS}	High-speed RX Equalization	EQ1=float, EQ0=high, 240MHz	1.73	3.09	4.4	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=low, 240MHz	2.00	3.46	4.7	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=float, 240MHz	2.25	3.80	5.1	dB
EQ_{HS}	High-speed RX Equalization	EQ1=high, EQ0=high, 240MHz	2.25	3.80	5.1	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=low, 240MHz	0.25	0.48	0.75	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=float, 240MHz	0.62	0.9	1.2	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=low, EQ0=high, 240MHz	0.89	1.36	1.5	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=low, 240MHz	1.4	1.7	2.0	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=float, 240MHz	1.7	2.1	2.5	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=float, EQ0=high, 240MHz	2.1	2.5	2.9	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=low, 240MHz	2.7	3.2	3.7	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=float, 240MHz	3.4	4.0	4.6	dB
PE_{HS}	High-speed TX Pre-emphasis	EQ1=high, EQ0=high, 240MHz	3.4	4.0	4.6	dB
CDP						
$V_{\text{DM_SRC}}$	VDM_SRC Voltage	Load Current in the range of 0 to 250 μA	0.5		0.7	V
$I_{\text{DP_SINK}}$	IDP_SINK (D+)	D+ Voltage = 0 V to 0.7 V	25		175	μA
$V_{\text{DAT_REF+}}$	VDAT_REF comparator rising threshold		300		400	mV
$V_{\text{DAT_REF-}}$	VDAT_REF comparator falling threshold		300		400	mV
$V_{\text{DAT_REF_HYS}}$	VDAT_REF comparator hysteresis		15	20	25	mV
THERMAL SHUTDOWN						
TSD+	Thermal shutdown turn-on temperature		160	170	180	$^\circ\text{C}$
TSD-	Thermal shutdown turn-off temperature		150	160	170	$^\circ\text{C}$

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSx}} = 5\text{ V}$, $V_{3\text{P3Vx}} = 3.3\text{ V}$, $V_{1\text{P8Vx}} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD _{HYS}	Thermal shutdown hysteresis			10		°C

- (1) If V_{BUSx} pins are externally connected to the corresponding $V_{3\text{P3Vx}}$ pins, then UVLO thresholds on V_{BUSx} are governed by $UV^+_{(V3P3Vx)}$, $UV^-_{(V3P3Vx)}$ and $UVHYS_{(V3P3Vx)}$
- (2) If V_{CCx} pins are externally connected to the corresponding $V_{1\text{P8Vx}}$ pins, then UVLO thresholds on V_{CCx} are governed by $UV^+_{(V1P8Vx)}$, $UV^-_{(V1P8Vx)}$ and $UVHYS_{(V1P8Vx)}$

6.10 Switching Characteristics

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSx}} = 5\text{ V}$, $V_{3\text{P3Vx}} = 3.3\text{ V}$, $V_{1\text{P8Vx}} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-UP TIMING						
T_{SUPRAMP}	Allowed power supply ramp-up times on V_{BUSx} , $V_{3\text{P3Vx}}$, V_{CCx} and $V_{1\text{P8Vx}}$ external power supplies		0.005		100	ms
T_{PWRUP}	Time taken for the device to power up, and recognize USB signaling, after valid power supply is provided on both side 1 and side 2.	All external power supplies are ramped up together with $5\ \mu\text{s}$ power up time.		5	10	ms
UDx, DDx, HS Driver Switching Characteristics						
T_{HSR}	Rise Time (10% - 90%)	USB 2.0 Spec Section 7.1.2, ideal $45\ \Omega$ to GND loads on D+ and D-, $\text{EQxx} = 00$	429	450	528	ps
T_{HSF}	Fall Time (10% - 90%)	USB 2.0 Spec Section 7.1.2, ideal $45\ \Omega$ to GND loads on D+ and D-, $\text{EQxx} = 00$	426	443	526	ps
UDx, DDx, FS Driver Switching Characteristics						
T_{FR}	Rise Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, $C_L = 50\ \text{pF}$	4		20	ns
T_{FF}	Fall Time (10% - 90%)	USB 2.0 Spec Figure 7-8, Figure 7-9, $C_L = 50\ \text{pF}$	4		20	ns
T_{FRFM}	Differential Rise and Fall Time Matching ($T_{\text{FR}}/T_{\text{FM}}$)	USB 2.0 Spec 7.1.2, Excluding the first transition from the Idle state, Figure 7-9, $C_L = 50\ \text{pF}$	90		111.1	%
UDx, DDx, LS Driver Switching Characteristics						
T_{LR}	Rise Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range $50\ \text{pF}$ to $600\ \text{pF}$.	75		300	ns
T_{LF}	Fall Time (10% - 90%)	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range $50\ \text{pF}$ to $600\ \text{pF}$.	75		300	ns
T_{LRFM}	Rise and Fall Time Matching (TLR/TFM), Excluding first transition from idle state.	USB 2.0 Spec Figures 7-8 and 7-10, with C_L range $50\ \text{pF}$ to $600\ \text{pF}$.	80		125	%
REPEATER TIMING - CONNECT, DISCONNECT, RESET, L1, L2						
T_{FILTCNN}	Debounce filter on FS or LS Connect Detection		45	70	80	μs
T_{DDIS}	Time to detect disconnect at the DS facing port in LS/FS L0 mode.		2		7	μs
T_{DETRST}	Time taken to detect reset on US port in LS/FS L0 mode		0		7	μs
$T_{2\text{SUSP}}$	Time taken by the US side to detect suspend mode (L2) and draw less than $2.5\ \text{mA}$ current when bus is continuously in idle state.		3		10	ms
$t_{\text{DRESUMEL1}}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from sleep/L1 state.				1	μs
$t_{\text{DRESUMEL2}}$	Maximum time to detect resume on the US and reflect/drive resume on the DS port from suspend/L2 state.				130	μs
t_{DWAKEL1}	Maximum time to detect and propagate remote wake when in sleep/L1 state.				5	μs
t_{DWAKEL2}	Maximum pulse width of remote wake that is guaranteed to be detected when in suspend/L2 state.				900	μs

Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSX}} = 5\text{ V}$, $V_{3\text{P3VX}} = 3.3\text{ V}$, $V_{1\text{P8VX}} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DRSMPROP}	Minimum duration of resume driven upstream and downstream after detecting remote wake when in suspend/L2 state.		1			ms
CMTI	Common mode transient immunity	$V_{\text{CM}} = 1200\text{ VPK}$	75	100		kV/ μs
REPEATER TIMING - LS, FS						
T_{LSDD}	Low-speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			358	ns
T_{LSOP}	LS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-20		20	ns
T_{LSJP}	LS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-2		2	ns
T_{LSJN}	LS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-7.0		7.0	ns
T_{LST}	Minimum width of SE0 interval during LS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	210			ns
T_{LEOPD}	Repeater EOP delay relative to T_{LSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		200	ns
T_{LESK}	SE0 skew caused by the repeater during LS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-100		100	ns
T_{FSDD}	Full-Speed Differential Data Propagation Delay	USB 2.0 spec section 7.1.14. Figure 7-52(C).			70	ns
T_{FSOP}	FS Data bit-width distortion after SOP	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-10		10	ns
T_{FSJP}	FS repeater additive jitter - paired transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-2		2	ns
T_{FSJN}	FS repeater additive jitter - next transition	USB 2.0 spec section 7.1.14. Figure 7-52(C).	-6.0		6.0	ns
T_{FST}	Minimum width of SE0 interval during FS differential transition - filtered out by the repeater	USB 2.0 spec section 7.1.4.	14			ns
T_{FEOPD}	Repeater EOP delay relative to T_{FSDD}	USB 2.0 spec section 7.1.14. Figure 7-53(C).	0		17	ns
T_{FESK}	SE0 skew caused by the repeater during FS EOP	USB 2.0 spec section 7.1.14. Figure 7-53(C).	-15		15	ns
REPEATER TIMING - HS						
T_{HSSOPT}	High-speed Start of Packet Truncation	USB 2.0 spec, section 7.1.10.		6	8	UI
T_{HSEOPD}	High-speed End of Packet Dribble	USB 2.0 spec, section 7.1.13.		7	8	UI
T_{HSPD}	High-speed Propagation Delay	USB 2.0 spec, section 7.1.14.	2	3	4	ns
T_{HSTJ}	High-speed total additive jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), RX EQ disabled, TX PE disabled.				120	ps
T_{HSRJ}	High-speed additive random jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), RX EQ disabled, TX PE disabled.				35	ps
T_{HSDJ}	High-speed additive deterministic jitter (output jitter - input jitter) of repeater (includes all complete SOP bits), RX EQ disabled, TX PE disabled.				82	ps

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Over recommended operating conditions (unless otherwise noted). All typical values are at $T_A = 25^\circ\text{C}$, $V_{\text{BUSX}} = 5\text{ V}$, $V_{3P3VX} = 3.3\text{ V}$, $V_{1P8VX} = 1.8\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{HSDIS}	Time window of continuous no transition during which the HS Disconnect Detector output must be sampled		36		82	ns
T_{FILT}	Time for which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake	USB 2.0 spec, section 7.1.7.5.	2.5			μs
CDP TIMING						
$T_{\text{VDMSRC_EN}}$	Time taken to enable VDMSRC on D- after detecting VDPSRC connection on D+				0.1	ms
$T_{\text{VDMSRC_DIS}}$	Time taken to disable VDMSRC on D- after detecting VDPSRC disconnection on D+				0.1	ms
$T_{\text{CON_IDPSINK_DIS}}$	Time taken to disable IDP_SINK on D+ after detecting connect				0.1	ms

7 Detailed Description

7.1 Overview

ISOUSB211 is a galvanically-isolated USB2.0 compliant repeater supporting Low Speed (1.5 Mbps), Full Speed (12 Mbps) and High Speed (480 Mbps) signaling rates. The device supports automatic speed and connection detection, reflection of pull-ups/pull-downs, and link power management allowing drop-in USB hub, host, peripheral and cable isolation. Most microcontrollers integrate the USB PHY, and so offer only D+ and D- bus lines as external pins. ISOUSB211 can isolate these pins from the USB bus without needing any other intervention from the microcontroller. The device also supports automatic role reversal - if after disconnect, if a new connect is detected on the Upstream facing port, then the Upstream and Downstream port definitions are reversed. The ISOUSB211 has inbuilt programmable equalization to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. High Speed (HS) Test Mode entry is also automatically detected, as required by the USB2.0 standard, to enable HS compliance tests.

ISOUSB211 is available in basic and reinforced isolation options with isolation withstand voltage of 3000 V_{RMS} and 5700 V_{RMS} respectively, and with surge test voltage of 6 kV_{PK} and 12.8 kV_{PK} respectively. The device can operate completely off a 4.25 V to 5.5 V supply (USB VBUS power) or from local 3.3-V and 1.8- supplies, if available, on both side 1 and side 2. This flexibility in supply voltages allows optimization for thermal performance based on power rails available in the system.

7.2 Functional Block Diagram

A simplified functional block diagram of ISOUSB211 is shown in [图 7-1](#). The device comprises the following:

1. Transmit and receive circuits and pull-up and pull-down resistors according to the USB standard.
2. Digital logic to handle bi-directional communication, and various state-transitions.
3. Internal LDOs to generate V_{3P3Vx} and V_{1P8Vx} supplies from the V_{BUSx} and V_{CCx} supplies respectively.
4. Galvanic isolation.

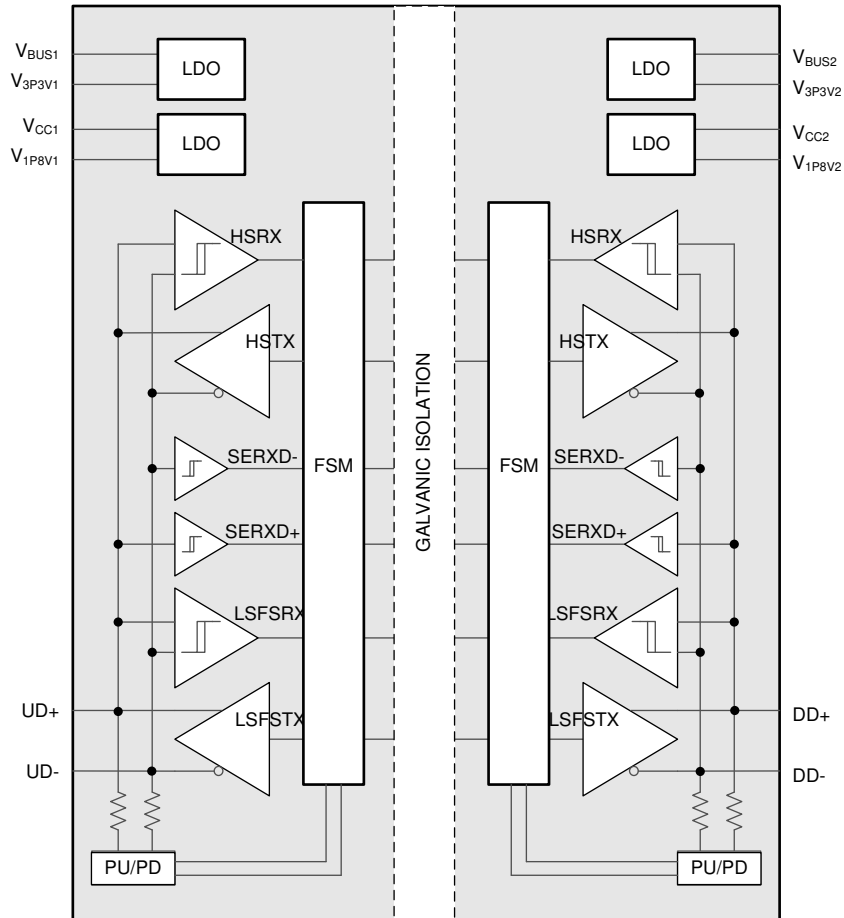


图 7-1. ISOUSB211 Simplified Functional Block Diagram

7.3 Feature Description

7.3.1 Power Supply Options

The ISOUSB211 can be powered by connecting a 4.25 V to 5.5 V supply on V_{BUSx} pins, in which case an internal LDO generates V_{3P3Vx} voltage. This option is suitable for the side facing the USB connector, where a 5-V VBUS supply is available. Alternatively, V_{BUSx} and V_{3P3Vx} pins can be shorted together and an external power 3.3-V supply can be connected to both. This second option is suitable for the side facing the microcontroller, where a 5-V supply may not be available.

The ISOUSB211 also needs a 1.8-V supply for operation. A 2.4 V to 5.5 V supply can be connected on V_{CCx} pins, in which case internal LDOs generate the V_{1P8Vx} supplies. In the simplest implementation, V_{CCx} can be connected to the USB VBUS on the side facing the connector, and to the 3.3-V local supply on the side facing the microcontroller. In this implementation, there is power dissipation on the internal LDOs of ISOUSB, which limits the maximum ambient temperature supported by ISOUSB211.

To reduce power dissipation inside the ISOUSB211, an external 1.8-V supply can be connected to both V_{CCx} and V_{1P8Vx} pins shorted together, in which case the internal 1.8-V LDOs of ISOUSB211 are bypassed. In this implementation, some of the power dissipation is transferred to the external 1.8-V supply, and overall higher ambient temperature operation is achieved for the ISOUSB211. If the external 1.8-V supply is an LDO, the effect is to reduce power dissipation inside ISOUSB211, but overall no reduction in system current or power dissipation is achieved. Alternatively, if the external 1.8-V supply is a DC-DC (buck) converter, both system power and ISOUSB211 power dissipation can be reduced.

A third option is to include external resistors between V_{CCx} pins and VBUS and 3.3-V local supplies. These resistors can be accommodated since V_{CCx} pins operate down to 2.4 V. The resistors drop voltage and dissipate

power and serve a similar purpose as external 1.8-V LDOs, that is, reduce power dissipation inside ISOUSB211 and allow higher ambient temperature operation.

Refer to the [Thermal Considerations](#) section for further details on how to optimize ISOUSB211 internal power dissipation according to the maximum ambient temperature required in the system, and for recommendations on external resistors, LDOs and buck converters.

7.3.2 Power Up

Until all power supplies on both sides of ISOUSB211 are above their respective UVLO thresholds, the device ignores any activity on the bus lines on both upstream and downstream side. Once the power supplies are above their UVLO thresholds, the device is ready to respond to activity on the bus lines. When the power supplies on side 1 are up, this is indicated on side 2 by V1OK = High. Similarly, V2OK = High indicates that Side 2 is fully powered up.

7.3.3 Symmetric Operation, Dual-Role Port and Role-Reversal

ISOUSB211 supports symmetric operation. Normally, UD+ and UD- are upstream facing ports and connect to a host or hub. DD+ and DD- are downstream facing ports and connect to a peripheral. However, it is also possible to connect UD+ and UD- to a peripheral and DD+ and DD- to a host or hub. Whichever side sees a connect first (D+ or D- pulled up to 3.3V) becomes the downstream facing side. This feature enables implementation of dual-role port (for eg. type C dual-role port) and role-reversal (for eg. OTG Host Negotiation Protocol - HNP). In the rest of this document, DD+/DD- are treated as downstream facing ports, and UD+/UD- as upstream facing ports, but the various operations and features described are equally applicable if this assignment is swapped.

7.3.4 Connect and Speed Detection

When there is no peripheral device connected to the downstream side of ISOUSB211, internal $15\text{ k}\Omega$ pull-down resistors on DD+ and DD- pins pull the bus lines to zero, creating an SE0 state. When either the DD+ or DD- lines is pulled up higher than the V_{IH} threshold, for a time period higher than $T_{FILTCNN}$, the ISOUSB211 device treats this as a connect. The ISOUSB211 device configures internal pull-up on the upstream side to match the pull-up detected on the downstream side. After connect is detected, the ISOUSB211 device waits for a reset to be asserted by the host/hub on the upstream side. Depending on whether DD+ or DD- is pulled up at the start of reset, the speed of the ISOUSB211 repeater is set. Once set, the speed of the repeater can only be changed after a power down or disconnect event.

A high-speed (HS) capable device is attached to the ISOUSB211 device would proceed to perform high-speed handshake using chirp signaling as specified in the USB2.0 standard. This would be followed by chirp signals from the host. The ISOUSB211 device reflects these chirp signals across the barrier, including HS idle (SE0) states from downstream to upstream and vice versa. Upon successful completing of the HS handshake ISOUSB211 speed is set to High speed. Once set to high-speed, the speed of the repeater can only be changed after power down, HS disconnect event, or if the peripheral or host/hub do not perform HS handshake after a reset.

7.3.5 Disconnect Detection

When in Full-speed (FS) and Low-speed (LS) modes, disconnection of a peripheral is indicated when the host/hub is not driving any signal on the upstream side, and when the downstream bus is in the SE0 state (Both DD+ and DD- are below the V_{IL} threshold) for a time period higher than T_{DDIS} . Upon disconnect detection in FS and LS modes, the ISOUSB211 device removes the pull-up resistor from the upstream side, thus allowing the upstream UD+ and UD- lines to discharge to zero. The ISOUSB211 then waits for the next connect event to occur.

When in High Speed (HS) mode, if the ISOUSB211 detects a continuous period of no transitions lasting T_{HSDIS} , the device samples the DD+ and DD- lines using the HS Disconnect detector. If the input differential voltage crosses V_{HSDSC} during T_{HSDIS} , the repeater removes the HS termination from both the downstream and upstream terminals and transitions to a disconnect state. The ISOUSB211 then waits for the next connect event to occur.

7.3.6 Reset

The ISOUSB211 device detects Reset assertion (prolonged SE0 state) on its upstream facing side, and transmits the same to the downstream facing side. In FS and LS states the reset is detected within 2.5 μ s. In HS state, an extended HS idle state can be the beginning of reset, or an entry into L2 Power Management state. ISOUSB211 is able to make the distinction between the two, and accordingly either continue to drive HS idle (same as reset) on the downstream side or transition to the L2 suspend state.

7.3.7 LS/FS Message Traffic

The ISOUSB211 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the LS/FS idle state first (J to K transition). After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues till either an End-of-Packet (EOP) or a long idle is seen. At this point, the ISOUSB211 device tri-states its LS/FS transmitters, and waits for the next transition from the LS/FS idle state.

7.3.8 HS Message Traffic

The ISOUSB211 device monitors the state of the bus on both upstream and downstream sides. The direction of communication is set by which side transitions from the HS idle state first. Transition from HS idle state to valid HS data is detected by the HS Squelch Detector. After that, data is transferred digitally across the barrier, and reconstructed on the other side. Data transmission continues till the bus returns to HS idle state, also indicated by the HS Squelch Detector. At this point, the ISOUSB211 device tri-states its HS transmitters, and waits for the next transition from the HS idle state.

7.3.9 Equalization and Pre-emphasis

The ISOUSB211 has inbuilt programmable receive equalization and transmit pre-emphasis to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagram templates. These settings are controlled by EQ11 and EQ10 on side 1 and EQ21 and EQ20 on side 2. The EQxx pins can be connected to ground, connected to 3.3-V supply or left floating, together creating 9 different equalization levels. EQ11 and EQ10 can be chosen based on the length of D+/D- board trace and corresponding channel loss estimated on side 1, and similarly EQ21 and EQ20 for side 2. Typical 45-Ohm trace in FR4 has about 0.15 dB/inch for 480 Mbps signaling. Further adjustments to the EQ settings can be made by observing the transmit eye-diagram at the connector. If the trace lengths are very small, no equalization may be needed, and the EQxx pins can be connected to ground.

7.3.10 L2 Power Management State (Suspend) and Resume

The ISOUSB211 device supports L2 or Suspend low power state. Suspend mode is detected if the bus stays in the LS/FS/HS idle state for more than 3 ms. When Suspend is detected from LS and FS idle state, the ISOUSB211 continues in the LS or FS idle state, at the same time reducing internal power consumption. If Suspend is detected from HS idle state, the ISOSUB211 detects the DS port transition to FS idle state (FS J), and reflects this upstream, while disabling all high-speed circuits to reduce power consumption. The transition to the L2 low-power mode is completed within 10 ms.

Exit from L2 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB211, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB211 followed by Resume signaling from the host/hub on the upstream facing side. Resume and Wake are signaled by a 'K' state. ISOUSB211 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS, FS or HS idle state depending on the state it was in before entering the L2 state.

7.3.11 L1 Power Management State (Sleep) and Resume

The ISOUSB211 device supports L1 or Sleep low power state. When L1 entry is detected from the LS and FS idle state, the ISOUSB211 continues in the LS or FS idle state, at the same time reducing internal power consumption. If L1 entry is detected from HS idle state, the ISOSUB211 disables all high-speed circuits to reduce power consumption. The transition to the L1 low-power mode is completed within 50 μ s.

Exit from L1 occurs through either Resume signaling from the host, on the upstream facing side of ISOUSB211, or Remote Wake signaling from the peripheral on the downstream facing side of ISOUSB211 followed by Resume signaling from the host/hub on the upstream facing side. Resume and Wake are signaled by a ‘K’ state. ISOUSB211 is able to replicate the K signaling appropriately both upstream and downstream. After Resume/Wake signaling the device returns to LS, FS or HS idle state depending on the state it was in before entering the L1 state.

7.3.12 HS Test Mode Support

USB2.0 standards needs test mode support, where the host/hub or peripheral is expected to enter High Speed test-modes based on commands received. ISOUSB211 is able to automatically detect test mode entry to enable HS compliance tests.

7.3.13 CDP Advertising

The ISOUSB211 device supports CDP advertising on both downstream and upstream facing side according to Battery Charger standard BC 1.2. CDP advertising is useful when isolating a host or hub, to indicate to the connected peripheral that the port is capable of supplying 1.5 A of current on VBUS. CDP advertising can be enabled by connecting the downstream side CDPENX pin to ground (active low).

7.4 Device Functional Modes

[Function Table](#) lists the functional modes for the ISOUSB211 device.

表 7-1. Function Table

SIDE 1 SUPPLY V _{BUS1} , V _{3P3V1} V _{CC1} , V _{1P8V1} ⁽¹⁾	BUS1 (UD+, UD-)	SIDE 2 SUPPLY V _{BUS2} , V _{3P3V2} V _{CC2} , V _{1P8V2}	BUS2 (DD+, DD-)	COMMENTS
Powered	Active	Powered	Active	When both sides are powered, the state-of the bus is reflected correctly from upstream to downstream and vice-versa.
Powered	15-k Ω PD	Powered	15-k Ω PD	Disconnected state is presented on both upstream and downstream
Powered	15-k Ω PD	Unpowered	Z	If a side is not powered, the bus lines on that side are in high-impedance state.
Unpowered	Z	Powered	15-k Ω PD	
Unpowered	Z	Unpowered	Undetermined	

(1) Powered = (V_{BUSx} ≥ UV_{+(V_{BUSx})}) || (V_{BUSx} = V_{3P3Vx} ≥ UV_{+(V_{3P3Vx})}) & ((V_{CCx} ≥ UV_{+(V_{CCx})}) || (V_{CCx} = V_{1P8Vx} ≥ UV_{+(V_{1P8Vx})}));
 Unpowered = ((V_{BUSx} < UV_{-(V_{BUSx})}) & (V_{3P3Vx} < UV_{-(V_{3P3Vx})})) || ((V_{CCx} < UV_{-(V_{CCx})}) & (V_{1P8Vx} < UV_{-(V_{1P8Vx})})); X = Irrelevant; H = High level; L = Low level; Z = High impedance

8 Power Supply Recommendations

0.1 μF capacitors are recommended to be placed very close to V_{3P3Vx} pins to GNDx. 1- μF capacitors are recommended to be placed placed very close to V_{BUSx} pins to GNDx. 2- μF , 0.1- μF , and 10-nF capacitors are recommended to be placed between V_{1P8Vx} and GNDx, between pins 4 and 3, between pins 25 and 26, between pins 11 and 12, and between pins 25 and 26 respectively, as close to the device as possible. Place the lower value capacitors closer to the IC. If V_{CCx} pins are connected through resistors as shown in [Example Configuration 3](#) 1- μF capacitors are recommended to be placed between V_{CCx} (pins 5, 24) and GNDx (pins 3, 26), as close to the device as possible, with higher priority being accorded to the capacitors on V_{1P8Vx} pins.

These decoupling capacitor recommendations are irrespective of whether the 3.3 V and 1.8 V supplies are provided externally or generated using internal LDOs.

Refer to the [节 10.1.1](#) section for recommended placement of the decoupling capacitors. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins on the top layer without the use of vias. The capacitors on V_{1P8Vx} supplies are higher in priority when considering placement close to the IC.

While isolating a host/hub or bus-powered peripherals, isolated power is needed and can be generated with the help of a transformer driver such as TI's [SN6505B](#). For such applications, detailed power supply design, and transformer selection recommendations are available in the [SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#). If CDP functionality is enabled while isolation host/hub, the isolated power supply must be capable of delivering 1.5 A on VBUS.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 Isolated Host or Hub

图 9-1 shows an application for isolating a host or a hub using ISOUSB211. In this example, on the microcontroller side, V_{3P3V1} and V_{BUS1} are together connected to an external 3.3-V supply. The V_{1P8V1} supply is generated using the internal 1.8-V LDO by providing 3.3-V supply to V_{CC1} . On the connector side, the VBUS from the USB connector is connected to V_{BUS2} and the V_{3P3V2} supply is generated using the internal 3.3-V LDO. V_{CC2} and V_{1P8V2} are together connected to an external 1.8-V supply derived from VBUS. Please refer to [Thermal Considerations](#) for options on optimizing power dissipation inside ISOUSB211 as required.

Decoupling capacitors are placed next to ISOUSB211 according to the recommendations provided in the [Power Supply Recommendations](#) section. An isolated DC-DC converter (such as the SN6505) is to provide power to the VBUS using the 3.3-V local supply. Note that, for a host or hub, the USB standard requires a 120- μ F capacitor to be placed on the VBUS so as to be able provide in-rush current when a downstream peripheral is attached. In addition, a 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 m Ω , may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211, as shown in the figure, to suppress transients such as ESD.

If the isolated power supply used is capable of providing >1.5 A current on the VBUS, the port can be configured as a CDP port according to Battery Charger specification BC 1.2. To do this, the CDPENZ2 pin of ISOUSB211

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must be connected to ground as shown. Under this condition ISOUSB211 responds to BC 1.2 signaling from a connected peripheral indicating to the peripheral that the port is capable of supply 1.5-A current on VBUS.

ADVANCE INFORMATION

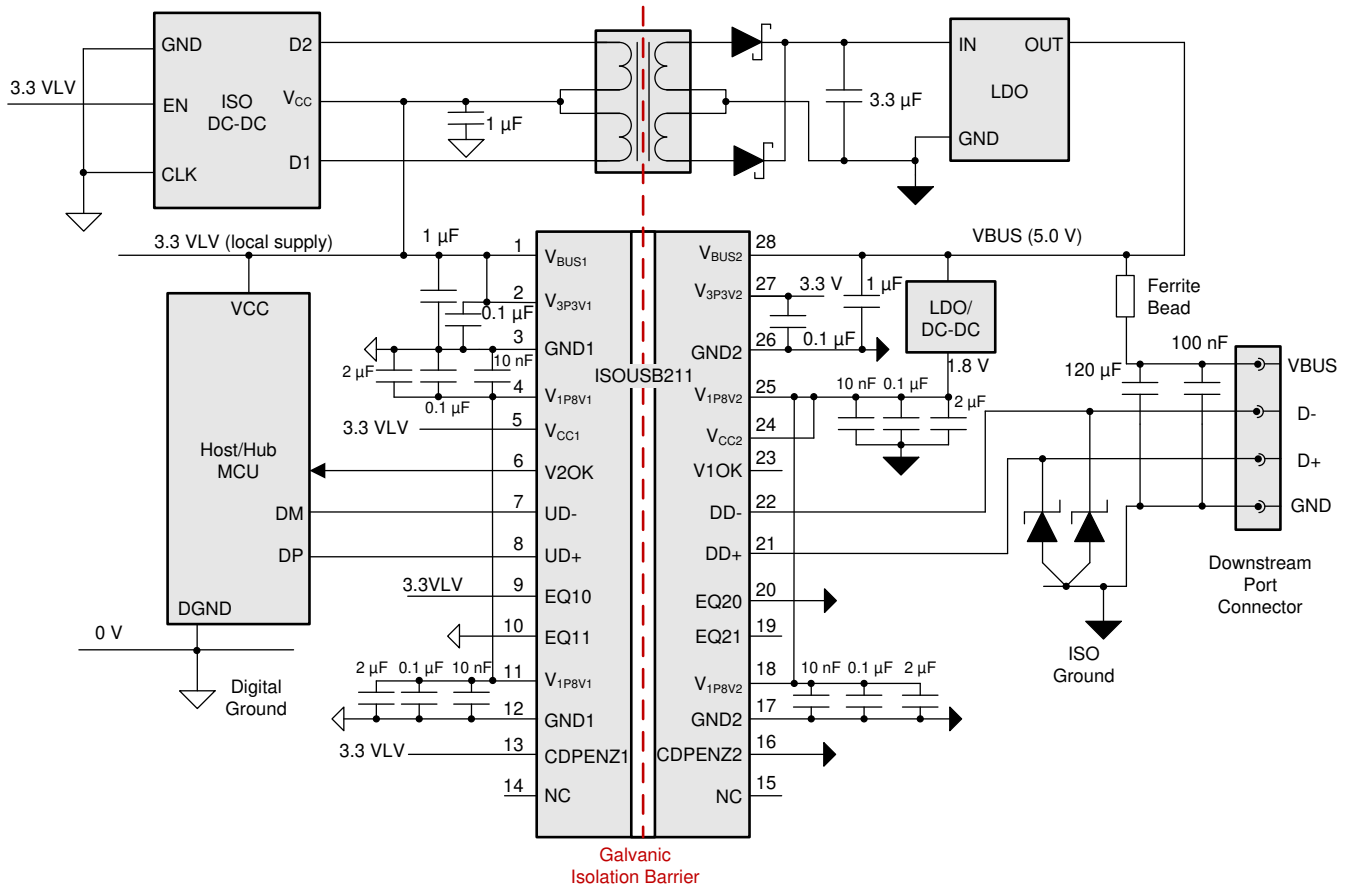


图 9-1. Isolated Host or Hub with ISOUSB211

9.1.2 Isolated Peripheral - Self-Powered

图 9-2 shows an application for isolating a self-powered peripheral using ISOUSB211. In this example, on the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. The V_{1P8V2} supply is generated using the internal 1.8-V LDO by providing 3.3-V supply to V_{CC1} . On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO. V_{CC1} and V_{1P8V1} are together connected to an external 1.8-V supply derived from VBUS. Please refer to [Thermal Considerations](#) for options on optimizing power dissipation inside ISOUSB211 as required.

Decoupling capacitors are placed next to ISOUSB211 according to the recommendations provided in the [Power Supply Recommendations](#) section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS must be less than 10- μ F. A 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 mΩ, may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211, as shown in the figure, to suppress transients such as ESD.

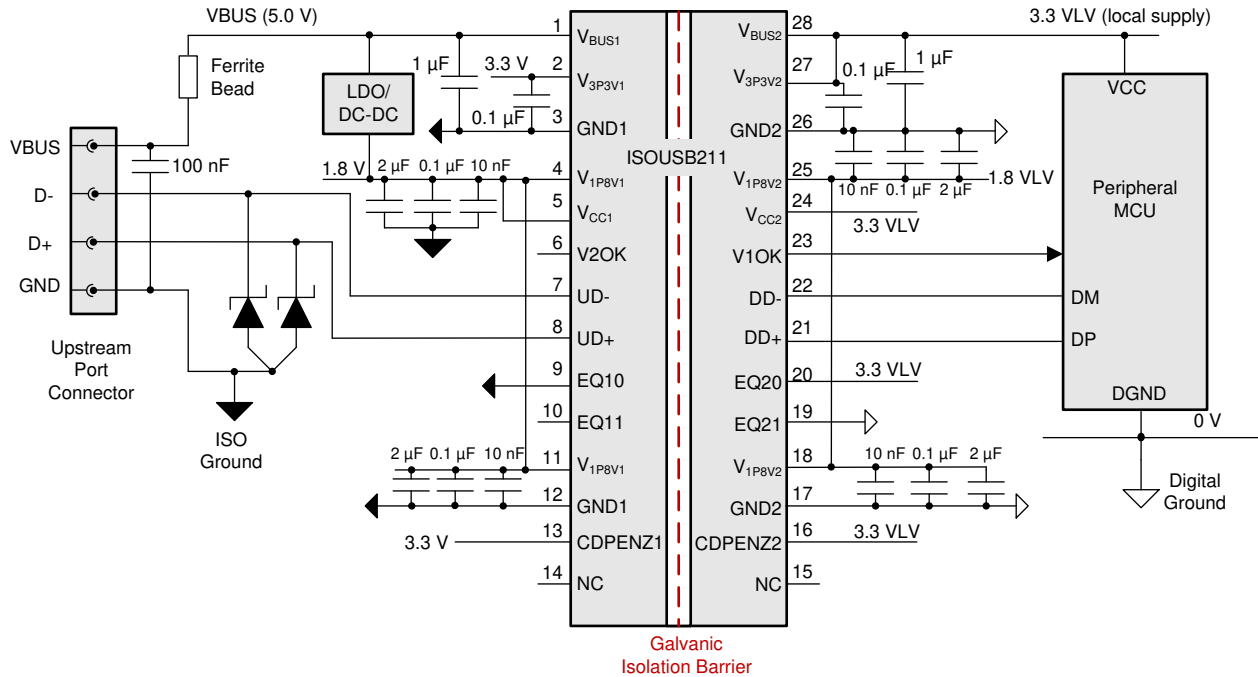


图 9-2. Isolated Self-Powered Peripheral with ISOUSB211

9.1.3 Isolated Peripheral - Bus-Powered

图 9-3 shows an application for isolating a self-powered peripheral using ISOUSB211. In this example, an isolated DC-DC converter (for example: SN6505) is used to create a 3.3-V local supply while deriving power from the USB VBUS. On the microcontroller side, V_{3P3V2} and V_{BUS2} are together connected to an external 3.3-V supply. The V_{1P8V2} supply is generated using the internal 1.8-V LDO by connecting the 3.3-V local supply to V_{CC1}. On the connector side, the VBUS from the USB connector is connected to V_{BUS1} and the V_{3P3V1} supply is generated using the internal 3.3-V LDO. V_{CC1} and V_{1P8V1} are connected together connected to an external 1.8-V supply derived from VBUS. Please refer to [Thermal Considerations](#) for options on optimizing power dissipation inside ISOUSB211 as required.

Decoupling capacitors are placed next to ISOUSB211 according to the recommendations provided in the [Power Supply Recommendations](#) section. Note that the USB standard requires that, for a peripheral, the total capacitor value on VBUS, including any decoupling capacitors reflected from the secondary side through the isolated DC-DC converter, must be less than 10-μF. A 100-nF capacitor is recommended close to the VBUS pin to handle transient currents.

ESD diodes with low capacitance and low dynamic resistance, such as PESD5V0C1USF, may be placed on D+ and D- lines. A ferrite bead, with dc resistance less than 100 m Ω , may be optionally placed between VBUS pin of the connector and the V_{BUS} pin of ISOUSB211, as shown in the figure, to suppress transients such as ESD.

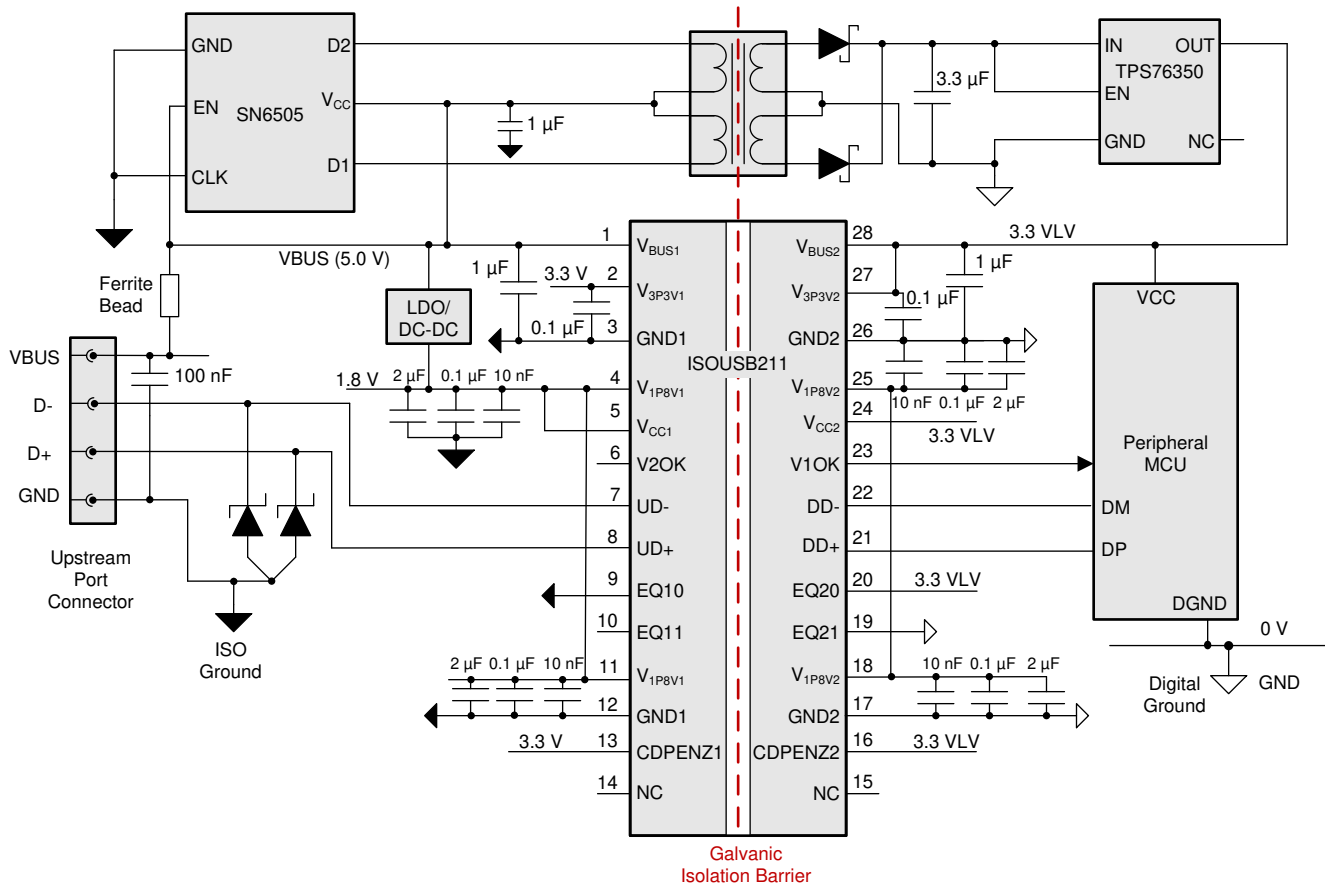


图 9-3. Isolated Bus-Powered Peripheral using ISOUSB211

9.1.4 Application Curve

9.1.4.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 图 9-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

图 9-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 135 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DP-28 package is specified upto 1500 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 135 years.

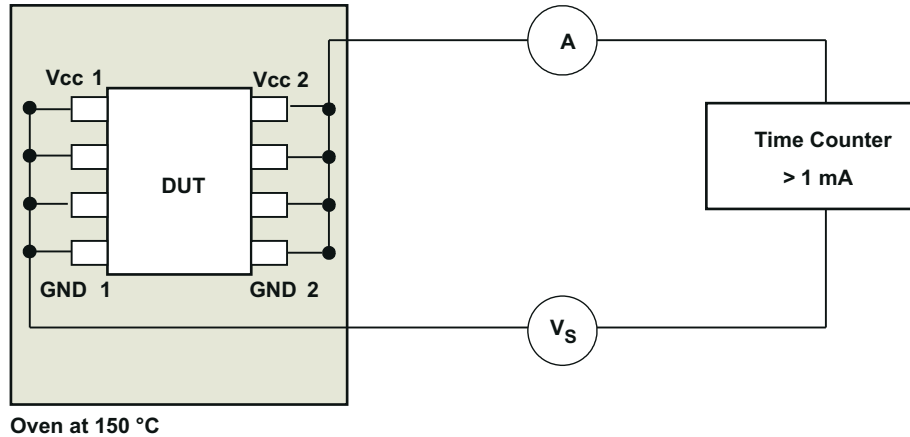


图 9-4. Test Setup for Insulation Lifetime Measurement

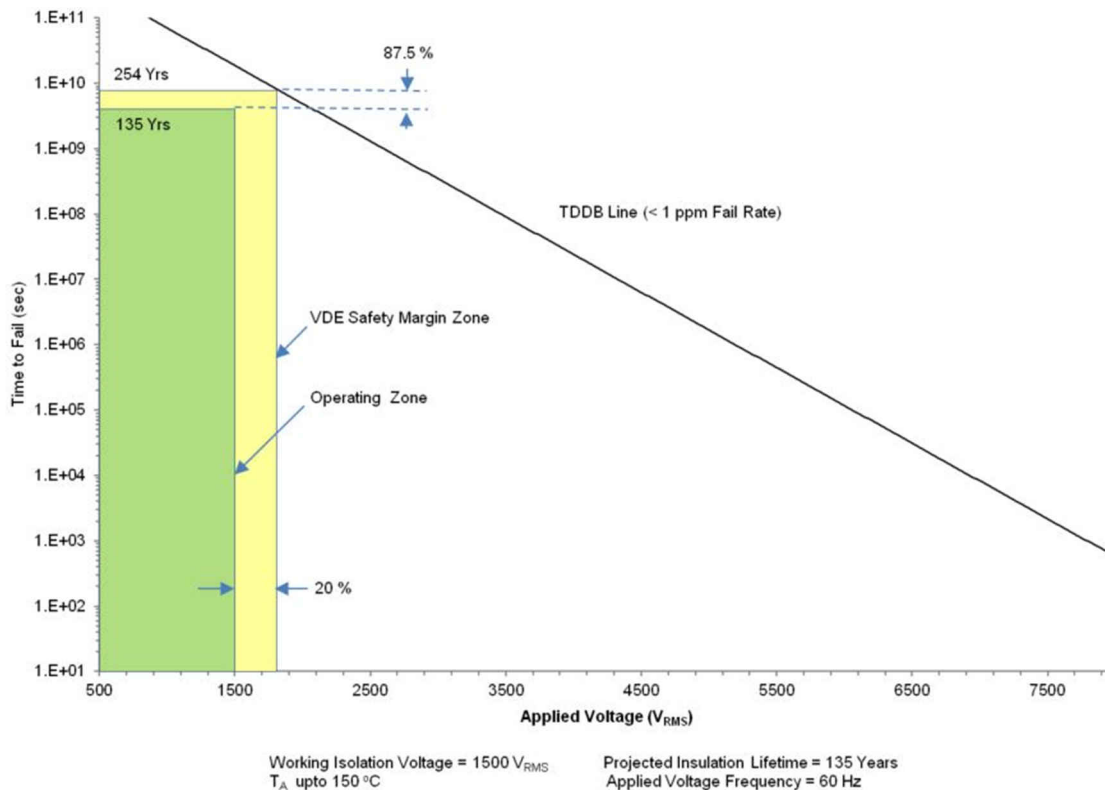


图 9-5. Insulation Lifetime Projection Data

9.2 Meeting USB2.0 HS Eye-Diagram Specifications

The USB2.0 standards specifies TX and RX eye-diagram templates that must be met at the connector. The horizontal eye-opening achieved at the connector is a combination of the performance at the microcontroller, the additive jitter of the ISOUSB211, and the inter-symbol interference resulting from the insertion loss of D+/D- board traces. For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB211, and from ISOUSB211 to the connector. Vias and stubs on D+/D- lines must be avoided.

The ISOUSB211 has inbuilt programmable receive equalization and transmit pre-emphasis to cancel signal loss caused by board traces, which helps in meeting USB2.0 high-speed TX and RX eye-diagrams. EQ11 and EQ10 can be chosen based on the length of D+/D- board traces and corresponding channel loss estimated on side 1,

and similarly EQ21 and EQ20 for side 2. The EQxx pins can be connected to ground, connected to 3.3-V supply or left floating, together creating 9 different equalization levels.

Typical 45-Ohm traces in FR4 have an insertion loss of about 0.15 dB/inch for 480 Mbps signaling. This number can be used to arrive at an estimate for the amount of Equalization/Pre-emphasis needed and the corresponding EQ settings. Further adjustments to the EQxx settings can be made by observing the transmit eye-diagram at the connector, and choosing the setting that gives the best eye-opening. Choosing the right setting for the transmit path will also result in an optimum performance for the receive path. If the trace lengths are very small, no equalization may be needed, and the EQxx pins can be connected to ground.

9.3 Thermal Considerations

ISOUSB211 offers different power supply input options, including internal LDOs, that can be used to optimize thermal performance in HS mode. If the 3.3-V and 1.8-V supplies are supplied using external regulators, the power dissipated inside the ISOUSB chip is lower. The internal power dissipated, when taken with the junction-to-air thermal resistance defined in the Thermal Information table can be used to determine the junction temperature for a given ambient temperature. The junction temperature must not exceed 150°C. This section describes different power supply configurations for ISOUSB211 and explains how the power dissipated inside ISOUSB211 and the internal temperature rise can be calculated in each case.

For optimal thermal performance, connect small ground planes to the GNDx pins, and connect these planes to the ground layer with multiple vias as shown in [Layout Example](#).

9.3.1 V_{BUS} / V_{3P3V} Power

If VBUS is connected to external 5.0-V supply, with V3P3V generated through an internal LDO, the power dissipated is $V_{BUSx} \times I_{VBUSx}$.

If VBUSx and V3P3Vx are shorted together and connected to an external 3.3V supply, the power dissipated due to this supply is $V_{3P3Vx} \times I_{3P3Vx}$.

9.3.2 V_{CCx} / V_{1P8Vx} Power

If V_{CCx} is connected to external 2.4 to 5.0-V supply, with V_{1P8Vx} generated through the internal 1.8-V LDO, the power dissipated is $V_{CCx} \times I_{VCCx}$.

If V_{CCx} and V_{1P8Vx} are shorted together and connected to an external 1.8-V supply, the power dissipated due to this supply is $V_{1P8Vx} \times I_{1P8Vx}$.

9.3.3 Example Configuration 1

In the application example shown in [Figure 9-6](#), ISOUSB211 is powered using USB VBUS on the connector side, and a local 3.3-V digital supply on the microcontroller side. No other external regulators or power supplies are used.

In this scenario, the total power consumption inside ISOUSB211 from both sides taken together is:

$$V_{BUS1} \times I_{VBUS1} + V_{BUS1} \times I_{VCC1} + V_{3P3V2} \times I_{3P3V2} + V_{3P3V2} \times I_{VCC2}$$

Assuming 5.25 V as the maximum value of VBUS1, and 3.5 V as the maximum value of the 3.3-V local supply, the internal power dissipation is calculated as:

$$5.25 \text{ V} \times 13.5 \text{ mA} + 5.25 \text{ V} \times 96 \text{ mA} + 3.5 \text{ V} \times 13.5 \text{ mA} + 3.5 \text{ V} \times 96 \text{ mA} = 960 \text{ mW}$$

Since the junction-to-air thermal resistance is 51°C/W, this power dissipation results in a 49°C internal temperature rise. Ambient temperature up to 101°C can be supported for this configuration.

This configuration offers the simplest implementation, but the ambient temperature supported is lower than other configurations.

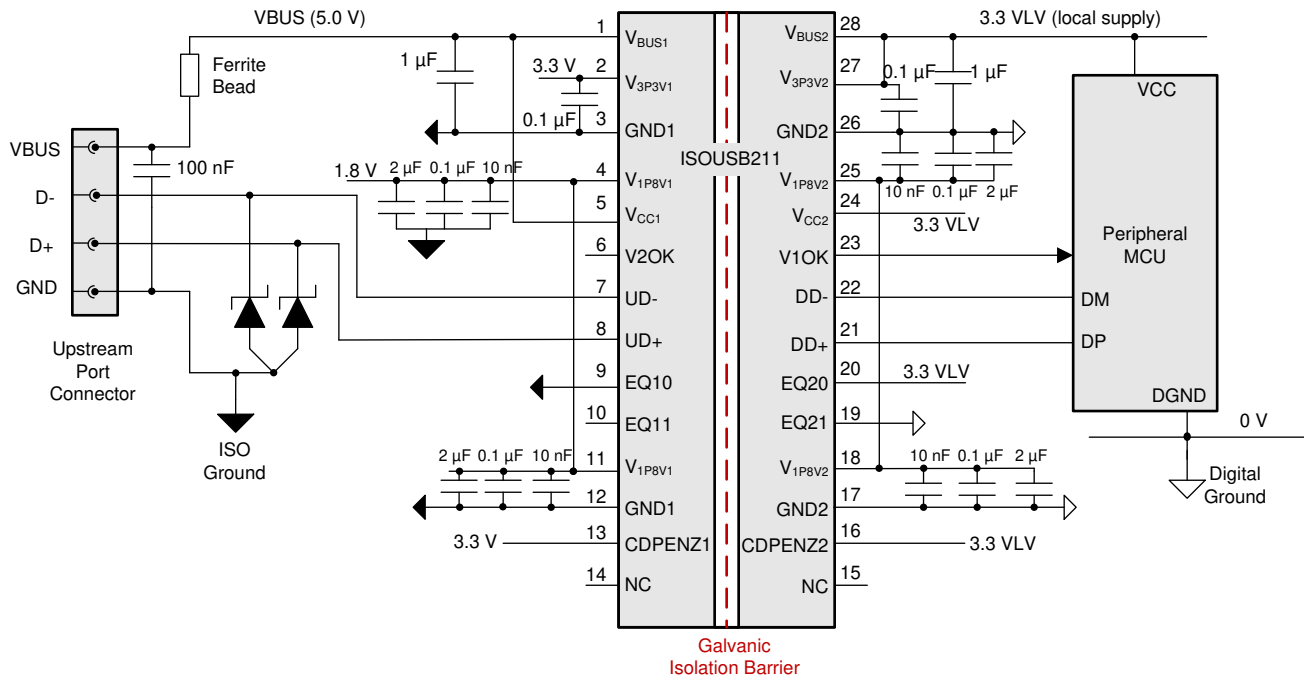


图 9-6. Using ISOUSB211 without External 1.8-V Regulators

9.3.4 Example Configuration 2

In the application example shown in 图 9-7, ISOUSB211 is powered using USB VBUS on the connector side, and a local 3.3-V digital supply on the microcontroller side to generate V_{3P3Vx} . An external LDO or DC-DC buck converter is used to generate V_{1P8Vx} on both sides.

In this scenario, the total power consumption from both sides taken together is:

$$V_{BUS1} \times I_{VBUS1} + V_{1P8V1} \times I_{1P8V1} + V_{3P3V2} \times I_{3P3V2} + V_{1P8V2} \times I_{1P8V2}$$

Assuming 5.25 V as the maximum value of VBUS, and 1.89 V as the maximum value of the external 1.8-V power supply, the internal power dissipation is calculated as

$$5.25 \text{ V} \times 13.5 \text{ mA} + 1.89 \text{ V} \times 96 \text{ mA} + 3.5 \text{ V} \times 13.5 \text{ mA} + 1.89 \text{ V} \times 96 \text{ mA} = 481 \text{ mW}$$

Since the junction-to-air thermal resistance is 51°C/W, this power dissipation results in a 25°C internal temperature rise. Ambient temperature up to 125°C can be supported for this configuration.

TLV741P and TLV62568 are examples of low-cost LDO and buck converter respectively that may be used in this application. Both options reduce the power dissipation in ISOUSB211. However, the buck converter additionally reduces power dissipation at the system level, and also the current drawn from VBUS and local 3.3-V supplies.

This configuration offers the lowest power dissipation and the highest ambient temperature operation using external regulators.

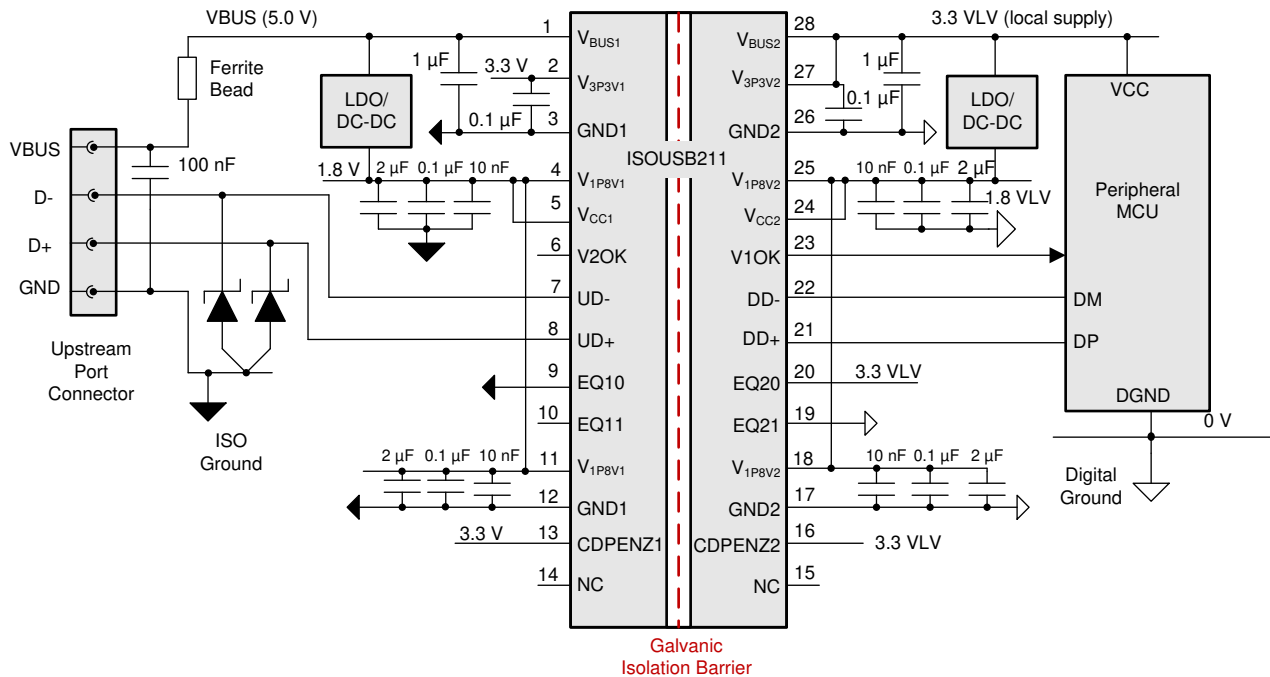


图 9-7. Using ISOUSB211 with 1.8-V supplied with External Regulators

9.3.5 Example Configuration 3

In the application example shown in 图 9-8, ISOUSB211 is powered using USB VBUS on the connector side, and a local 3.3-V digital supply on the microcontroller side to generate V_{3P3Vx}. The internal LDOs are used to generate V_{1P8Vx} on both sides like in Example Configuration 1. However, the V_{CC1} and V_{CC2} are connected to VBUS and 3.3 VLV, not directly like in Example Configuration 1, but through resistors R1 (20 Ω, 250 mW) and R2 (5 Ω, 50 mW) respectively.

The external resistors drop voltage, and dissipate power, helping reduce the power dissipation within ISOUSB211, and the corresponding temperature rise. The resistor values are decided keeping in mind that the V_{CCx} voltage can be as low as 2.4 V. Additional 1- μ F capacitors are needed on V_{CCx} pins.

In this scenario, the total power consumption inside the IC from both sides taken together is:

$$V_{BUS1} \times I_{VBUS1} + V_{BUS1} \times I_{VCC1} - 20 \Omega \times I_{VCC1} \times I_{VCC1} + V_{3P3V2} \times I_{3P3V2} + V_{3P3V2} \times I_{VCC2} - 5 \Omega \times I_{VCC2} \times I_{VCC2}$$

Assuming 5.25 V as the maximum value of VBUS, and 3.5 V as the maximum value of the 3.3-V local supply, the internal power dissipation is calculated as

$$5.25 \text{ V} \times 13.5 \text{ mA} + 5.25 \text{ V} \times 96 \text{ mA} - 20 \Omega \times 96 \text{ mA} \times 96 \text{ mA} + 3.5 \text{ V} \times 13.5 \text{ mA} + 3.5 \text{ V} \times 96 \text{ mA} - 5 \Omega \times 96 \text{ mA} \times 96 \text{ mA} = 728 \text{ mW.}$$

Since the junction-to-air thermal resistance is 51°C/W, this power dissipation results in a 38°C internal temperature rise. Ambient temperature up to 112°C can be supported for this configuration.

This configuration offers a middle path between [Example Configuration 1](#) and [Example Configuration 2](#), achieving lower temperature rise, and higher ambient temperature operation, with the addition of only two resistors and two capacitors.

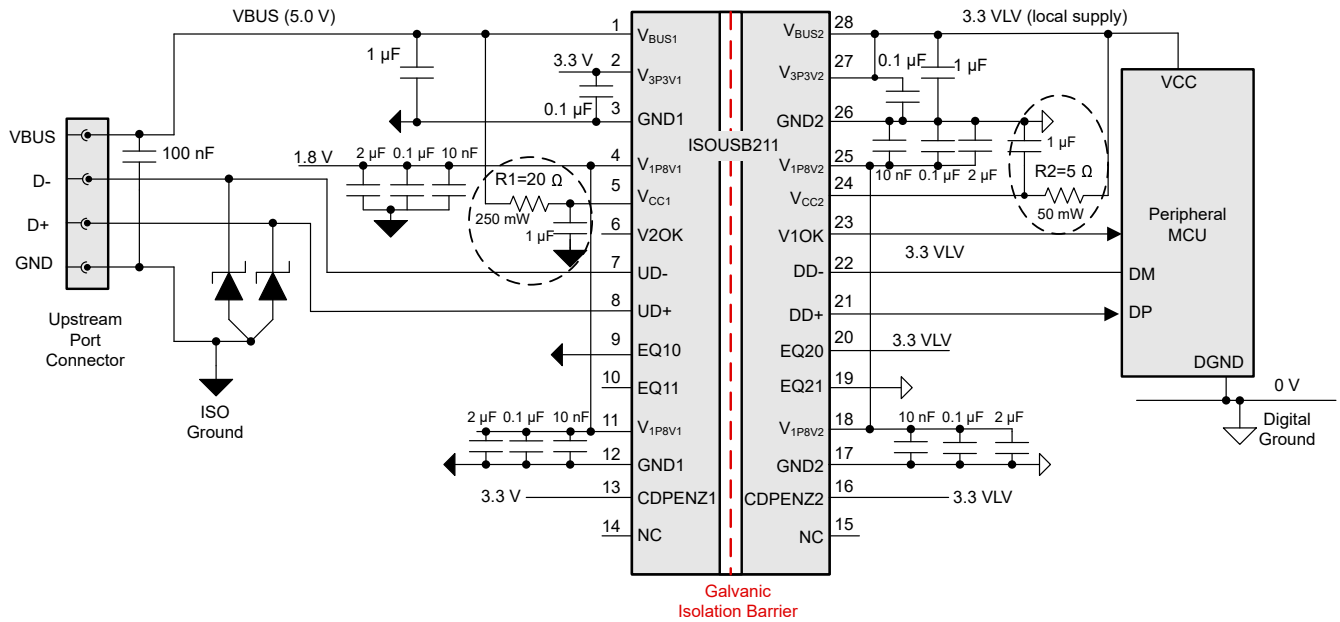


图 9-8. Using ISOUSB211 with Resistors in series with V_{CCx} pins

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Three layers are sufficient to accomplish a low EMI PCB design. Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, optional power layer, and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB211, and from ISOUSB211 to the connector. Vias and stubs on D+/D- lines must be avoided. This is especially important for High Speed Operation.
- Placing a solid ground plane just below the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow. D+ and D- traces must be designed for 90- Ω differential impedance and as close to 45- Ω single ended impedance as possible.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Decoupling capacitors must be placed on the top layer, and the routing between the capacitors and the corresponding to supply and ground pins must be completed in the top layer itself. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Connect a small plane (for example, 2 mm x 2 mm) to the GND pins on the top layer to improve thermal performance. Connect this to the ground player in the second layer with multiple vias. See [Layout Example](#) for details.

10.1.1 Layout Example

The layout example in this section shows the recommended placement for de-coupling capacitors and ESD protection diodes. A continuous ground plane is recommended below the D+/D- signal traces. Small footprint capacitors (0402/0201) are recommended so that these may be placed very close to the supply pins and corresponding ground pins and connected using the top layer. There should not be any vias in the routing path between the decoupling capacitors and the corresponding supply and ground pins. The capacitors on V_{1P8Vx} supplies are higher in priority when considering placement close to the IC. The ESD protection diodes should be placed close to the connector with a strong connection to the ground plane. Pins 4 and 11 for V_{1P8V1} and pins 18 and 25 for V_{1P8V2} are connected together, but this connection is after the de-coupling capacitors. If more than 2 layers are available in the PCB, this connection should be made in an inner or bottom layer (ex. Layer 3 or 4) so as to not interrupt the ground plane under the D+/D- traces. The example shown is for an isolated host or hub, but similar considerations apply for isolated peripherals also. The 120- μ F capacitor on VBUS only applies to host or hub and should not be used for peripherals. A ferrite bead, with dc resistance less than 100 m Ω , may be optionally placed on the VBUS route, after the 100-nF (and 120- μ F) capacitors to prevent transients such as ESD from affecting the rest of the circuits.

For best performance, it is recommended to minimize the length of D+/D- board traces from the MCU to ISOUSB211, and from ISOUSB211 to the connector. Vias and stubs on D+/D- lines must be avoided. This is especially important for High Speed Operation.

Connect a small plane (for example, 2 mm x 2 mm) to the GND pins on the top layer to improve thermal performance. Connect this to the ground player in the second layer with multiple vias.

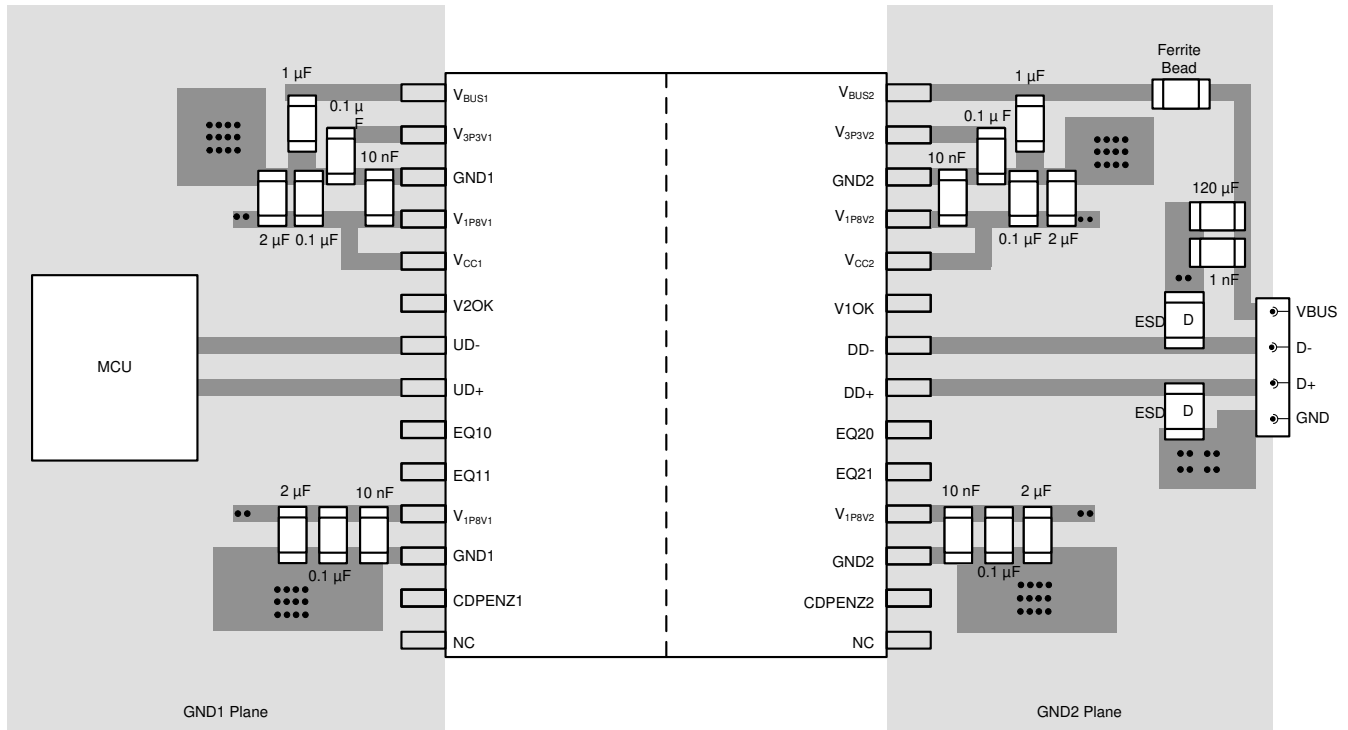


图 10-1. Layout Example for ISOUSB211

10.1.2 PCB Material

For digital circuit boards operating at less than 500 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

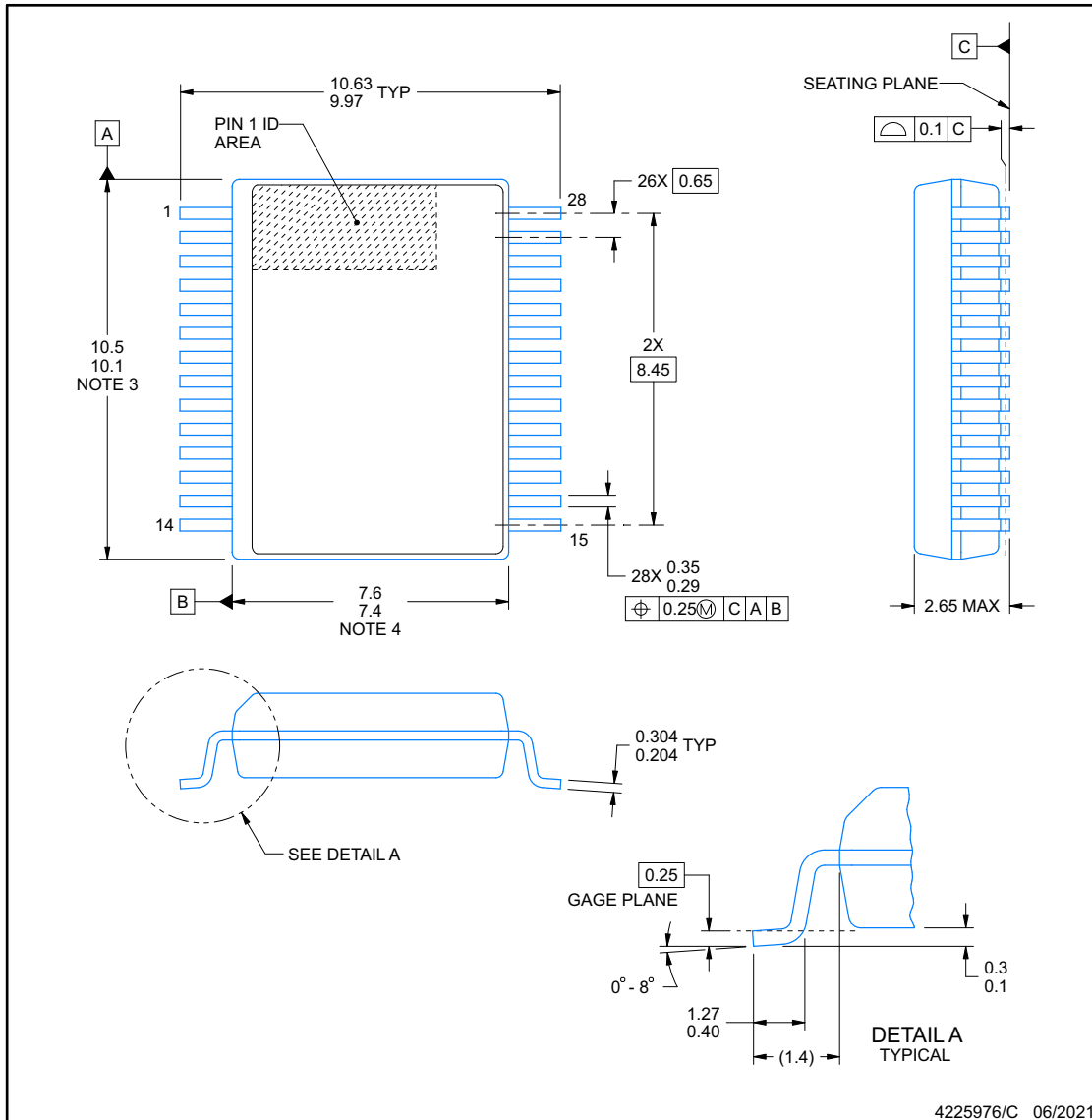
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



DP0028A

PACKAGE OUTLINE
SSOP - 2.65 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

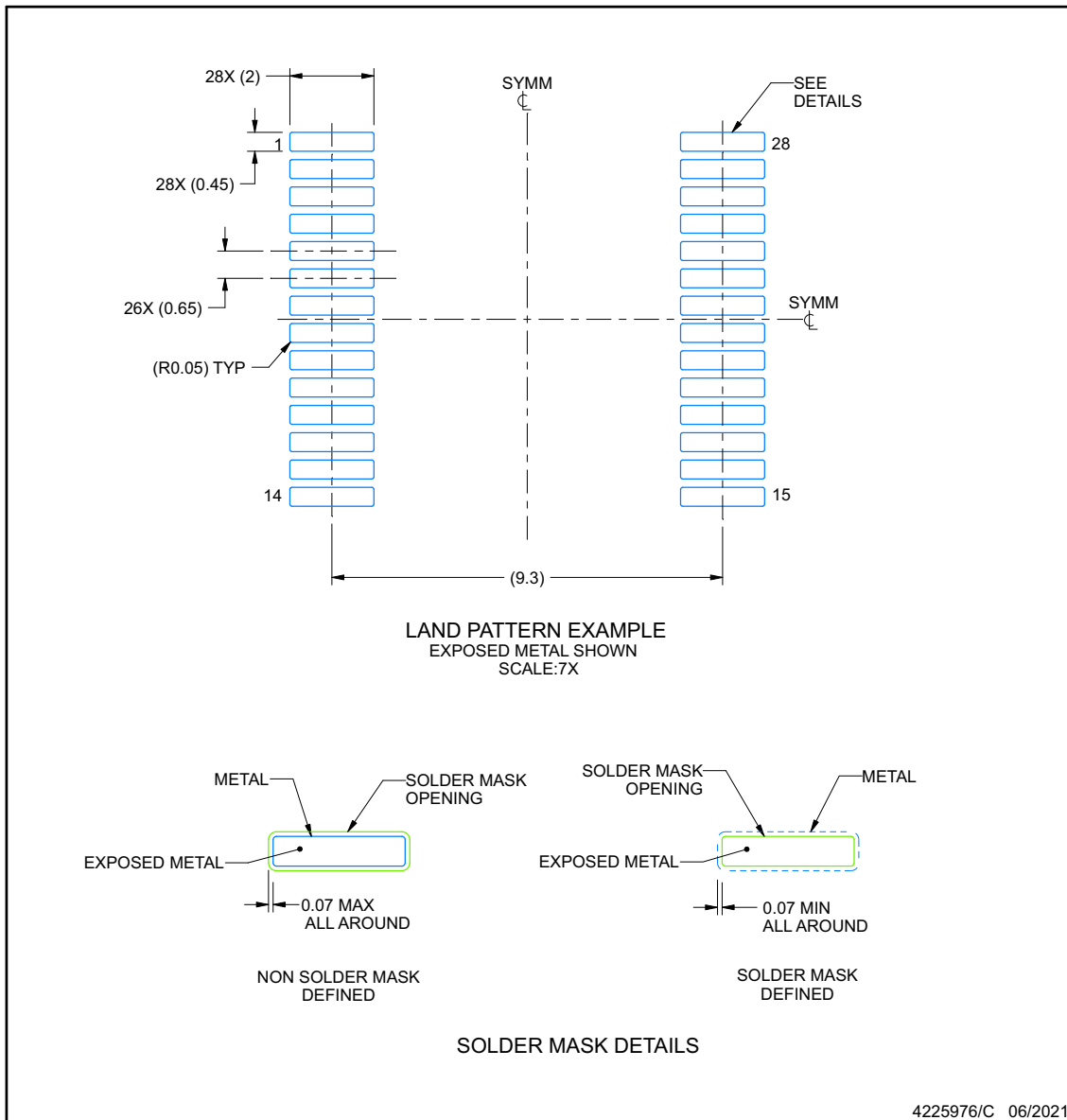
EXAMPLE BOARD LAYOUT

DP0028A

SSOP - 2.65 mm max height

SHRINK SMALL-OUTLINE PACKAGE

ADVANCE INFORMATION



NOTES: (continued)

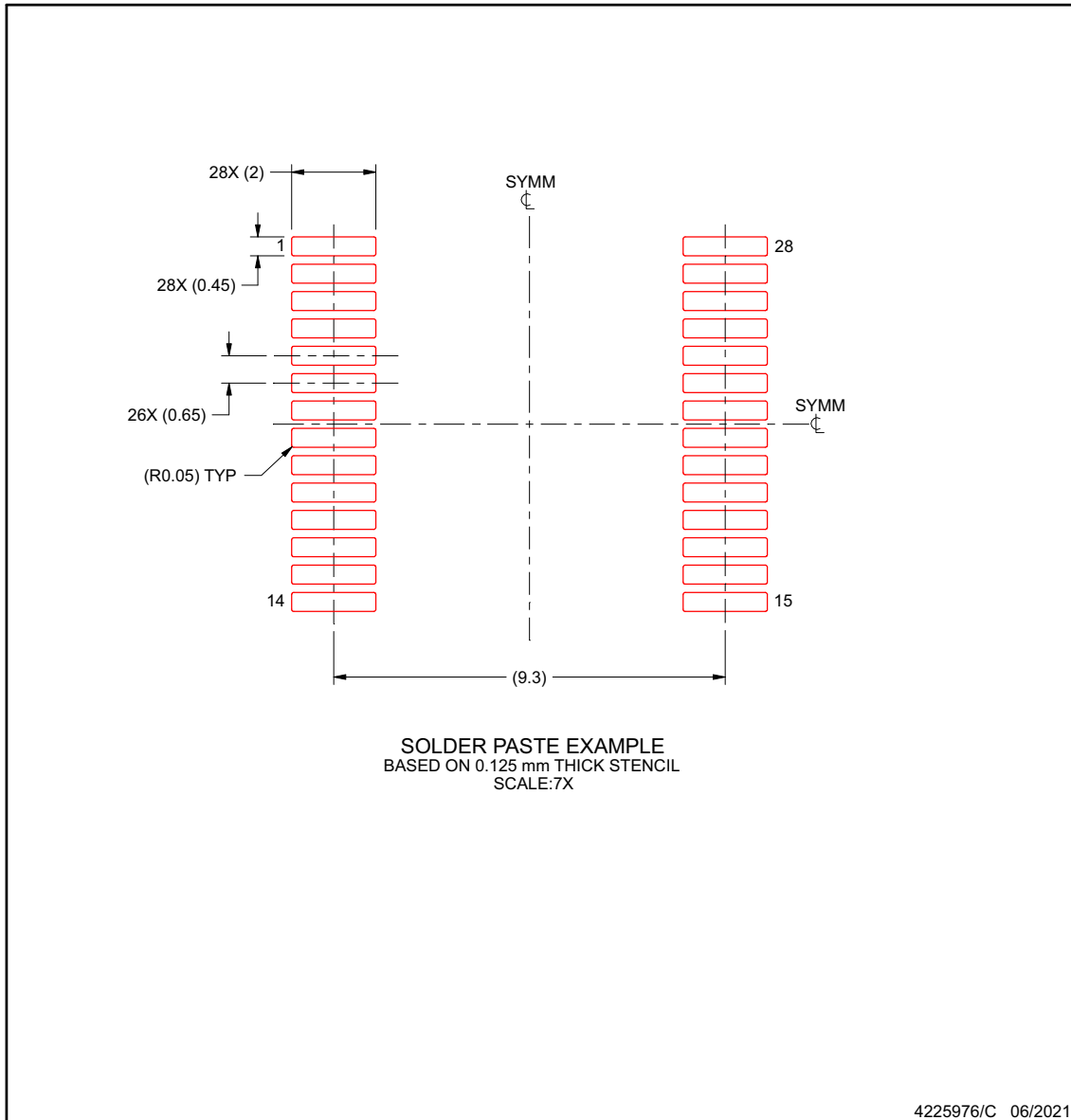
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DP0028A

SSOP - 2.65 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES: (continued)

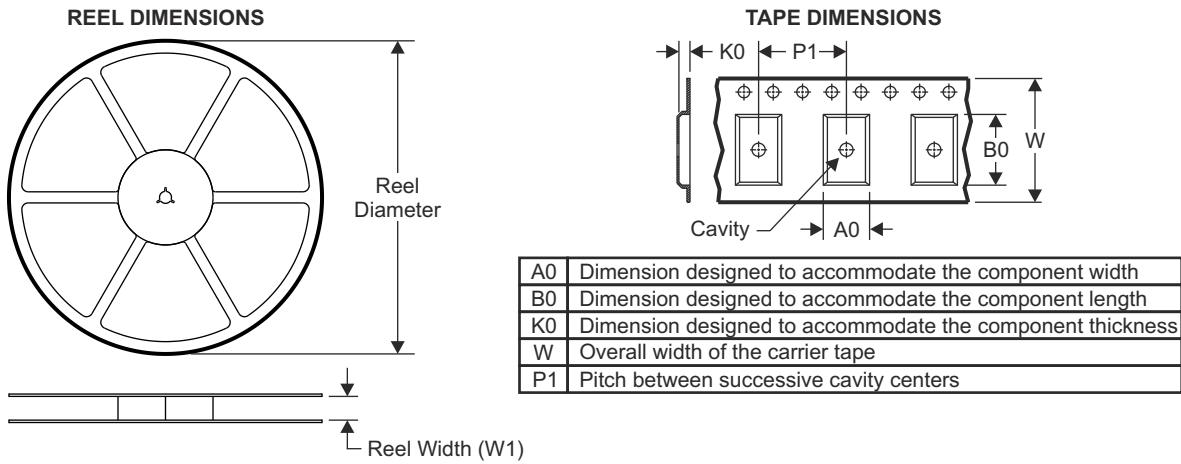
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

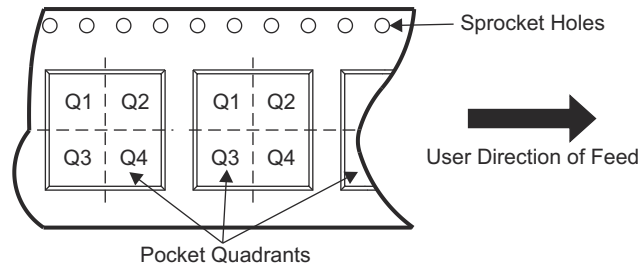
ISOUSB211

ZHCSQ53A - NOVEMBER 2021 - REVISED MARCH 2022

12.1 Tape and Reel Information



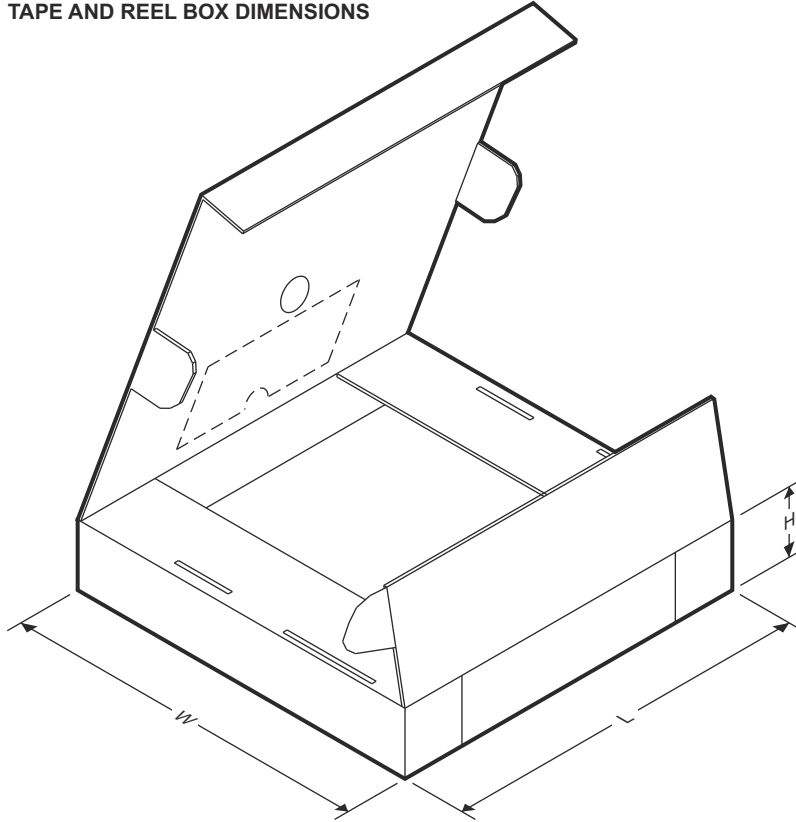
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XISOUSB211DPR	SSOP	DP	28	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XISOUSB211DPR	SSOP	DP	28	2000	350.0	350.0	43.0

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOUSB211DPR	ACTIVE	SSOP	DP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOUSB211	Samples
XISOUSB211DPR	ACTIVE	SSOP	DP	28	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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