LM3485 Hysteretic PFET Buck Controller

1 Features

- Easy-to-Use Control Methodology
- No Control-Loop Compensation Required
- 4.5-V to 35-V Wide Input Range
- 1.242-V to V_{IN} Adjustable Output Range
- High Efficiency 93%
- ±1.3% (±2% Over Temp) Internal Reference
- 100% Duty Cycle
- Maximum Operating Frequency > 1 MHz
- Current Limit Protection

2 Applications

- Set-Top Box
- DSL or Cable Modem
- PC/IA
- Auto PC
- TFT Monitor
- Battery-Powered Portable Applications
- Distributed Power Systems
- Always On Power

3 Description

The LM3485 is a high-efficiency PFET switching regulator controller that can be used to quickly and easily develop a small, low-cost, switching buck regulator for a wide range of applications. The hysteretic control architecture provides for simple design without any control-loop stability concerns using a wide variety of external components. The PFET architecture also allows for low component count as well as ultralow dropout, 100% duty cycle operation. Another benefit is high efficiency operation at light loads without an increase in output ripple.

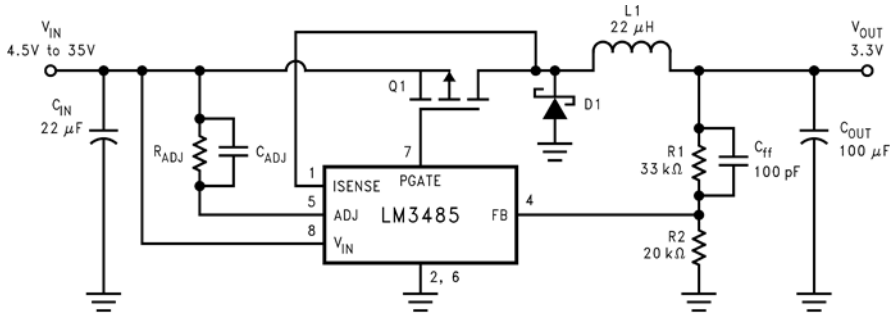
Current limit protection is provided by measuring the voltage across the $R_{DS(ON)}$ of the PFET, thus eliminating the need for a sense resistor. The cycle-by-cycle current limit can be adjusted with a single resistor, ensuring safe operation over a range of output currents.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3485	VSSOP (8)	3.0 mm × 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (February 2013) to Revision H **Page**

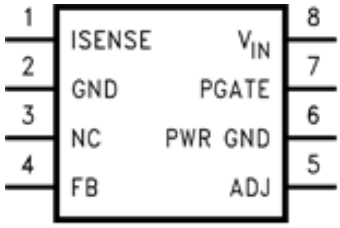
- Added *ESD Ratings*, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision F (February 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format ... 20

5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



Pin Functions

NO.	NAME	I/O	DESCRIPTION
1	ISENSE	I	The current sense input pin. This pin should be connected to Drain node of the external PFET.
2	GND	G	Signal ground
3	NC	—	No connection
4	FB	I	The feedback input. Connect the FB to a resistor voltage divider between the output and GND for an adjustable output voltage.
5	ADJ	I	Current limit threshold adjustment. It connects to an internal 5.5-µA current source. A resistor is connected between this pin and the input Power Supply. The voltage across this resistor is compared with the V_{DS} of the external PFET to determine if an over-current condition has occurred.
6	PWR GND	G	Power ground
7	PGATE	O	Gate Drive output for the external PFET. PGATE swings between V_{IN} and V_{IN}-5 V.
8	VIN	P/I	Power supply input pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	TYP	MAX	UNIT
PGATE voltage		−0.3		36	V
FB voltage		−0.3		5	V
ISENSE voltage		−1.0		36	V
ADJ voltage		−0.3		36	V
Maximum junction temperature			150		°C
Power dissipation (at T_A = 25°C)		417			mW
Lead temperature	Vapor phase (60 sec.)		215		°C
	Infrared (15 sec.)		220		°C
Storage temperature, T_{stg}		−65		160	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
	Supply voltage	4.5		35	V
T_J	Operating junction temperature	−40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM3485 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	81.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

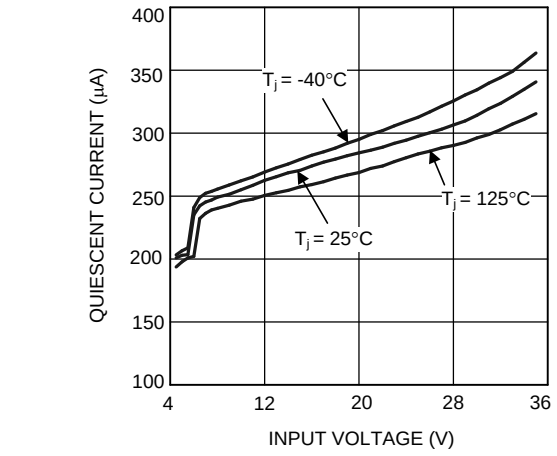
Specifications are for T_J = 25°C. Unless otherwise specified, V_{IN} = 12 V, $V_{ISNS} = V_{IN} - 1$ V, and $V_{ADJ} = V_{IN} - 1.1$ V. Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
I_Q	Quiescent current at ground pin	FB = 1.5 V (Not Switching)			250		µA
		(T_J = −40°C to 125°C)				400	
V_{FB}	Feedback voltage(3)			1.226	1.242	1.258	V
		(T_J = −40°C to 125°C)		1.217		1.267	
V_{HYST}	Comparator hysteresis				10	15	mV
		(T_J = −40°C to 125°C)			14	20	
V_{CL}(4)	Current limit comparator trip voltage	R_{ADJ} = 20 kΩ			110		mV
		R_{ADJ} = 160 kΩ			880		
V_{CL_OFFSET}	Current limit comparator offset	V_{FB} = 1.5 V			0		mV
		(T_J = −40°C to 125°C)		−20		20	
I_{CL_ADJ}	Current limit ADJ current source	V_{FB} = 1.5 V			5.5		µA
		(T_J = −40°C to 125°C)		3.0		7.0	
T_{ONMIN_CLCL}	Current limit one shot off time	V_{ADJ} = 11.5 V V_{ISNS} = 11.0 V V_{FB} = 1.0 V			9		µs
			(T_J = −40°C to 125°C)	6		14	
R_{PGATE}	Driver resistance	Source I_{SOURCE} = 100 mA			5.5		Ω
		Sink I_{Sink} = 100 mA			8.5		
I_{PGATE}	Driver output current	Source V_{IN} = 7 V, P_{GATE} = 3.5 V			0.44		A
		Sink V_{IN} = 7 V, P_{GATE} = 3.5 V			0.32		
I_{FB}	FB pin bias current(5)	V_{FB} = 1.0 V			300		nA
		(T_J = −40°C to 125°C)				750	
T_{ONMIN_NOR}	Minimum on time in normal operation	$V_{ISNS} = V_{ADJ}$ + 0.1 V C_{load} on OUT = 1000 pF(6)			100		ns
T	Minimum on time in current limit	$V_{ISNS} = V_{ADJ}$ + 0.1 V V_{FB} = 1.0 V C_{load} on OUT = 1000 pF(6)			175		ns
$\%V_{FB}/\Delta V_{IN}$	Feedback voltage line regulation	4.5 ≤ V_{IN} ≤ 35 V			0.010%		

(1) All limits are at room temperature unless otherwise specified. All room temperature limits are 100% tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) The V_{FB} is the trip voltage at the FB pin when PGATE switches from high to low.
(4) $V_{CL} = I_{CL\_ADJ} \times R_{ADJ}$
(5) Bias current flows out from the FB pin.
(6) A 1000-pF capacitor is connected between V_{IN} and PGATE.

6.6 Typical Characteristics

Unless otherwise specified, T_J = 25°C



FB = 1.5 V

Figure 1. Quiescent Current vs Input Voltage

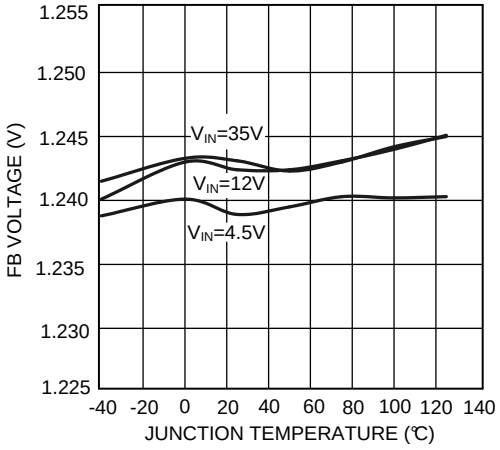


Figure 2. Feedback Voltage vs Temperature

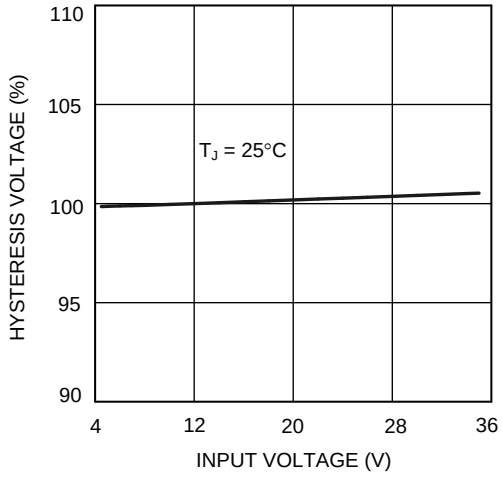


Figure 3. Hysteresis Voltage vs Input Voltage

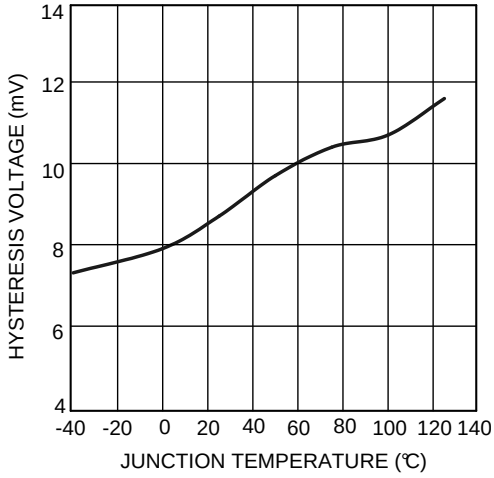


Figure 4. Hysteresis Voltage vs Temperature

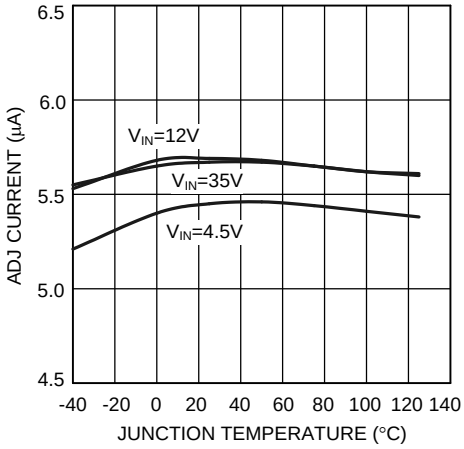


Figure 5. Current Limit ADJ Current vs Temperature

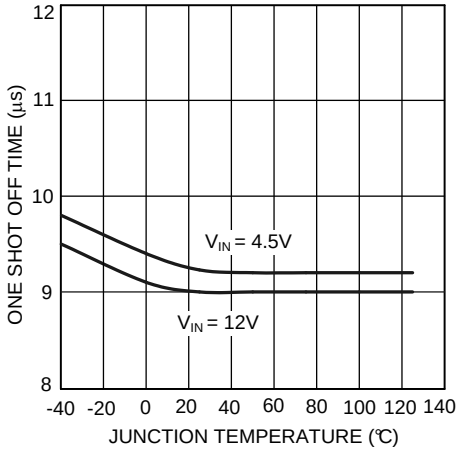


Figure 6. Current Limit One-Shot OFF-Time vs Temperature

Typical Characteristics (continued)

Unless otherwise specified, T_J = 25°C

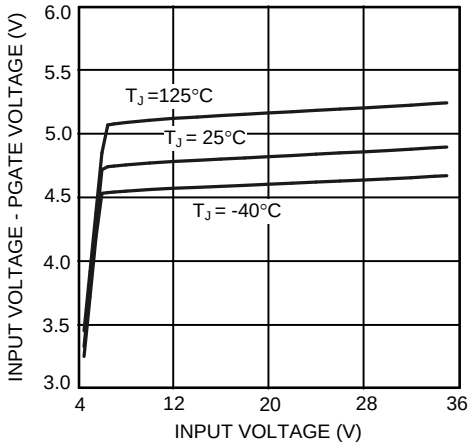
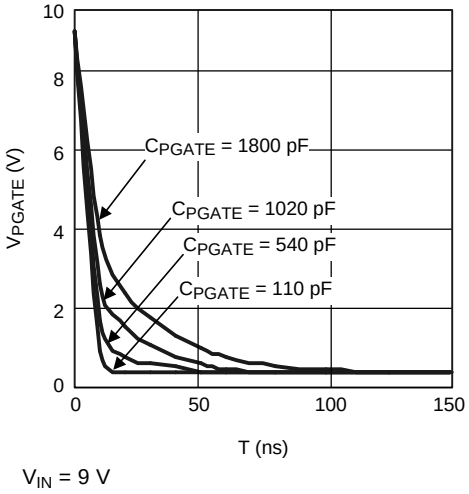


Figure 7. PGATE Voltage vs Input Voltage



V_{IN} = 9 V

Figure 8. Typical V_{PGATE} vs Time

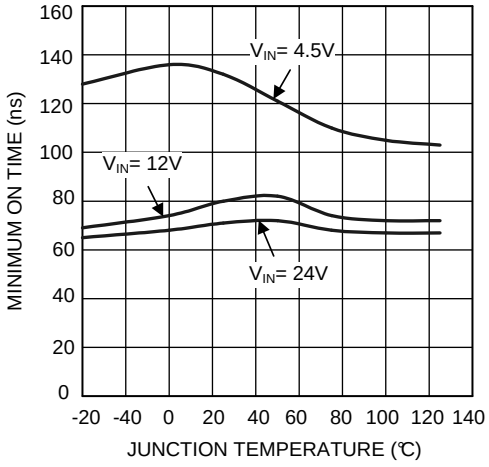
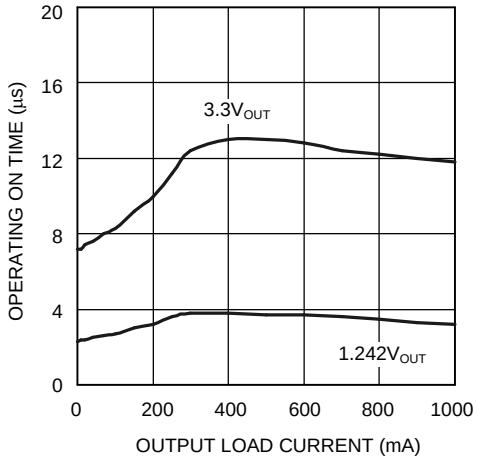
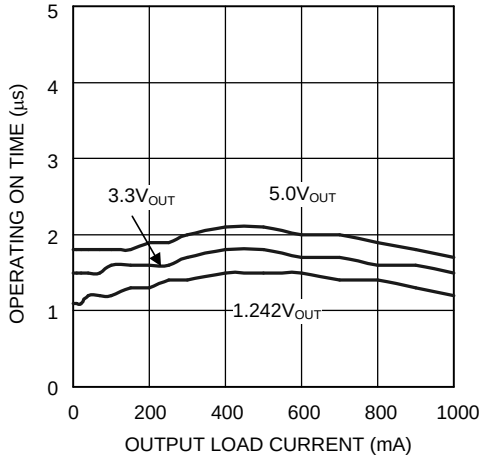


Figure 9. Minimum ON-Time vs Temperature



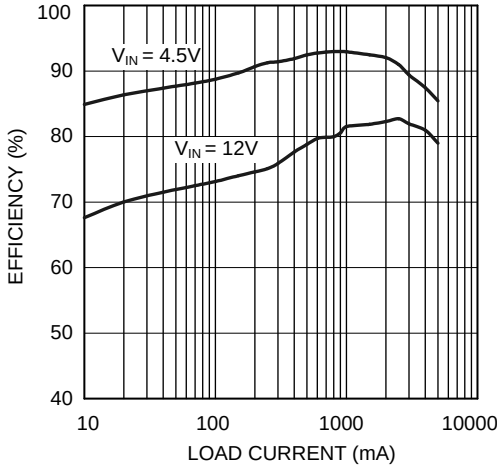
V_{IN} = 4.5 V

Figure 10. Operating ON-Time vs Output Load Current



V_{IN} = 12 V

Figure 11. Operating ON-Time vs Output Load Current

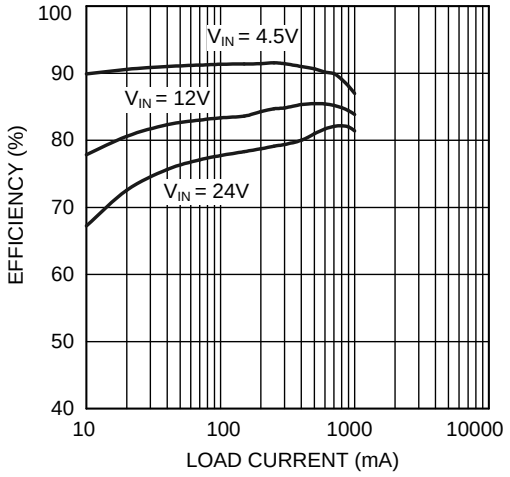


V_{OUT} = 3.3 V L = 6.8 µH

Figure 12. Efficiency vs Load Current

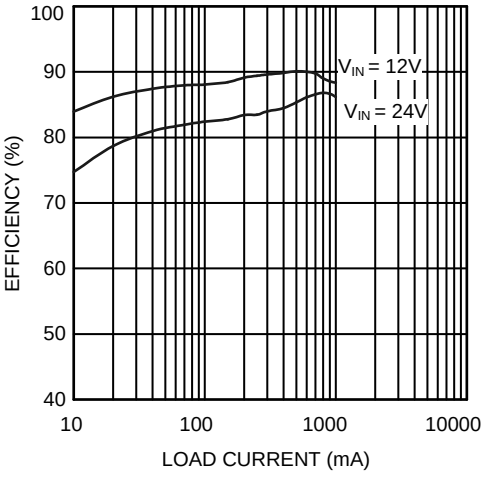
Typical Characteristics (continued)

Unless otherwise specified, T_J = 25°C



V_{OUT} = 3.3 V L = 22 µH

Figure 13. Efficiency vs Load Current



V_{OUT} = 5.0 V L = 22 µH

Figure 14. Efficiency vs Load Current

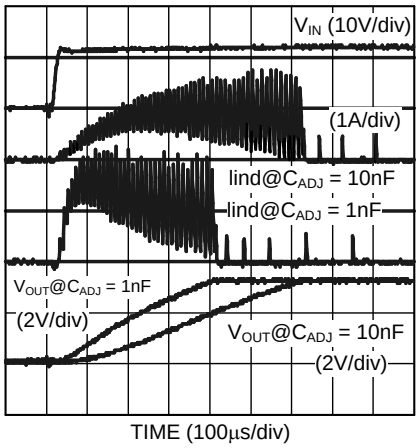
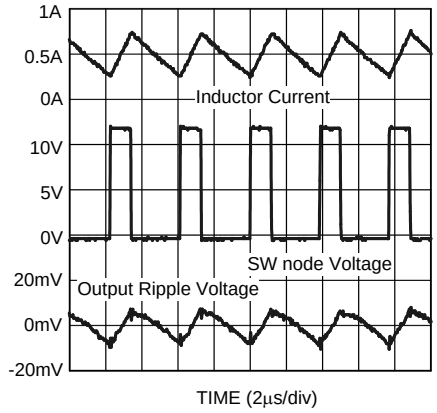
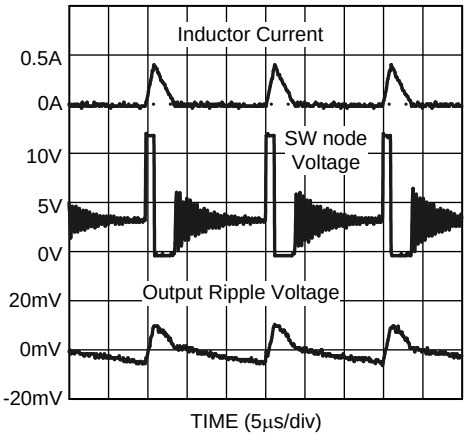


Figure 15. Start Up



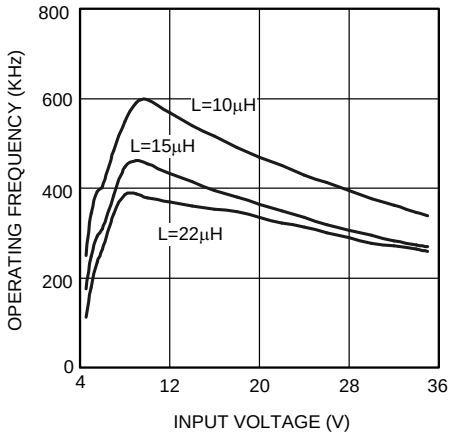
V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 500 mA
L = 22 µH

Figure 16. Continuous Mode Operation



V_{IN} = 12 V V_{OUT} = 3.3 V I_{OUT} = 50 mA
L = 22 µH

Figure 17. Discontinuous Mode Operation

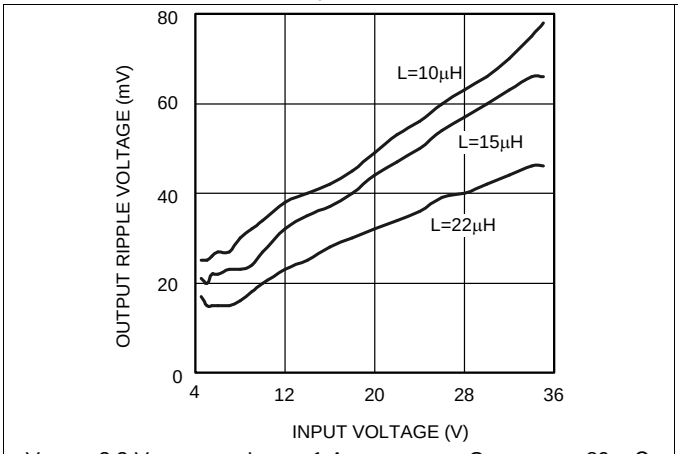


V_{OUT} = 3.3 V I_{OUT} = 1 A $C_{OUT(ESR)}$ = 80 mΩ
C_{ff} = 100 pF

Figure 18. Operating Frequency vs Input Voltage

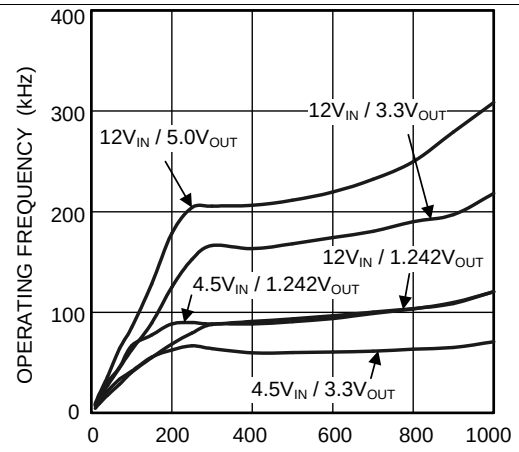
Typical Characteristics (continued)

Unless otherwise specified, T_J = 25°C



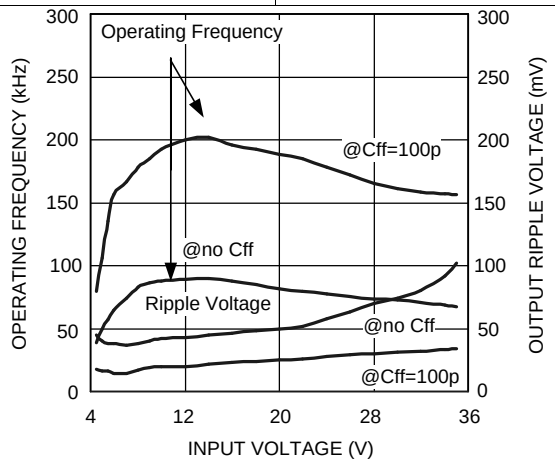
V_{OUT} = 3.3 V I_{OUT} = 1 A $C_{OUT(ESR)}$ = 80 mΩ
C_{ff} = 100 pF

Figure 19. Output Ripple Voltage vs Input Voltage



L = 22 µH $C_{OUT(ESR)}$ = 45 mΩ C_{ff} = 100 pF

Figure 20. Operating Frequency vs Output Load Current



V_{OUT} = 3.3 V
L = 22 µH
I_{OUT} = 500 mA

Figure 21. Feed-Forward Capacitor (Cff) Effect

7 Detailed Description

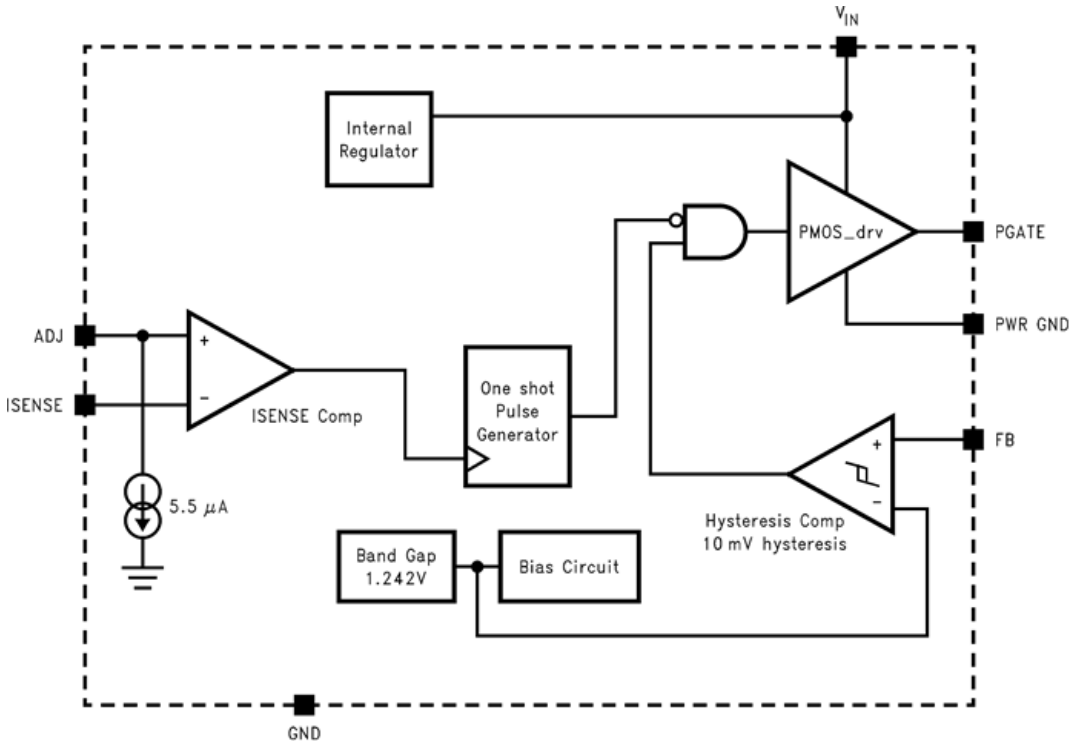
7.1 Overview

The LM3485 is buck (step-down) DC-DC controller that uses a hysteretic control scheme. The comparator is designed with approximately 10 mV of hysteresis. In response to the voltage at the FB pin, the gate drive (PGATE pin) turns the external PFET on or off. When the inductor current is too high, the current limit protection circuit engages and turns the PFET off for approximately 9 µs.

Hysteretic control does not require an internal oscillator. Switching frequency depends on the external components and operating conditions. Operating frequency reduces at light loads resulting in excellent efficiency compared to other architectures.

Two external resistors can easily program the output voltage. The output can be set in a wide range from 1.242-V (typical) to V_{IN}.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hysteretic Control Circuit

The LM3485 uses a comparator-based voltage control loop. The feedback is compared to a 1.242-V reference, and a 10-mV hysteresis is designed into the comparator to ensure noise free operation.

When the FB input to the comparator falls below the reference voltage, the output of the comparator moves to a low state. This results in the driver output, PGATE, pulling the gate of the PFET low and turning on the PFET. With the PFET on, the input supply charges Cout and supplies current to the load via the series path through the PFET and the inductor. Current through the Inductor ramps up linearly and the output voltage increases. As the FB voltage reaches the upper threshold, which is the internal reference voltage plus 10 mV, the output of the comparator changes from low to high, and the PGATE responds by turning the PFET off. As the PFET turns off, the inductor voltage reverses, the catch diode turns on, and the current through the inductor ramps down. Then, as the output voltage reaches the internal reference voltage again, the next cycle starts.

Feature Description (continued)

The LM3485 operates in discontinuous conduction mode at light load current or continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak, then ramps down to zero. Next cycle starts when the FB voltage reaches the internal voltage. Until then, the inductor current remains zero. Operating frequency is lower and switching losses reduce. In continuous conduction mode, current always flows through the inductor and never ramps down to zero.

The output voltage (V_{OUT}) can be programmed by two external resistors. It can be calculated as Equation 1:

$$V_{OUT} = 1.242 \times (R1 + R2) / R2 \quad (1)$$

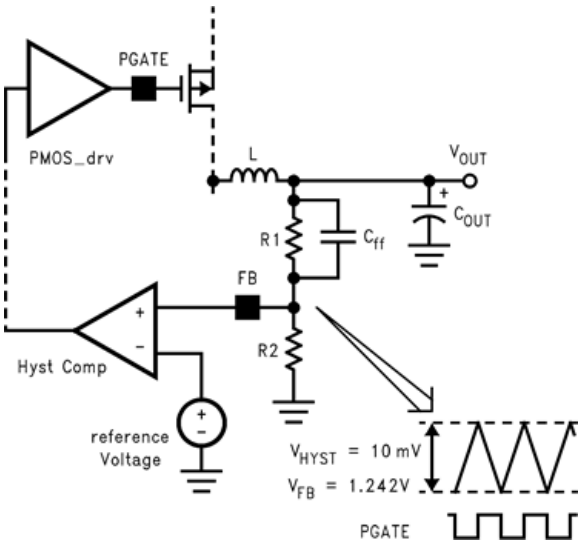


Figure 22. Hysteretic Window

The minimum output voltage ripple (V_{OUT_PP}) can be calculated in the same way.

$$V_{OUT\_PP} = V_{HYST} (R1 + R2) / R2 \quad (2)$$

For example, with V_{OUT} set to 3.3 V, V_{OUT_PP} is 26.6 mV

$$V_{OUT\_PP} = 0.01 \times (33K + 20K) / 20K = 0.0266 \text{ V} \quad (3)$$

Operating frequency (F) is determined by knowing the input voltage, output voltage, inductor, V_{HYST}, equivalent series resistance (ESR) of output capacitor, and the delay. It can be approximately calculated using Equation 4:

$$F = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT}) \times ESR}{(V_{HYST} \times \alpha \times L) + (V_{IN} \times delay \times ESR)} \quad (4)$$

where

- (R1 + R2) / R2
- delay: It includes the LM3485 propagation delay time and the PFET delay time

The propagation delay is 90-ns typically (see Figure 23).

Feature Description (continued)

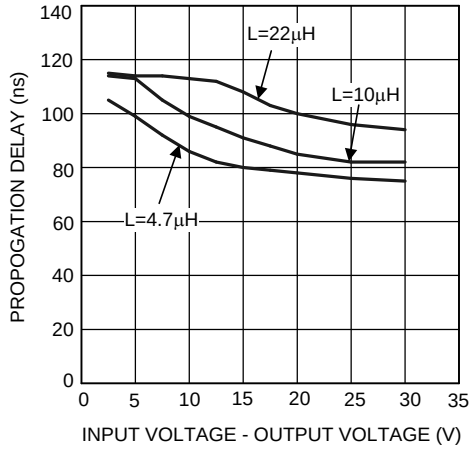


Figure 23. Propagation Delay

The operating frequency and output ripple voltage can also be significantly influenced by the speed up capacitor (Cff). Cff is connected in parallel with the high-side feedback resistor, R1. The location of this capacitor is similar to where a feed-forward capacitor would be located in a PWM control scheme. However, the effect on hysteretic operation is much different. The output ripple causes a current to be sourced or sunk through this capacitor. This current is essentially a square wave. Because the input to the feedback pin, FB, is a high impedance node, the current flows through R2. The end result is a reduction in output ripple and an increase in operating frequency. When adding Cff, calculate Equation 4 with α = 1. The value of Cff depends on the desired operating frequency and the value of R2. A good starting point is 470-pF ceramic at 100-kHz decreasing linearly with increased operating frequency. Also, as the output voltage is programmed below 2.5 V, the effect of Cff will decrease significantly.

7.3.2 Current Limit Operation

The LM3485 has a cycle-by-cycle current limit. Current limit is sensed across the V_{DS} of the PFET or across an additional sense resistor. When current limit is activated, the LM3485 turns off the external PFET for a period of 9 µs (typical). The current limit is adjusted by an external resistor, R_{ADJ}.

The current limit circuit is composed of the ISENSE comparator and the one-shot pulse generator. The positive input of the ISENSE comparator is the ADJ pin. An internal 5.5-µA current sink creates a voltage across the external R_{ADJ} resistor. This voltage is compared to the voltage across the PFET or sense resistor. The ADJ voltage can be calculated with Equation 5.

$$V_{ADJ} = V_{IN} - (R_{ADJ} \times 3.0\ \mu A)$$

where

- 3.0 µA is the minimum $I_{CL\text{-}ADJ}$ value (5)

The negative input of the ISENSE comparator is the ISENSE pin that should be connected to the drain of the external PFET. The inductor current is determined by sensing the V_{DS}. It can be calculated with Equation 6.

$$V_{ISENSE} = V_{IN} - (R_{DSON} \times I_{IND\_PEAK}) = V_{IN} - V_{DS} \quad (6)$$

Feature Description (continued)

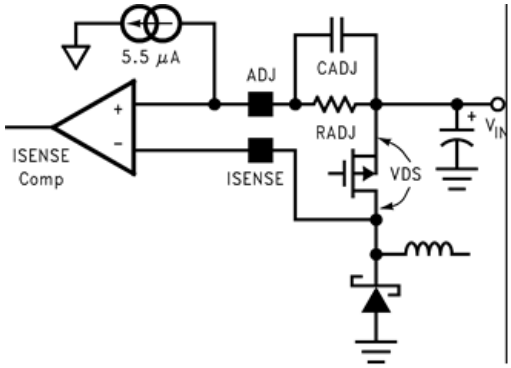


Figure 24. Current Sensing by V_{DS}

The current limit is activated when the voltage at the ADJ pin exceeds the voltage at the I_{SENSE} pin. The ISENSE comparator triggers the 9-µs one shot pulse generator forcing the driver to turn the PFET off. The driver turns the PFET back on after 9 µs. If the current has not reduced below the set threshold, the cycle will repeat continuously.

A filter capacitor, C_{ADJ}, should be placed as shown in Figure 24. C_{ADJ} filters unwanted noise so that the ISENSE comparator will not be accidentally triggered. A value of 100 pF to 1 nF is recommended in most applications. Higher values can be used to create a soft-start function (see *Start Up*).

The current limit comparator has approximately 100 ns of blanking time. This ensures that the PFET is fully on when the current is sensed. However, under extreme conditions such as cold temperature, some PFETs may not fully turn on within the blanking time. In this case, the current limit threshold must be increased. If the current limit function is used, the on time must be greater than 100 ns. Under low duty cycle operation, the maximum operating frequency will be limited by this minimum on time.

During current limit operation, the output voltage will drop significantly as will operating frequency. As the load current is reduced, the output will return to the programmed voltage. However, there is a current limit foldback phenomenon inherent in this current limit architecture. See Figure 25.

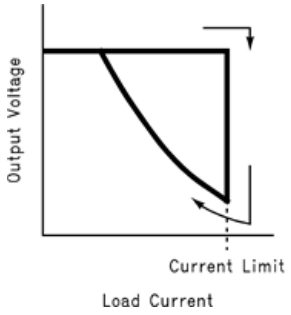


Figure 25. Current Limit Fold Back Phenomenon

At high input voltages (>28 V) increased undershoot at the switch node can cause an increase in the current limit threshold. To avoid this problem, a low Vf Schottky catch diode must be used (see *Catch Diode Selection (D1)*). Additionally, a resistor can be placed between the ISENSE pin and the switch node. Any value up to approximately 600 Ω is recommended.

7.4 Device Functional Modes

7.4.1 Start Up

The current limit circuit is active during start-up. During start-up the PFET will stay on until either the current limit or the feedback comparator is tripped

If the current limit comparator is tripped first then the fold back characteristic should be taken into account. Start-up into full load may require a higher current limit set point or the load must be applied after start-up.

One problem with selecting a higher current limit is inrush current during start-up. Increasing the capacitance (C_{ADJ}) in parallel with R_{ADJ} results in soft-start. C_{ADJ} and R_{ADJ} create an RC time constant forcing current limit to activate at a lower current. The output voltage will ramp more slowly when using the soft-start functionality. There are example start-up plots for C_{ADJ} equal to 1 nF and 10 nF in *Typical Characteristics*. Lower values for C_{ADJ} will have little to no effect on soft-start.

7.4.2 External Sense Resistor

The V_{DS} of a PFET will tend to vary significantly over temperature. This will result an equivalent variation in current limit. To improve current limit accuracy an external sense resistor can be connected from V_{IN} to the source of the PFET, as shown in Figure 26.

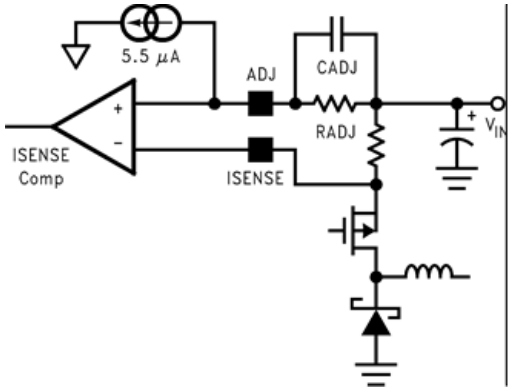


Figure 26. Current Sensing by External Resistor

7.4.3 PGATE

When switching, the PGATE pin swings from VIN (off) to some voltage below VIN (on). How far the PGATE will swing depends on several factors including the capacitance, on time, and input voltage.

As shown in the Typical Characteristics, PGATE voltage swing will increase with decreasing gate capacitance. Although PGATE voltage will typically be around VIN-5 V, with every small gate capacitances, this value can increase to a typical maximum of VIN-8.3 V.

Additionally, PGATE swing voltage will increase as on time increases. During long on times, such as when operating at 100% duty cycle, the PGATE voltage will eventually fall to its maximum voltage of VIN-8.3 V (typical) regardless of the PFET gate capacitance.

The PGATE voltage will not fall below 0.4 V (typical). Therefore, when the input voltage falls below approximately 9 V, the PGATE swing voltage range will be reduced. At an input voltage of 7 V, for instance, PGATE will swing from 7 V to a minimum of 0.4 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Hysteretic control is a simple control scheme. However the operating frequency and other performance characteristics highly depend on external conditions and components. If either the inductance, output capacitance, ESR, V_{IN}, or Cff is changed, there will be a change in the operating frequency and output ripple. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and C_{OUT} ESR.

8.2 Typical Application

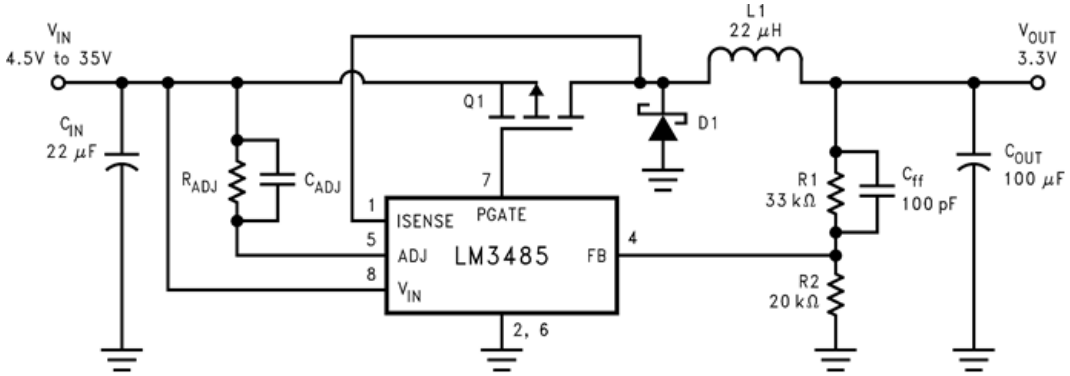


Figure 27. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETERS	VALUE
Input Voltage Range	7 V to 28 V
Output Voltage	3.3 V
Output Current Rating	1 A
Output Voltage Ripple	26.6 mV
Operating Frequency (VIN 12 V, Load Current 1 A)	210 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Step by Step Design Procedure

To begin the design process, the following items must be considered:

- Output current rating
- Input voltage range
- Output voltage
- Input voltage ripple
- Output voltage ripple

8.2.2.2 Inductor Selection (L1)

The important parameters for the inductor are the inductance and the current rating. The LM3485 operates over a wide frequency range and can use a wide range of inductance values. A good rule of thumb is to use the equations used for Simple Switcher®. The equation for inductor ripple (Δi) as a function of output current (I_{OUT}) for I_{out} < 2.0 Amps is Equation 7:

$$\Delta i \le I_{out} \times 0.386827 \times I_{out}^{-0.366726} \quad (7)$$

For I_{out} > 2.0 Amps, follow Equation 8:

$$\Delta i \le I_{out} \times 0.3 \quad (8)$$

The inductance can be calculated based upon the desired operating frequency using Equation 9 and Equation 10:

$$L = \frac{V_{IN} - V_{DS} - V_{OUT}}{\Delta i} \bullet \frac{D}{f} \quad (9)$$

$$D = \frac{V_{OUT} + V_D}{V_{IN} - V_{DS} + V_D}$$

where

- D is the duty cycle
- V_D is the diode forward voltage
- V_{DS} is the voltage drop across the PFET (10)

The inductor should be rated using Equation 11 and Equation 12:

$$Ipk = (Iout + \Delta i / 2) \times 1.1 \quad (11)$$

$$I_{RMS} = \sqrt{iout^2 + \frac{\Delta i^2}{3}} \quad (12)$$

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency. The second is the ESR.

8.2.2.3 Output Voltage Set Point

The output voltage (VOUT) can be programmed by two external resistors. It can be calculated using Equation 13.

$$VOUT = 1.242 \times (R1 + R2) / R2 \quad (13)$$

Refer to *Typical Application* . A good starting point is to select R2 to be in the range of 10 kΩ to 20 kΩ.

8.2.2.4 Output Capacitor Selection (C_{OUT})

The ESR of the output capacitor times the inductor ripple current is equal to the output ripple of the regulator. However, the V_{HYST} sets the first order value of this ripple. As ESR is increased with a given inductance, then operating frequency increases as well. If ESR is reduced then the operating frequency reduces.

The use of ceramic capacitors has become a common practice of many power supply designers. However, ceramic capacitors have a very low ESR resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low value resistor should be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provides highly accurate control over the output voltage ripple. The other types of capacitors, such as Sanyo POS CAP and OS-CON, Panasonic SP CAP, Nichicon *NA* series, are also recommended and may be used without additional series resistance.

For all practical purposes, any type of output capacitor may be used with proper circuit verification.

8.2.2.5 Input Capacitor Selection (C_{IN})

A bypass capacitor is required between the input source and ground. It must be located near the source pin of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer's recommended voltage derating. For high input voltage application, low ESR electrolytic capacitor, the Nichicon *UD* series or the Panasonic *FK* series, is available. The RMS current in the input capacitor can be calculated using Equation 14.

$$I_{RMS\_CIN} = I_{OUT} \times \frac{\left(V_{OUT} \times \left(V_{IN} - V_{OUT}\right)\right)^{1/2}}{V_{IN}} \quad (14)$$

The input capacitor power dissipation can be calculated using Equation 15.

$$P_{D(CIN)} = I_{RMS\_CIN}^2 \times ESR_{CIN} \quad (15)$$

The input capacitor must be able to handle the RMS current and the P_D. Several input capacitors may be connected in parallel to handle large RMS currents. In some cases it may be much cheaper to use multiple electrolytic capacitors than a single low ESR, high performance capacitor such as OS-CON or Tantalum. The capacitance value should be selected such that the ripple voltage created by the charge and discharge of the capacitance is less than 10% of the total ripple across the capacitor.

8.2.2.6 Programming the Current Limit (R_{ADJ})

The current limit is determined by connecting a resistor (R_{ADJ}) between input voltage and the ADJ pin.

$$R_{ADJ} = I_{IND\_PEAK} \times R_{DSON} / I_{CL\_ADJ}$$

where

- R_{DSON} : Drain-Source ON resistance of the external PFET
- I_{CL_ADJ} : 3.0 µA minimum
- $I_{IND\_PEAK} = I_{LOAD} + I_{RIPPLE} / 2$ (16)

Using the minimum value for I_{CL_ADJ} (3.0 µA) ensures that the current limit threshold will be set higher than the peak inductor current.

The R_{ADJ} value must be selected to ensure that the voltage at the ADJ pin does not fall below 3.5 V. With this in mind,

$$R_{ADJ\_MAX} = (V_{IN} - 3.5) / 7\ \mu A \quad (17)$$

If a larger R_{ADJ} value is needed to set the desired current limit, either use a PFET with a lower R_{DSON}, or use a current sense resistor as shown in Figure 26.

The current limit function can be disabled by connecting the ADJ pin to ground and ISENSE to V_{IN}.

8.2.2.7 Catch Diode Selection (D1)

The important parameters for the catch diode are the peak current, the peak reverse voltage, and the average power dissipation. The average current through the diode can be calculated using Equation 18.

$$I_{D\_AVE} = I_{OUT} \times (1 - D) \quad (18)$$

The off state voltage across the catch diode is approximately equal to the input voltage. The peak reverse voltage rating must be greater than input voltage. In nearly all cases a Schottky diode is recommended. In low output voltage applications a low forward voltage provides improved efficiency. For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

8.2.2.8 P-Channel MOSFET Selection (Q1)

The important parameters for the PFET are the maximum Drain-Source voltage (V_{DS}), the on resistance (R_{DSON}), Current rating, and the input capacitance.

The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The V_{DS} must be selected to provide some margin beyond the input voltage.

PFET drain current, Id, must be rated higher than the peak inductor current, $I_{IND\text{-}PEAK}$.

Depending on operating conditions, the PGATE voltage may fall as low as V_{IN} – 8.3 V. Therefore, a PFET must be selected with a V_{GS} greater than the maximum PGATE swing voltage.

As input voltage decreases below 9 V, PGATE swing voltage may also decrease. At 5.0-V input the PGATE will swing from V_{IN} to V_{IN} – 4.6 V. To ensure that the PFET turns on quickly and completely, a low threshold PFET should be used when the input voltage is less than 7 V.

However, PFET switching losses will increase as the V_{GS} threshold decreases. Therefore, whenever possible, a high threshold PFET should be selected. Total power loss in the FET can be approximated using Equation 19:

$$PDswitch = R_{DSON} \times I_{OUT}^2 \times D + F \times I_{OUT} \times V_{IN} \times (t_{on} + t_{off}) / 2 \quad (19)$$

where

- t_{on} = FET turnon time
- t_{off} = FET turnoff time

A value from 10 ns to 20 ns is typical for t_{on} and t_{off}.

A PFET should be selected with a turn on rise time of less than 100 ns. Slower rise times will degrade efficiency, can cause false current limiting, and in extreme cases may cause abnormal spiking at the PGATE pin.

The R_{DSON} is used in determining the current limit resistor value, R_{ADJ}.

NOTE

The R_{DSON} has a positive temperature coefficient. At 100°C, the R_{DSON} may be as much as 150% higher than the 25°C value. This increase in R_{DSON} must be considered it when determining R_{ADJ} in wide temperature range applications. If the current limit is set based upon 25°C ratings, then false current limiting can occur at high temperature.

Keeping the gate capacitance below 2000 pF is recommended to keep switching losses and transition times low. This will also help keep the PFET drive current low, which will improve efficiency and lower the power dissipation within the controller.

As gate capacitance increases, operating frequency should be reduced and as gate capacitance decreases operating frequency can be increased.

8.2.3 Application Curves

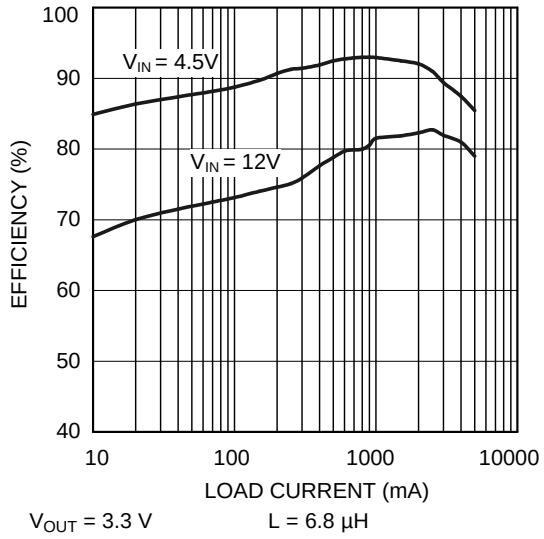


Figure 28. Efficiency vs Load Current

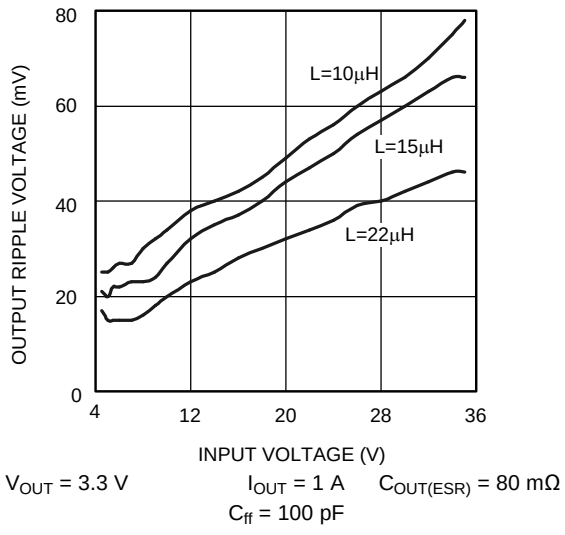


Figure 29. Output Ripple Voltage vs Input Voltage

9 Power Supply Recommendations

The devices are designed to generate from an input voltage supply range between 4.5 V and 35 V. The input should be well regulated. If the input supply is located more than a few inches from the LM3485 EVM, an additional bulk capacitor may be required. A tantalum capacitor with a valve of 47 µt as a typical choice.

10 Layout

10.1 Layout Guidelines

The PC board layout is very important in all switching regulator designs. Poor layout can cause switching noise into the feedback signal and general EMI problems. For minimal inductance, the wires indicated by heavy lines should be as wide and short as possible. Keep the ground pin of the input capacitor as close as possible to the anode of the diode. This path carries a large AC current. The switching node, the node with the diode cathode, inductor, and FET drain, should be kept short. This node is one of the main sources for radiated EMI because it is an AC voltage at the switching frequency. It is always good practice to use a ground plane in the design, particularly at high currents.

The two ground pins, PWR GND and GND, should be connected by as short a trace as possible; they can be connected underneath the device. These pins are resistively connected internally by approximately 50 Ω. The ground pins should be tied to the ground plane, or to a large ground trace in close proximity to both the FB divider and C_{OUT} grounds.

The gate pin of the external PFET should be located close to the PGATE pin. However, if a very small FET is used, a resistor may be required between PGATE and the gate of the FET to reduce high frequency ringing. Because this resistor will slow the rise time of the PFET, the current limit blanking time should be taken into consideration (see *Current Limit Operation*).

The feedback voltage signal line can be sensitive to noise. Avoid inductive coupling to the inductor or the switching node, by keeping the FB trace away from these areas.

10.2 Layout Example

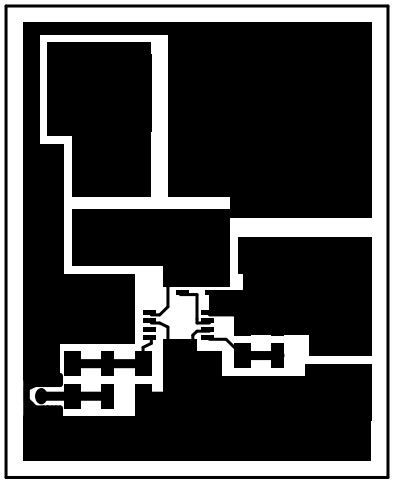


Figure 30. Top Layer,
Typical PCB Layout (3.3-V Output)

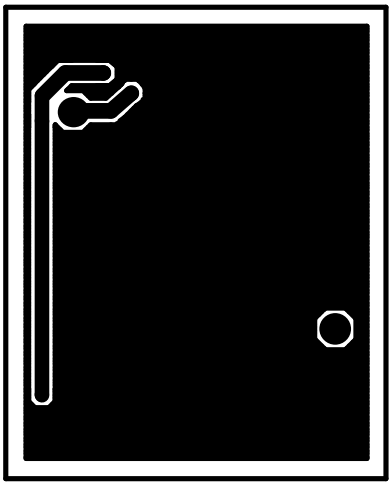


Figure 31. Bottom Layer,
Typical PCB Layout (3.3-V Output)

Layout Example (continued)

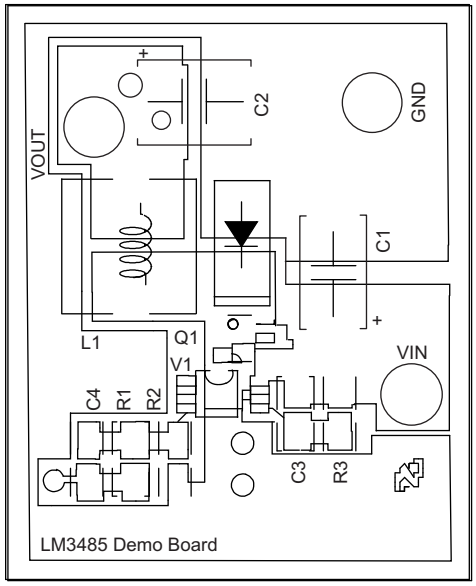


Figure 32. Silk Screen, Typical PCB Layout (3.3-V Output)

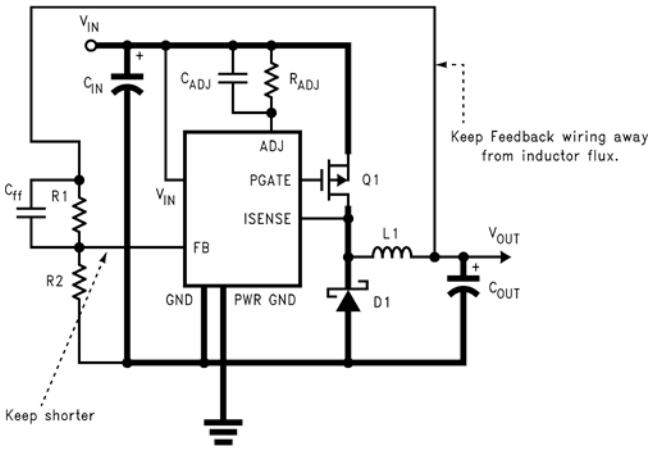


Figure 33. Typical PCB Layout Schematic (3.3-V Output)

Table 2. Typical Application BOM

DESIGNATOR		DESCRIPTION	PART NUMBER	DISTRIBUTOR
C1	C_{OUT}	22-µF to 35-V	EEJL1VD226R	Panasonic
C2	C_{IN}	100-µF to 6.3-V	6TPC100M	
C3	C_{ADJ}	1-nF ceramic chip capacitor		
C4	C_{FF}	100-pF ceramic chip capacitor		
D1		1 A to 40 V	MBRS140T3	On Semiconductor
L1		22 µH	QH66SN220M01L	Murata
Q1			FDC5614P	Fairchild
R1		33k-Ω chip resistor		
R2		20-kΩ chip resistor		
R3	R_{ADJ}	240-kΩ chip resistor		

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
Simple Switcher is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3485MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	S29B	Samples
LM3485MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	S29B	Samples
LM3485Q1MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SVJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM3485, LM3485-Q1 :

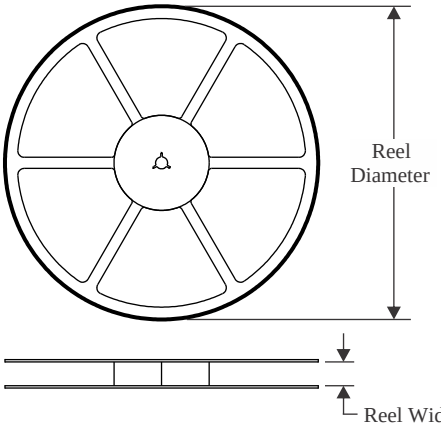
- Catalog: LM3485
- Automotive: LM3485-Q1

NOTE: Qualified Version Definitions:

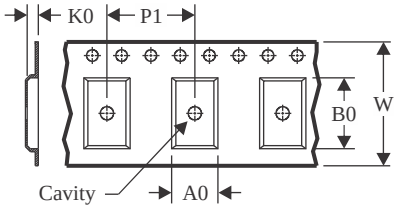
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

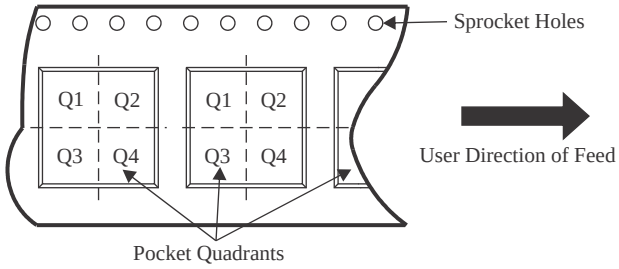


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

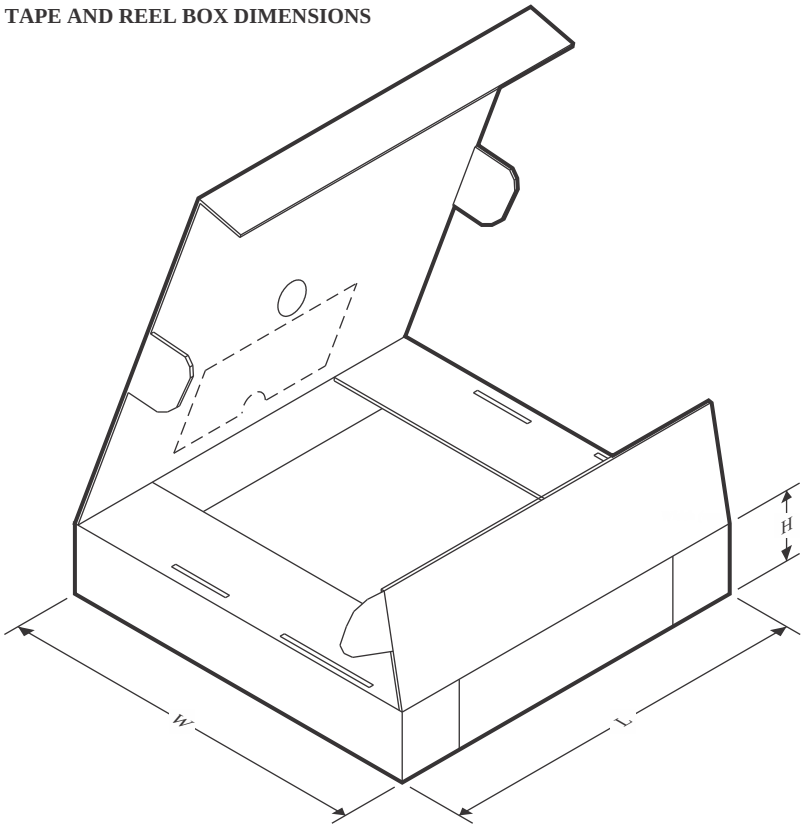
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3485MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3485MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3485Q1MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

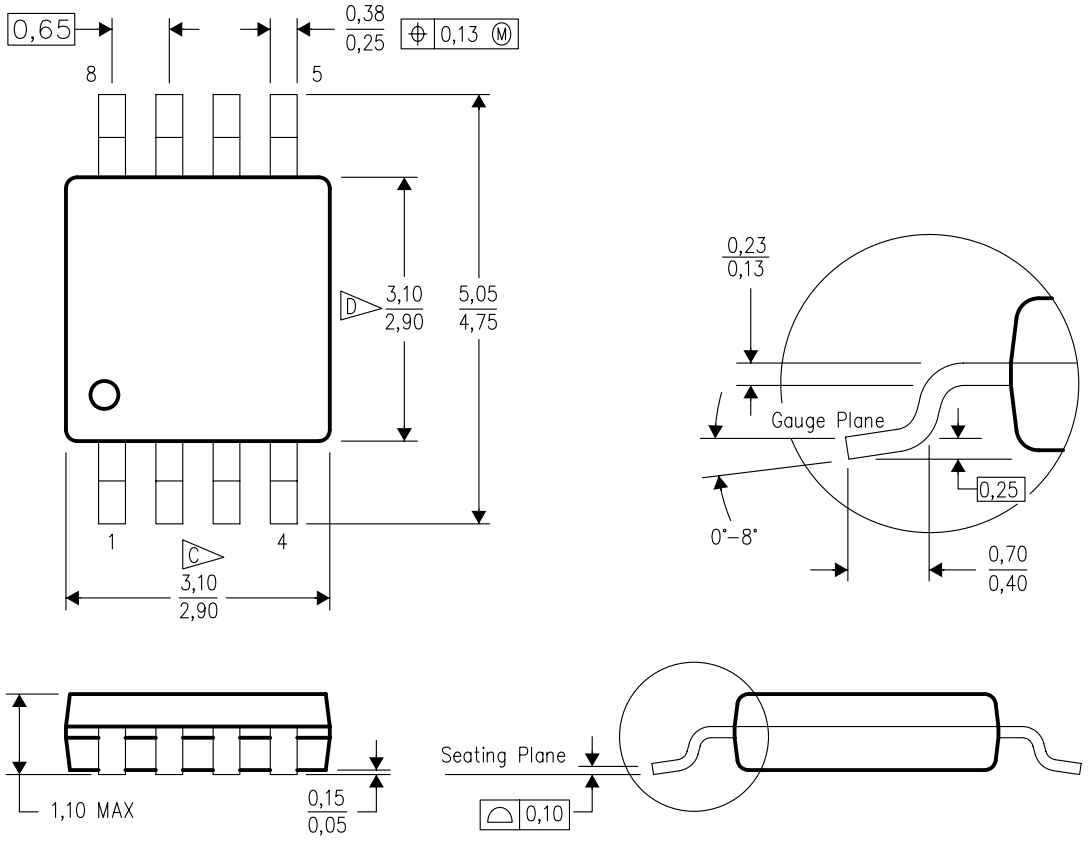
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3485MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM3485MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3485Q1MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0

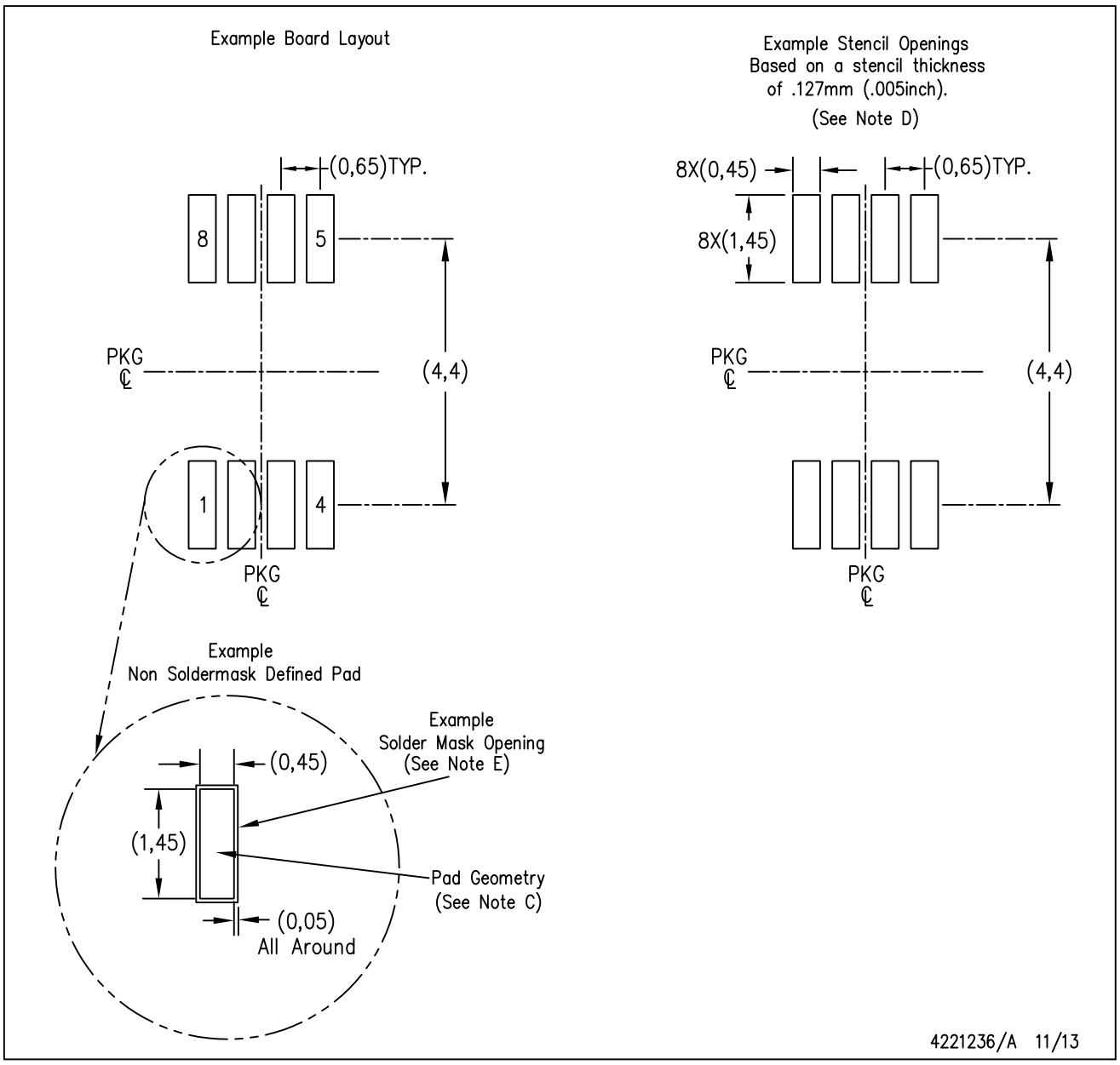
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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