TEXAS INSTRUMENTS

LP3878-ADJ

ZHCS589D – MAY 2005 – REVISED FEBRUARY 2015

LP3878-ADJ 用于 1V 至 5V 应用的微功耗 800mA 低噪声“陶瓷稳定”可调节稳压器

1 特性

- 输入电源电压：2.5V 至 16V
- 输出电压范围：1V 至 5.5V
- 设计用于与低等效串联电阻 (ESR) 陶瓷电容搭配使用
- 极低输出噪声
- 8 引脚小外形尺寸 (SO) PowerPAD™ 和晶圆级小外形无引线 (WSON) 表面贴装封装
- 关断模式下的静态电流 < 10μA
- 任意负载条件下的接地引脚电流均较低
- 过温和过流保护
- -40°C 至 125°C 的工作结温范围

2 应用

- 专用集成电路 (ASIC) 电源：
  - 台式机、笔记本电脑和图形卡
  - 机顶盒、打印机和复印机
- 数字信号处理 (DSP) 和现场可编程门阵列 (FPGA) 电源
- 开关模式电源 (SMPS) 后置稳压器
- 医疗仪器

3 说明

LP3878-ADJ 是一款 800mA 可调输出稳压器，设计用于使需要低至 1V 输出电压的应用获得高性能和低噪声。

凭借优化的垂直集成 PNP (VIP) 工艺，LP3878-ADJ 提供了以下出色性能：

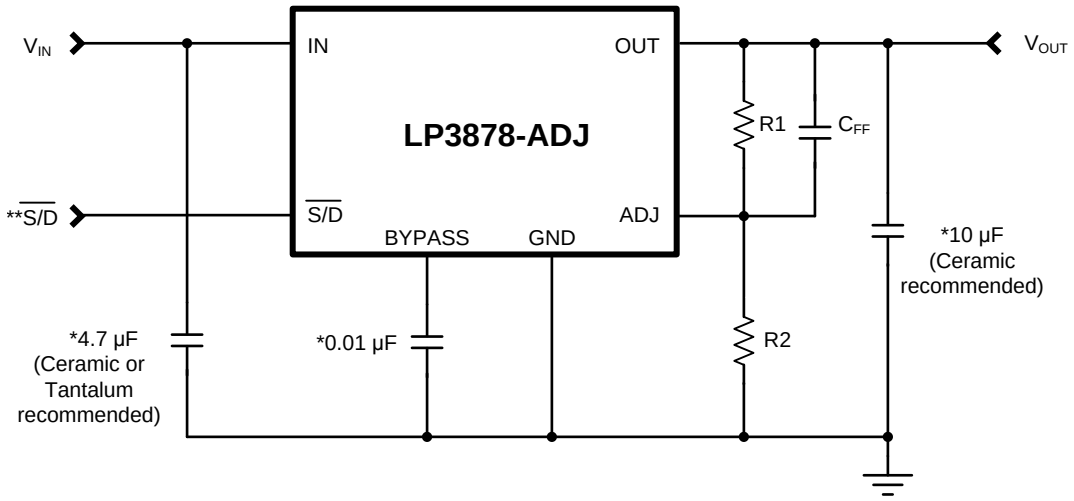
- 接地引脚电流：800mA 负载下的典型值为 5.5mA；100μA 负载下的典型值为 180μA。
- 低功耗关断：当 $\overline{\text{SHUTDOWN}}$ 引脚拉为低电平时，LP3878-ADJ 消耗的静态电流不到 10μA。
- 精密输出：确保室温下的输出电压精度为 1%。
- 低噪声：使用 10nF 旁路电容后，宽带输出噪声仅为 18μV（典型值）。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LP3878-ADJ	SO PowerPAD (8)	4.89mm × 3.90mm
	WSON (8)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

基本应用电路



* 图中显示的电容值是保证稳定性的最低要求。 选用更大的输出电容可改善动态响应。 输出电容必须满足 ESR 要求（请参见*Application Information*）。

** 必须主动禁止 $\overline{\text{SHUTDOWN}}$（或 $\overline{\text{S/D}}$）引脚（请参见*Device Functional Modes*）。 如果不使用该引脚，请将其连接至 IN（引脚 4）。

目录

4 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2014) to Revision D **Page**

- 已删除 VIP 的商标符号 - 不再是商标；在手册顶部导航栏处添加了参考设计图标 ... 1
- Deleted soldering info - now in POA ... 4
- Changed wording of footnote 5 to Ab Max Ratings ... 4
- Changed I_{OUT} to I_{OUT} throughout document ... 5
- Changed wording of *Reverse Input-Output Voltage* ... 11
- Changed outpin pin to OUT pin ... 15
- Added new paragraph to *Noise Bypass Capacitor* subsection ... 15

Changes from Revision B (April 2013) to Revision C **Page**

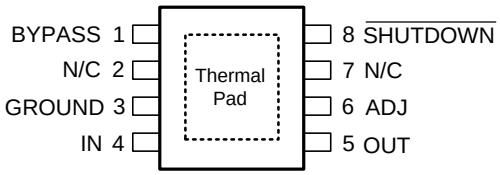
- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分；更新了热特性值 ... 1

Changes from Revision A (April 2013) to Revision B **Page**

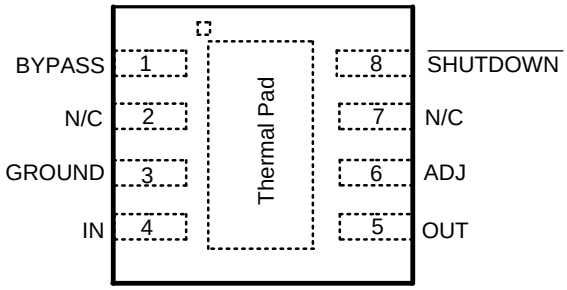
- Changed layout of National Data Sheet to TI format ... 16

5 Pin Configuration and Functions

SO PowerPAD (DDA) Package
8-Pin
Top View



WSON (NGT) Package
8-Pin
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
ADJ	6	I	Provides feedback to error amplifier from the resistive divider that sets the output voltage.
BYPASS	1	—	The capacitor connected between BYPASS and GROUND lowers output noise voltage level and is required for loop stability.
GROUND	3	—	Device ground.
IN	4	I	Input source voltage.
N/C	2		DO NOT CONNECT. Device pin 2 is reserved for post packaging test and calibration of the LP3878-ADJ V_{ADJ} accuracy. This pin must be left floating. Do not connect to any potential. Do not connect to ground. Any attempt to do pin continuity testing on device pin 2 is discouraged. Continuity test results will be variable depending on the actions of the factory calibration. Aggressive pin continuity testing (high voltage, or high current) on device pin 2 may activate the trim circuitry forcing V_{ADJ} to move out of tolerance.
N/C	7		No internal connection.
OUT	5	O	Regulated output voltage.
$\overline{\text{SHUTDOWN}}$	8	I	Output is enabled above turnon threshold voltage. Pull down to turn off regulator output.
Thermal Pad	—	—	The exposed thermal pad on the bottom of the package should be connected to a copper thermal pad on the PCB under the package. The use of thermal vias to remove heat from the package into the PCB is recommended. Connect the thermal pad to ground potential or leave floating. Do not connect the thermal pad to any potential other than the same ground potential seen at device pin 3. For additional information on using TI's Non Pull Back WSON package, see Application Note *AN-1187*, SNOA401.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
$\overline{\text{SHUTDOWN}}$ pin		1	kV
Power dissipation(3)	Internally Limited		
Input supply voltage (survival), V_{IN}	−0.3	16	V
ADJ pin	−0.3	6	V
Output voltage (survival), V_{OUT}(4)	−0.3	6	V
I_{OUT} (survival)	Short-Circuit Protected		
Input – output voltage (survival), $V_{IN} - V_{OUT}$(5)	−0.3	16	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military- or Aerospace-specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$. The value of $R_{\theta JA}$ for the WSON (NGT) and SO PowerPAD (DDA) packages are specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, see Application Note AN-1187, SNOA401. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(4) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP3878-ADJ output must be diode-clamped to ground.
(5) The PNP pass element contains a parasitic diode between the IN pin and the OUT pin that is normally reverse-biased. Forcing the OUT pin voltage above the IN pin voltage will turn on this diode and may induce a latch-up mode which can damage the part (see *Application and Implementation*).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	2.5	16	V
$V_{\overline{SD}}$	$\overline{\text{SHUTDOWN}}$ input voltage		V_{IN}	V
I_{OUT}	Output current		800	mA
T_J	Operating junction temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP3878-ADJ		UNIT
		DDA	NGT	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.5	38.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.0	27.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	26.5	15.2	
ψ_{JT}	Junction-to-top characterization parameter	8.0	0.2	
ψ_{JB}	Junction-to-board characterization parameter	26.4	15.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	4.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Limits are specified through design, testing, or correlation. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL). Unless otherwise specified: T_J = 25°C, V_{IN} = 3 V, V_{OUT} = 1 V, I_{OUT} = 1 mA, C_{OUT} = 10 µF, C_{IN} = 4.7 µF, $V_{\overline{SD}}$ = 2 V$V_{\overline{SD}}$, C_{BYPASS} = 10 nF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADJ}	Adjust pin voltage		0.99	1.00	1.01	V
		1 mA ≤ I_{OUT} ≤ 800 mA, 3 V ≤ V_{IN} ≤ 6 V	0.98	1.00	1.02	
		1 mA ≤ I_{OUT} ≤ 800 mA, 3 V ≤ V_{IN} ≤ 6 V –40°C ≤ T_J ≤ 125°C	0.97		1.03	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation	3 V ≤ V_{IN} ≤ 16 V		0.007	0.014	%/V
		3 V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C			0.032	
$V_{IN(MIN)}$	Minimum input voltage required to maintain output regulation	I_{OUT} = 800 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ – 1%		2.5		V
		I_{OUT} = 800 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ – 1% –40°C ≤ T_J ≤ 125°C			3.1	
		I_{OUT} = 800 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ – 1% 0 ≤ T_J ≤ 125°C		2.5		
		I_{OUT} = 800 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ – 1% 0 ≤ T_J ≤ 125°C, –40°C ≤ T_J ≤ 125°C			2.8	
		I_{OUT} = 750 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ – 1%		2.5		
		I_{OUT} = 750 mA, V_{OUT} ≥ $V_{OUT(NOM)}$ – 1% –40°C ≤ T_J ≤ 125°C			3.0	
V_{DOUT}	Dropout voltage(1) V_{OUT} = 3.8 V	I_{OUT} = 100 µA		1	2	mV
		I_{OUT} = 100 µA, –40°C ≤ T_J ≤ 125°C			3	
		I_{OUT} = 200 mA		150	200	
		I_{OUT} = 200 mA, –40°C ≤ T_J ≤ 125°C			300	
		I_{OUT} = 800 mA		475	600	
		I_{OUT} = 800 mA, –40°C ≤ T_J ≤ 125°C			1100	
I_{GND}	Ground pin current	I_{OUT} = 100 µA		180	200	µA
		I_{OUT} = 100 µA, –40°C ≤ T_J ≤ 125°C			225	
		I_{OUT} = 200 mA		1.5	2	mA
		I_{OUT} = 200 mA, –40°C ≤ T_J ≤ 125°C			3.5	
		I_{OUT} = 800 mA		5.5	8.5	
		I_{OUT} = 800 mA, –40°C ≤ T_J ≤ 125°C			15	
$I_{OUT(PK)}$	Peak output current	V_{OUT} ≥ $V_{OUT(NOM)}$ − 5%		1200		mA
$I_{OUT(MAX)}$	Short-circuit current	R_L = 0 Ω (steady state)		1300		
e_n	Output noise voltage (RMS)	Bandwidth = 100 Hz to 100 kHz, C_{BYPASS} = 10 nF		18		$\mu V_{(RMS)}$
$\Delta V_{OUT}/\Delta V_{IN}$	Ripple rejection	f = 1 kHz		60		dB
I_{ADJ}	ADJ pin bias current (sourcing)	I_{OUT} = 800 mA		200		nA
$\overline{\text{SHUTDOWN}}$ Input						
$V_{\overline{SD}}$	$\overline{\text{SHUTDOWN}}$ input voltage	V_H = Output ON		1.4		V
		V_H = Output ON, –40°C ≤ T_J ≤ 125°C			1.6	
		V_L = Output OFF, I_{IN} ≤ 10 µA		0.20		
		V_L = Output OFF, I_{IN} ≤ 10 µA –40°C ≤ T_J ≤ 125°C	0.04			
		V_{OUT} ≤ 10 mV, I_{IN} ≤ 50 µA		0.6		
$I_{\overline{SD}}$	$\overline{\text{SHUTDOWN}}$ input current	$V_{\overline{SD}}$ = 0 V		0.02		µA
		$V_{\overline{SD}}$ = 0 V, –40°C ≤ T_J ≤ 125°C			−1	
		$V_{\overline{SD}}$ = 5 V		5		
		$V_{\overline{SD}}$ = 5 V, –40°C ≤ T_J ≤ 125°C			15	

(1) Dropout voltage specification applies only if V_{IN} is sufficient so that it does not limit regulator operation.

6.6 Typical Characteristics

Unless otherwise specified: V_{IN} = 3.3 V, V_{OUT} = 1 V, I_{OUT} = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{\overline{SD}}$ = 2 V, C_{BYP} = 10 nF, T_J = 25°C.

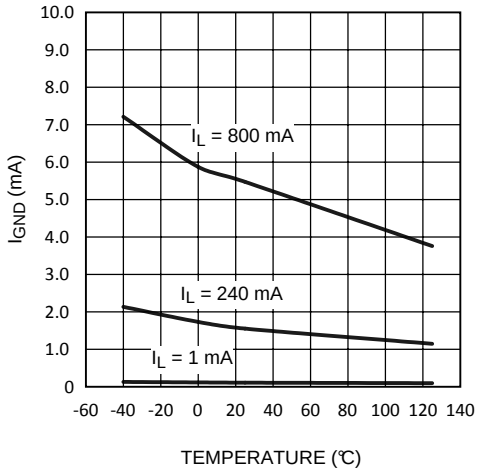


Figure 1. I_{GND} vs Temperature

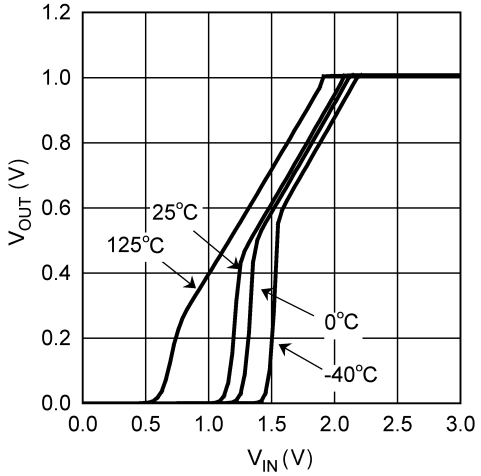


Figure 2. Minimum V_{IN} Over Temperature

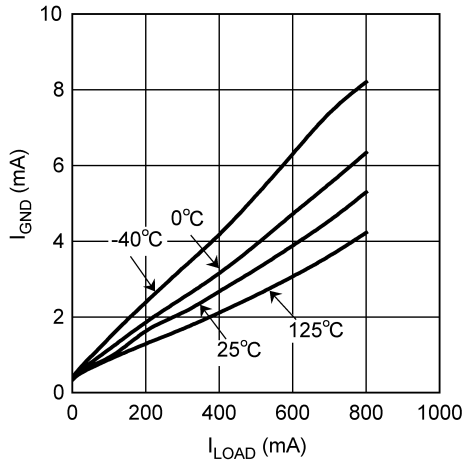


Figure 3. I_{GND} vs I_{Load}

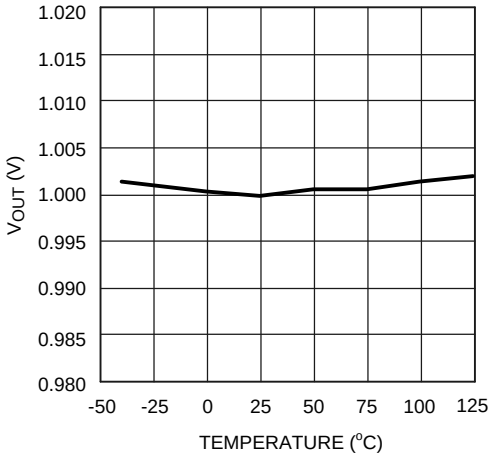


Figure 4. V_{OUT} vs Temperature

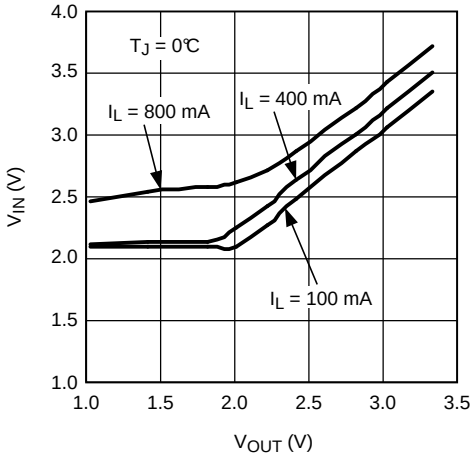


Figure 5. Minimum V_{IN} vs V_{OUT}

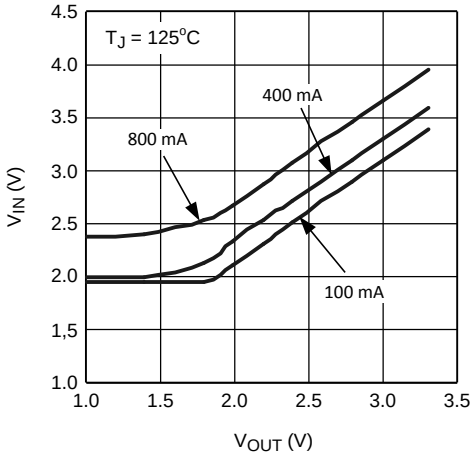


Figure 6. Minimum V_{IN} vs V_{OUT}

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3 V, V_{OUT} = 1 V, I_{OUT} = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{\overline{SD}}$ = 2 V, C_{BYP} = 10 nF, T_J = 25°C.

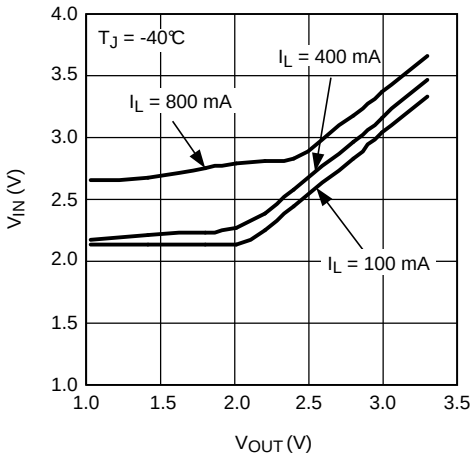


Figure 7. Minimum V_{IN} vs V_{OUT}

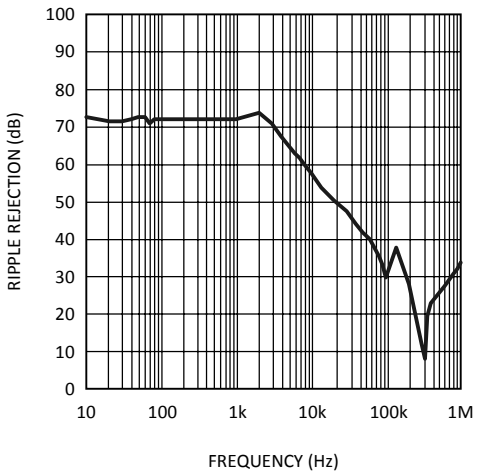


Figure 8. Ripple Rejection

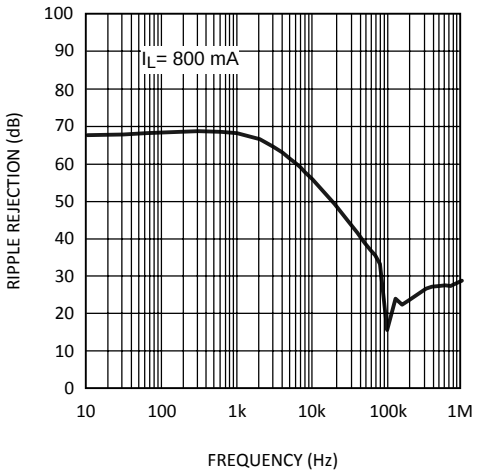


Figure 9. Ripple Rejection

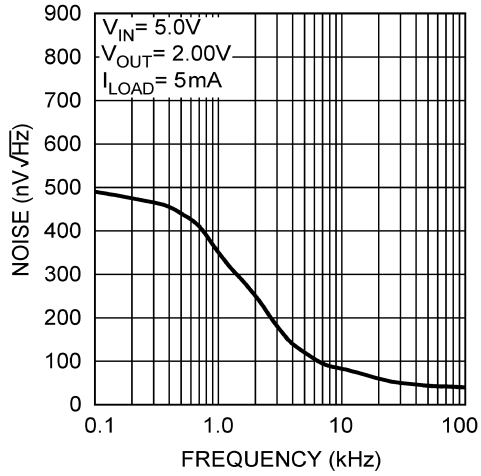


Figure 10. Output Noise Spectral Density

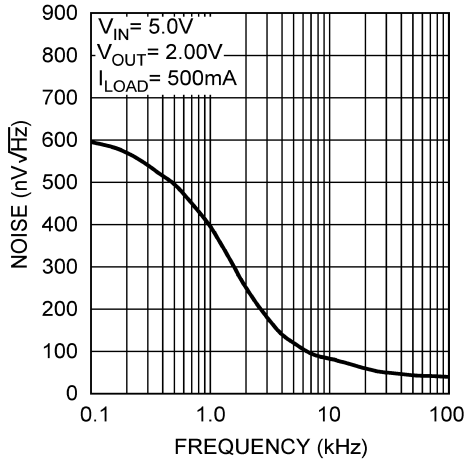


Figure 11. Output Noise Spectral Density

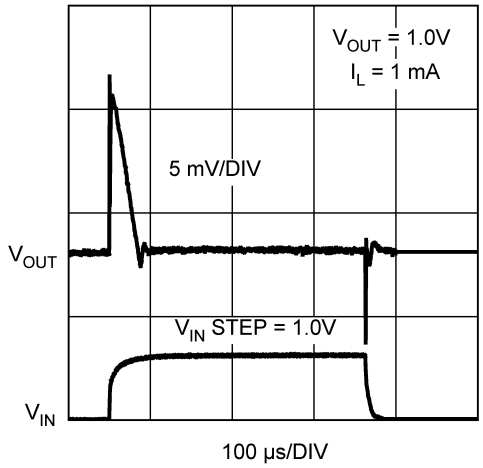


Figure 12. Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3 V, V_{OUT} = 1 V, I_{OUT} = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{\overline{SD}}$ = 2 V, C_{BYP} = 10 nF, T_J = 25°C.

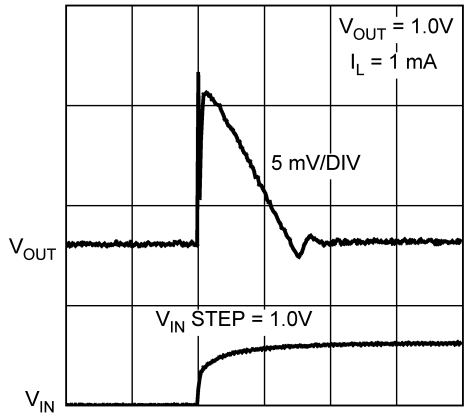


Figure 13. Line Transient Response

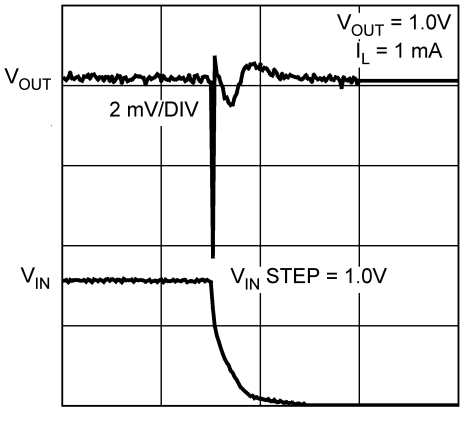


Figure 14. Line Transient Response

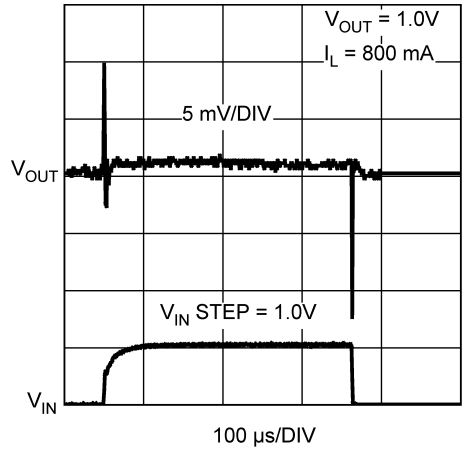


Figure 15. Line Transient Response

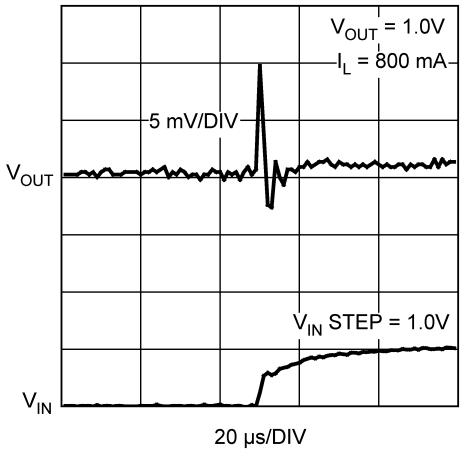


Figure 16. Line Transient Response

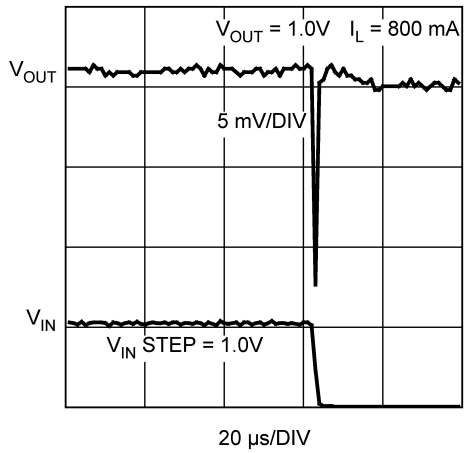


Figure 17. Line Transient Response

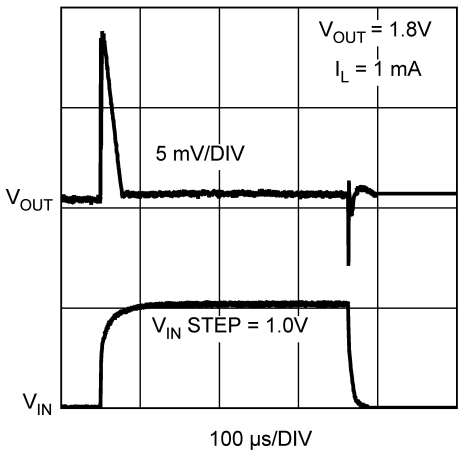


Figure 18. Line Transient Response

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3 V, V_{OUT} = 1 V, I_{OUT} = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{\overline{SD}}$ = 2 V, C_{BYP} = 10 nF, T_J = 25°C.

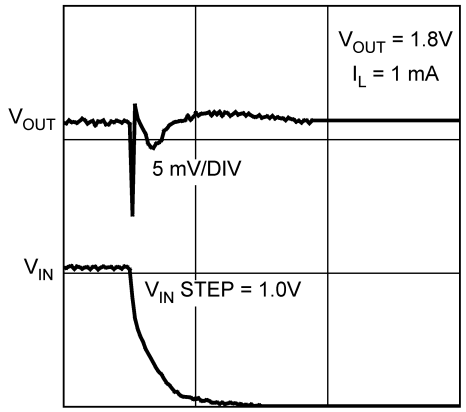


Figure 19. Line Transient Response

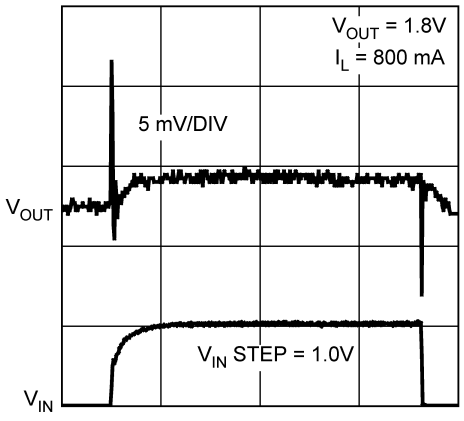


Figure 20. Line Transient Response

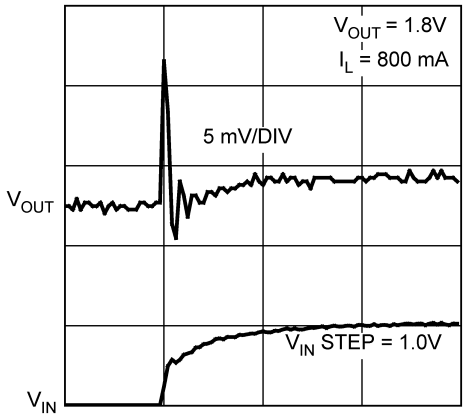


Figure 21. Line Transient Response

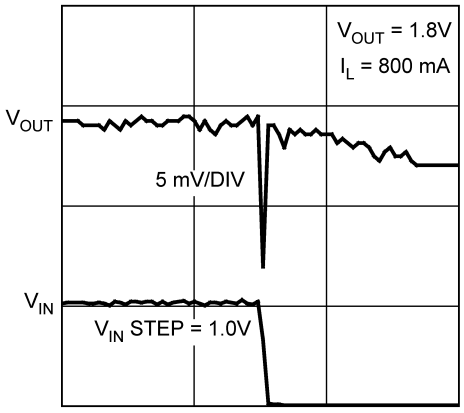


Figure 22. Line Transient Response

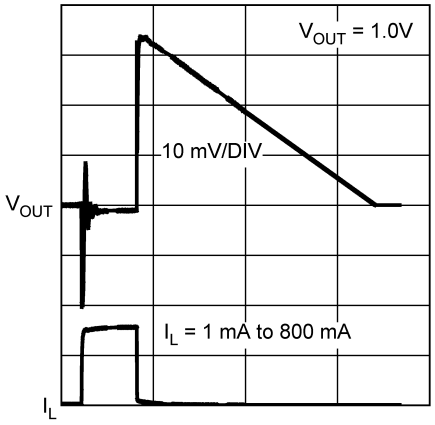


Figure 23. Load Transient Response

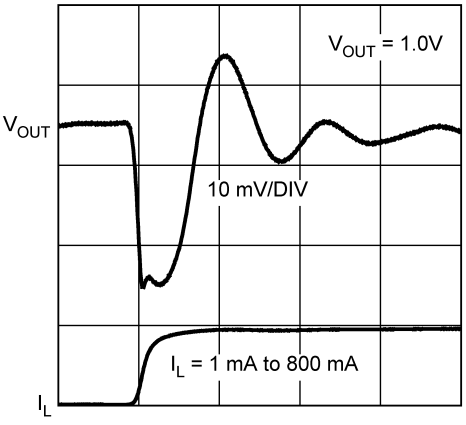


Figure 24. Load Transient Response

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 3.3 V, V_{OUT} = 1 V, I_{OUT} = 1 mA, C_{IN} = 4.7 µF, C_{OUT} = 10 µF, $V_{\overline{SD}}$ = 2 V, C_{BYP} = 10 nF, T_J = 25°C.

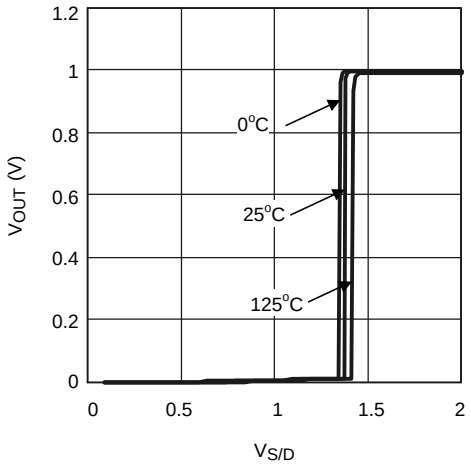


Figure 25. Turnon Characteristics

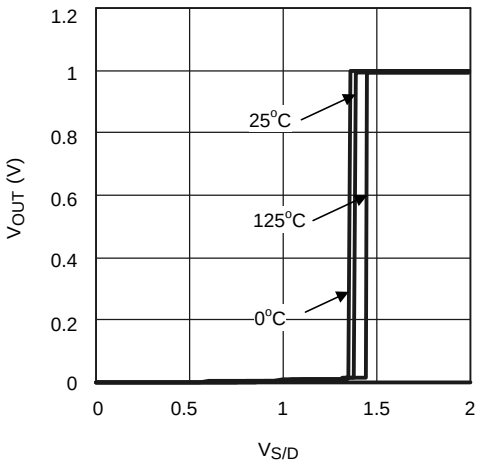


Figure 26. Turnoff Characteristics

7 Detailed Description

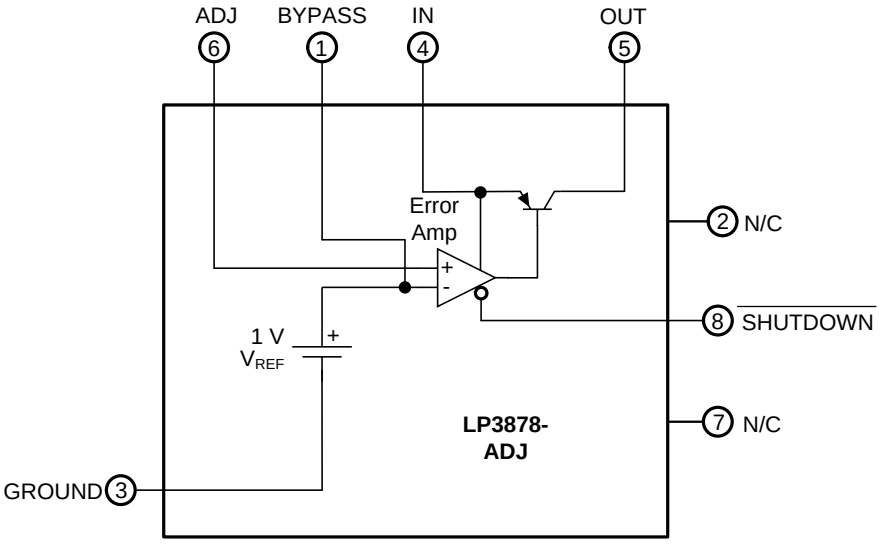
7.1 Overview

The LP3878-ADJ is an adjustable regulator; the output voltage can be set from 1 V to 5.5 V. The device can deliver 800-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are also included.

The LP3878-ADJ contains other features:

- Low power shutdown current and low ground pin current
- Very low output noise
- 8-lead SO PowerPAD or WSON surface-mount packages to allow for increased power dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Shutdown Input Operation

The LP3878-ADJ is shut off by pulling the $\overline{\text{SHUTDOWN}}$ input low, and turned on by pulling it high. If this feature is not to be used, the $\overline{\text{SHUTDOWN}}$ input should be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the $\overline{\text{SHUTDOWN}}$ input must be able to swing above and below the specified turnon or turnoff voltage thresholds listed in the *Electrical Characteristics* under $V_{ON/OFF}$.

7.3.2 Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP3878-ADJ contains a parasitic diode between the IN pin and the OUT pin. During normal operation (where the IN pin voltage is higher than the OUT pin voltage) this parasitic diode is reverse-biased. However, if the OUT pin voltage is pulled above the IN pin voltage this diode will turn ON, and current will flow into the LP3878-ADJ OUT pin.

In such cases, a parasitic SCR between the IN pin and the GND pin can latch ON which will allow a high current to flow from the VIN supply, into the IN pin to ground, which can damage the part. In any application where the OUT pin voltage may be higher than the IN pin voltage, even momentarily, an external Schottky diode must be connected from the IN pin to the OUT pin (cathode to IN pin, anode to OUT pin), to limit the reverse voltage across the LP3878-ADJ to 0.3 V (see *Absolute Maximum Ratings*).

7.3.3 Low Output Noise

With a 10-nF capacitor on the BYPASS pin, the output noise is only 18 µV.

7.4 Device Functional Modes

7.4.1 Operation With $V_{OUT(TARGET)}$ + 2 V ≤ V_{IN} ≤ 16 V

The device operates if the input voltage is equal to, or exceeds $V_{OUT(TARGET)}$ + 2 V. At input voltages below the minimum V_{IN} requirement, the device does not operate correctly and output voltage may not reach target value.

7.4.2 Operation With $\overline{\text{SHUTDOWN}}$ Pin Control

LP3878-ADJ is turned off by pulling the $\overline{\text{SHUTDOWN}}$ pin low, and turned on by pulling it high. If this feature is not used, the $\overline{\text{SHUTDOWN}}$ pin should be tied to V_{IN} to keep the regulator output on at all times. To assure proper operation, the signal source used to drive the $\overline{\text{SHUTDOWN}}$ input must be able to swing above and below the specified turnon and turnoff voltage thresholds listed in the *Electrical Characteristics* under V_L and V_H.

8 Application and Implementation

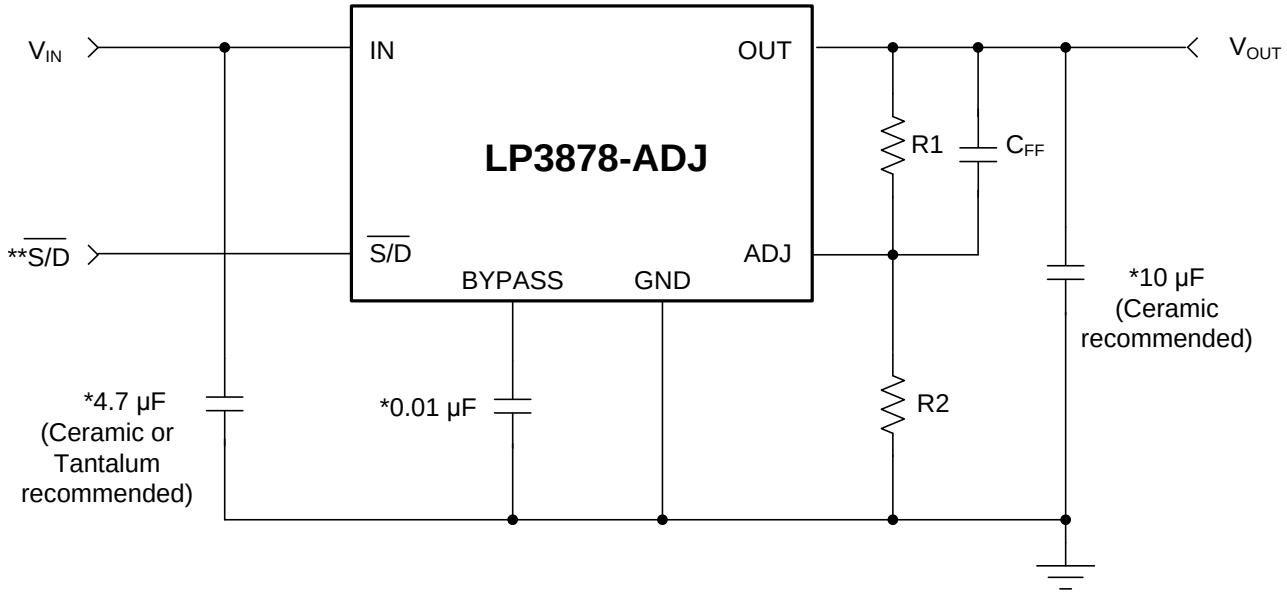
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3878-ADJ can provide 800-mA output current with 2.5-V to 6-V output voltage. A minimum 10-µF output capacitor is required for loop stability. An input capacitor of at least 4.7-µF is required also. The $\overline{\text{SHUTDOWN}}$ pin must be tied to input if not used. A 10-nF bypass capacitor is required to improve loop stability, it also can reduce noise on the regulator output significantly. A capacitor, C_{FF}, is required to increase phase margin and assure loop stability. Output voltage can be set by two resistors R1 and R2 (see Figure 27), and R2 must be less than 5 kΩ to ensure loop stability.

8.2 Typical Application



*Capacitor values shown are minimum required to assure stability. Larger output capacitor provides improved dynamic response. Output capacitor must meet ESR requirements (see *Application Information*).
**The $\overline{\text{SHUTDOWN}}$ (or $\overline{\text{S/D}}$) pin must be actively terminated (see *Device Functional Modes*). Tie to IN (pin 4) if not used.

Figure 27. Basic Application Circuit

8.2.1 Design Requirements

DESIGN PARAMETER	VALUE
Input voltage	3.8 V ±10%
Output voltage	1.8 V ±3%
Output current	800 mA (maximum)
Input capacitor	4.7 µF (minimum)
Output capacitor	10 µF (minimum)
Bypass capacitor	10 nF
External resistor R2	1 kΩ (less than 5 kΩ)

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

Like any low-dropout regulator, the LP3878-ADJ requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

8.2.2.1.1 Input Capacitor

A capacitor whose value is at least 4.7 µF (±20%) is required between the LP3878-ADJ input and ground. A good quality X5R or X7R ceramic capacitor should be used.

Capacitor tolerance and temperature variation must be considered when selecting a capacitor (see *Capacitor Characteristics*) to assure the minimum requirement of input capacitance is met over all operating conditions.

The input capacitor must be located not more than 0.5 inches from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum capacitor may be used, assuming the minimum input capacitance requirement is met.

8.2.2.1.2 Output Capacitor

The LP3878-ADJ requires a ceramic output capacitor whose size is at least 10 µF (±20%). A good quality X5R or X7R ceramic capacitor should be used. Capacitance tolerance and temperature characteristics must be considered when selecting an output capacitor.

The LP3878-ADJ is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an ultra-low equivalent series resistance (ESR) output capacitor.

The output capacitor selected must meet the requirement for minimum amount of capacitance and also have an ESR value which is within the stable range. A curve is provided which shows the stable ESR range as a function of load current (see Figure 28).

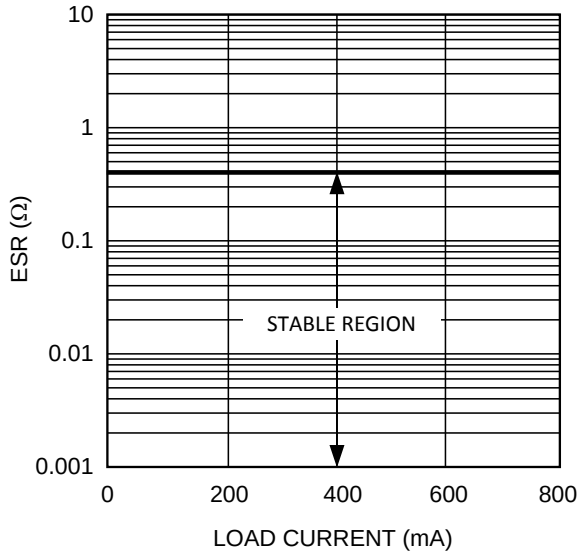


Figure 28. Stable Region for Output Capacitor ESR

NOTE

Important: The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

The output capacitor ESR forms a zero which is required to add phase lead near the loop gain crossover frequency, typically in the range of 50 kHz to 200 kHz. The ESR at lower frequencies is of no importance. Some capacitor manufacturers list ESR at low frequencies only, and some give a formula for Dissipation Factor (DF) which can be used to calculate a value for a term referred to as ESR. However, because the DF formula is usually at a much lower frequency than the range listed above, it will give an unrealistically high value. If good quality X5R or X7R ceramic capacitors are used, the actual ESR in the 50-kHz to 200-kHz range will not exceed 25 mΩ. If these are used as output capacitors for the LP3878-ADJ, the regulator stability requirements are satisfied.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range (see *Capacitor Characteristics*).

The output capacitor must be located not more than 0.5 inches from the OUT pin and returned to a clean analog ground.

8.2.2.1.3 Noise Bypass Capacitor

The 10-nF capacitor on the BYPASS pin significantly reduces noise on the regulator output and is required for loop stability. However, the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few µA flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, dc leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10-nF polypropylene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

While the capacitor value on the BYPASS will affect start-up time, this is not intended to be used as a soft-start circuit. There is no dedicated discharge circuitry for this capacitor, and it can be pre-biased if the IN pin, or the SHUTDOWN pin are not at 0 V at start-up.

8.2.2.2 Feedforward Capacitor

The feedforward capacitor designated C_{FF} in Figure 27 is required to increase phase margin and assure loop stability. Improved phase margin also gives better transient response to changes in load or input voltage, and faster settling time on the output voltage when transients occur. C_{FF} forms both a pole and zero in the loop gain, the zero providing beneficial phase lead (which increases phase margin) and the pole adding undesirable phase lag (which should be minimized). The zero frequency is determined both by the value of C_{FF} and R1:

$$f_Z = 1 / (2\pi C_{FF} \times R1) \quad (1)$$

The pole frequency resulting from C_{FF} is determined by the value of C_{FF} and the parallel combination of R1 and R2:

$$f_P = 1 / (2\pi C_{FF} \times (R1 // R2)) \quad (2)$$

At higher output voltages where R1 is much greater than R2, the value of R2 primarily determines the value of the parallel combination of R1 // R2. This puts the pole at a much higher frequency than the zero. As the regulated output voltage is reduced (and the value of R1 decreases), the parallel effect of R2 diminishes and the two equations become equal (at which point the pole and zero cancel out). Because the pole frequency gets closer to the zero at lower output voltages, the beneficial effects of C_{FF} are increased if the frequency range of the zero is shifted slightly higher for applications with low V_{OUT} (because then the pole adds less phase lag at the loop crossover frequency).

C_{FF} should be selected to place the pole-zero pair at a frequency where the net phase lead added to the loop at the crossover frequency is maximized. The following design guidelines were obtained from bench testing to optimize phase margin, transient response, and settling time:

- For $V_{OUT} \leq 2.5$ V: C_{FF} should be selected to set the zero frequency in the range of about 50 kHz to 200 kHz.

- For V_{OUT} > 2.5 V: C_{FF} should be selected to set the zero frequency in the range of about 20 kHz to 100 kHz.

8.2.2.3 Capacitor Characteristics

8.2.2.3.1 Ceramic

The LP3878-ADJ was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 10-µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 10-µF ceramic capacitor is in the range of 5 mΩ to 10 mΩ, which meets the ESR limits required for stability by the LP3878-ADJ.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Many large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

Another significant problem with Z5U and Y5V dielectric devices is that the capacitance drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it.

For these reasons, X7R and X5R type ceramic capacitors must be used on the input and output of the LP3878-ADJ.

8.2.2.4 Setting the Output Voltage

The output voltage is set using resistors R1 and R2 (see Figure 27).

The formula for output voltage is:

$$V_{OUT} = V_{ADJ} \times (1 + (R1 / R2)) \quad (3)$$

R2 must be less than 5 kΩ to ensure loop stability.

To prevent voltage errors, R1 and R2 must be located near the LP3878-ADJ and connected via traces with no other currents flowing in them (Kelvin connect). The bottom of the R1/R2 divider must be connected directly to the LP3878-ADJ ground pin.

8.2.3 Application Curves

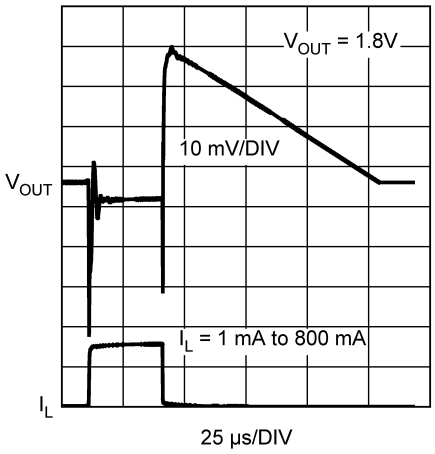


Figure 29. Load Transient Response

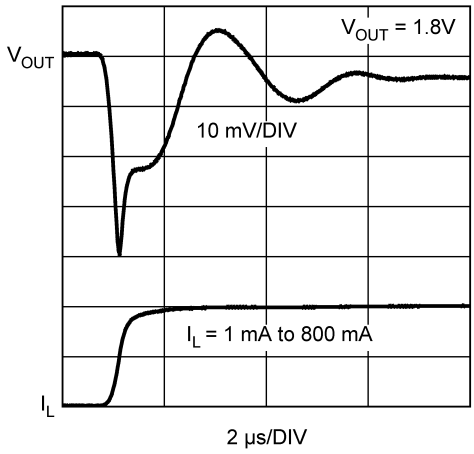


Figure 30. Load Transient Response

9 Power Supply Recommendations

The LP3878-ADJ is designed to operate from an input voltage supply range between 2.5 V and 16 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. An input capacitor of at least 4.7 µF is required.

10 Layout

10.1 Layout Guidelines

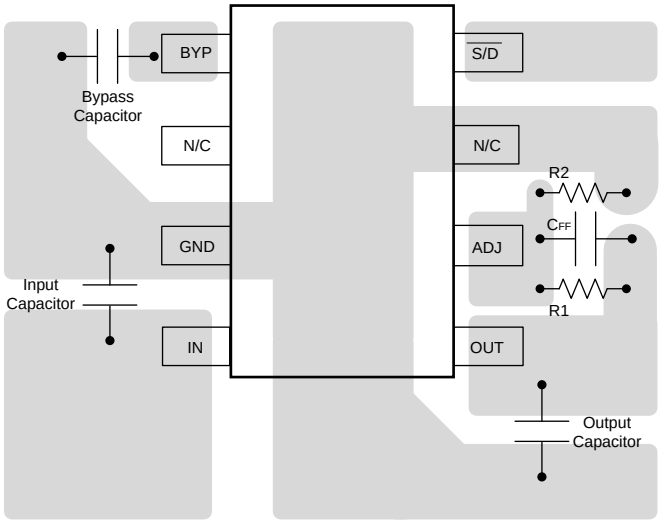
Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a single point ground.

It should be noted that stability problems have been seen in applications where vias to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single-point ground technique for the regulator and its capacitors fixed the problem.

Because high current flows through the traces going into IN and coming from OUT, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

10.2 Layout Example



10.3 Power Dissipation

The LP3878-ADJ is offered in the 8-lead SO PowerPAD or WSON surface-mount packages to allow for increased power dissipation compared to the SO-8 and Mini SO-8. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note *AN-1187*, SNOA401.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

应用手册 *AN-1187*，SNOA401

11.2 商标

PowerPAD is a trademark of Texas Instruments.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3878MR-ADJ	NRND	SO PowerPAD	DDA	8	95	Non-RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 125	3878 MRADJ	
LP3878MR-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	3878 MRADJ	Samples
LP3878MRX-ADJ/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	3878 MRADJ	Samples
LP3878SD-ADJ/NOPB	ACTIVE	WSON	NGT	8	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	3878ADJ	Samples
LP3878SDX-ADJ/NOPB	ACTIVE	WSON	NGT	8	4500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	3878ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

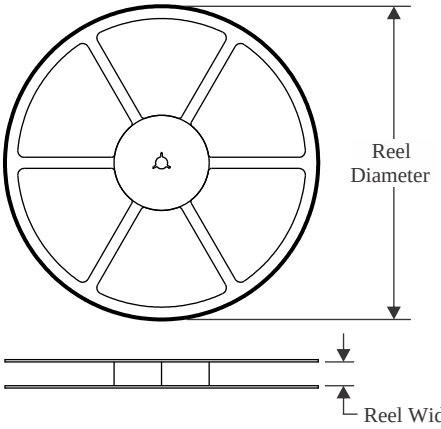
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

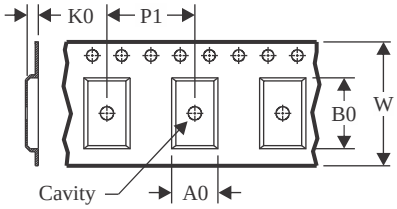
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

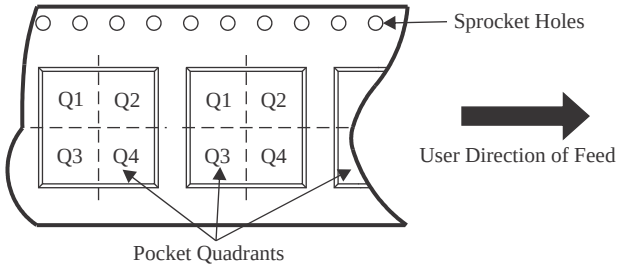


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

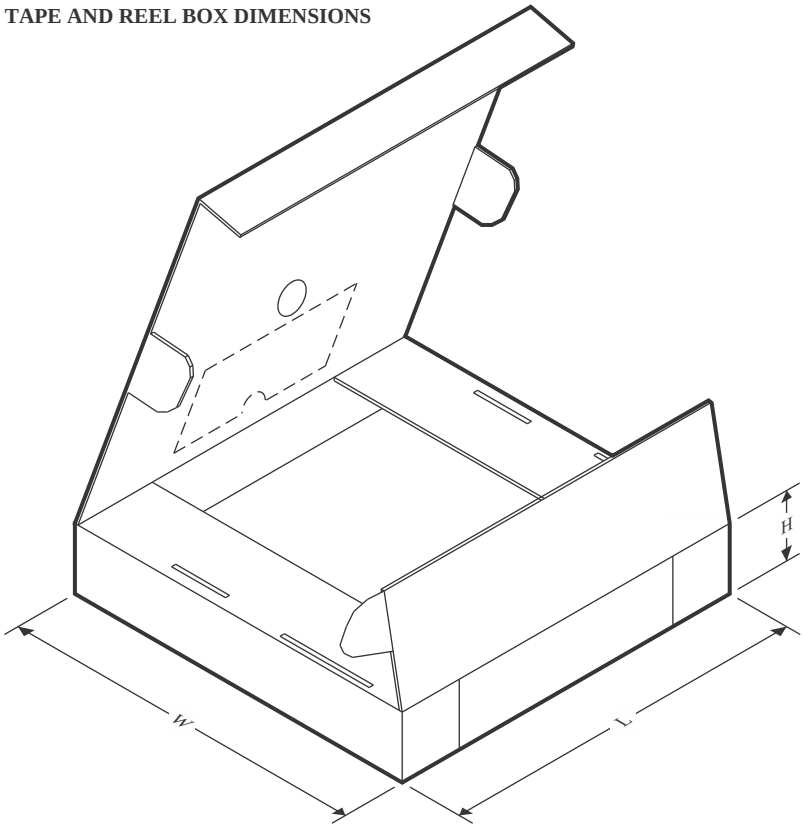
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3878MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP3878SD-ADJ/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3878SDX-ADJ/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3878SDX-ADJ/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

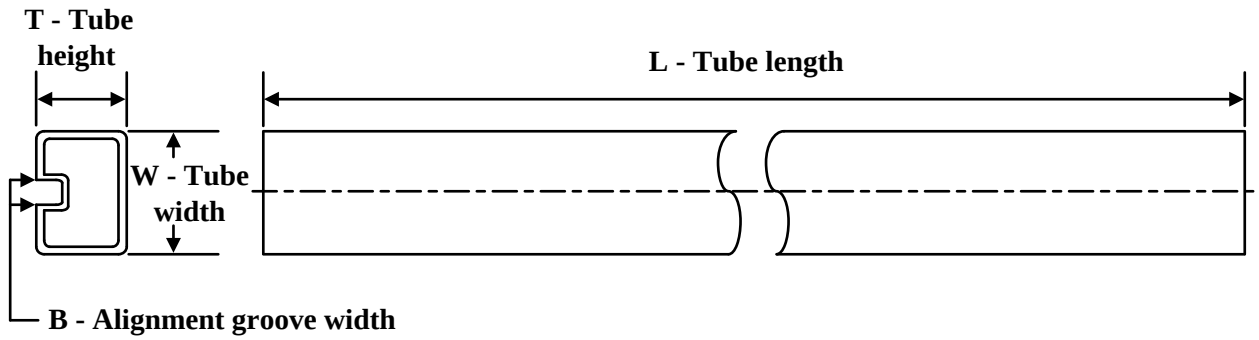
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3878MRX-ADJ/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
LP3878SD-ADJ/NOPB	WSON	NGT	8	1000	208.0	191.0	35.0
LP3878SDX-ADJ/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0
LP3878SDX-ADJ/NOPB	WSON	NGT	8	4500	346.0	346.0	35.0

TUBE



*All dimensions are nominal

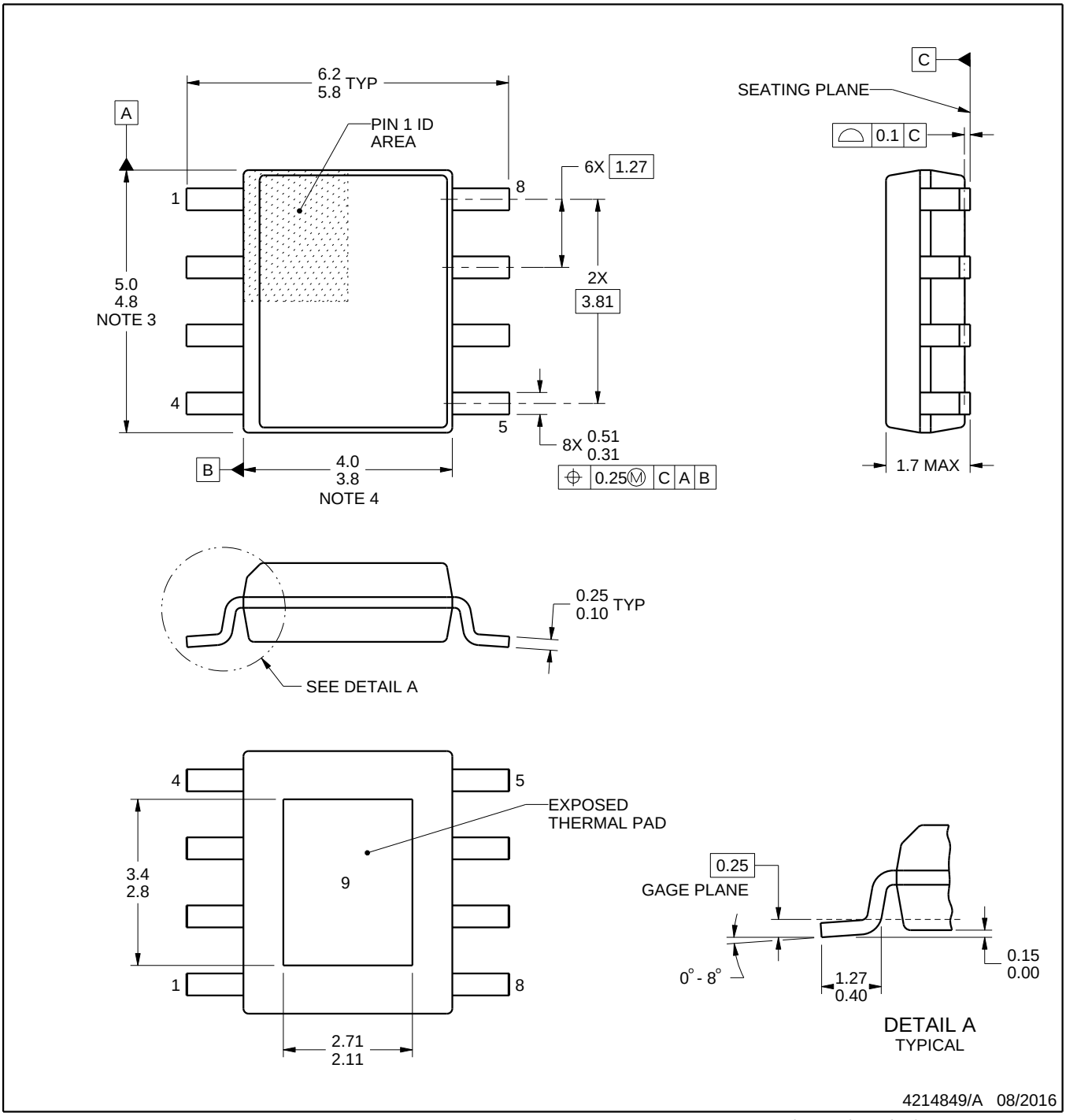
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP3878MR-ADJ	DDA	HSOIC	8	95	495	8	4064	3.05
LP3878MR-ADJ	DDA	HSOIC	8	95	495	8	4064	3.05
LP3878MR-ADJ/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

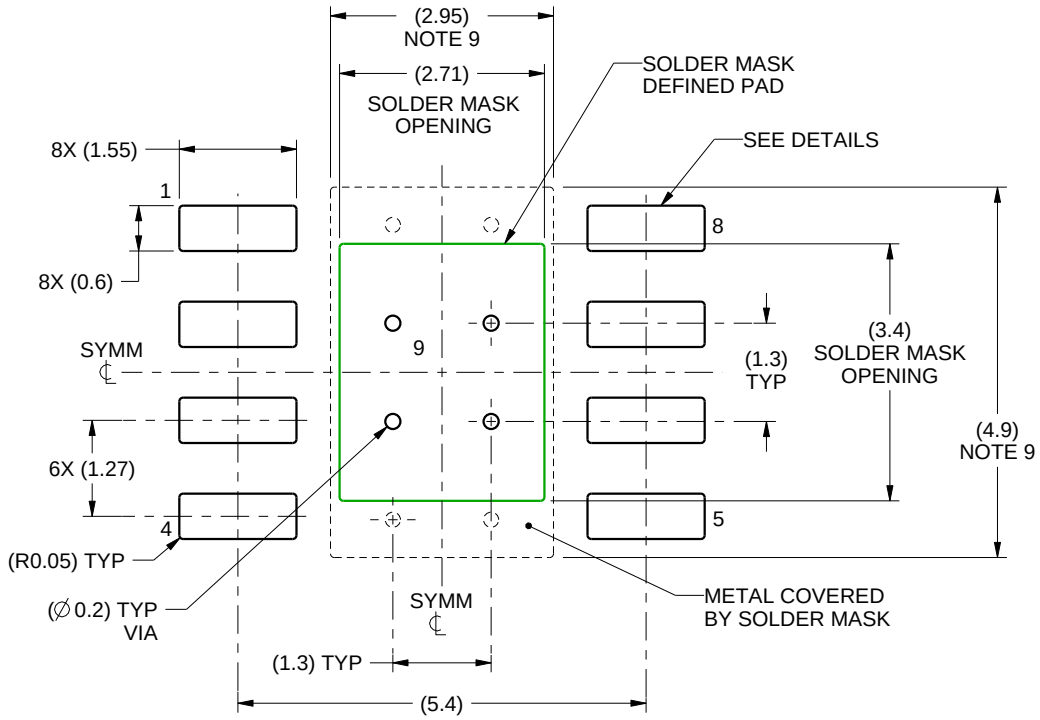
PLASTIC SMALL OUTLINE



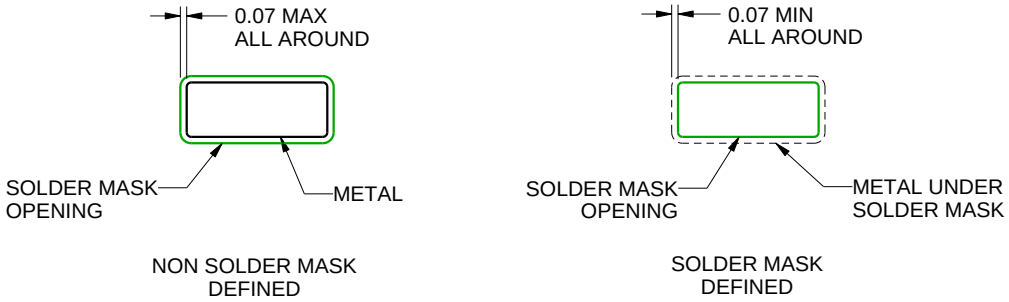
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

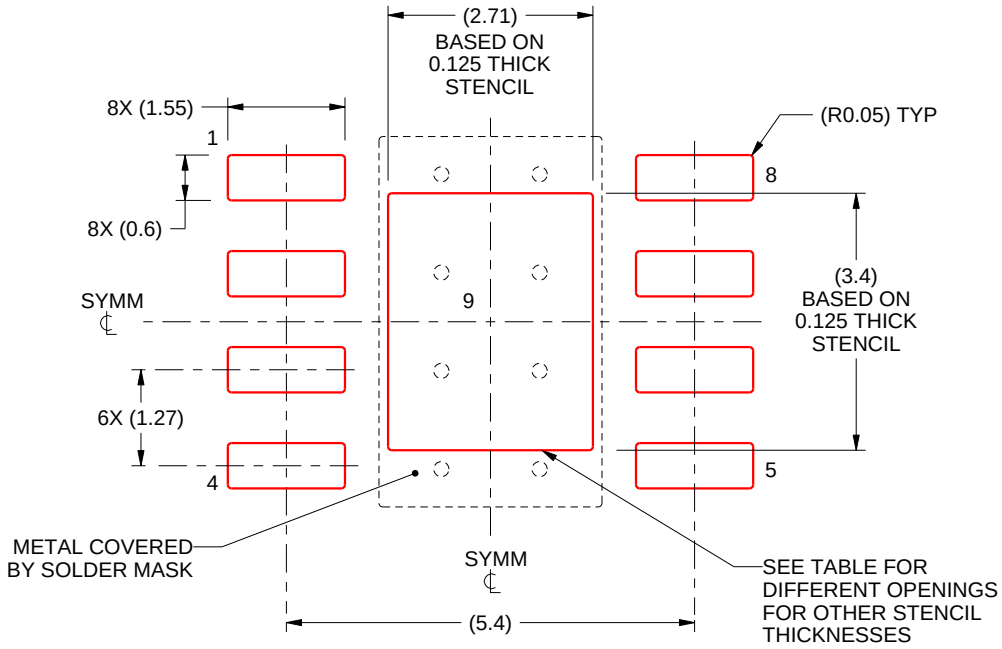
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

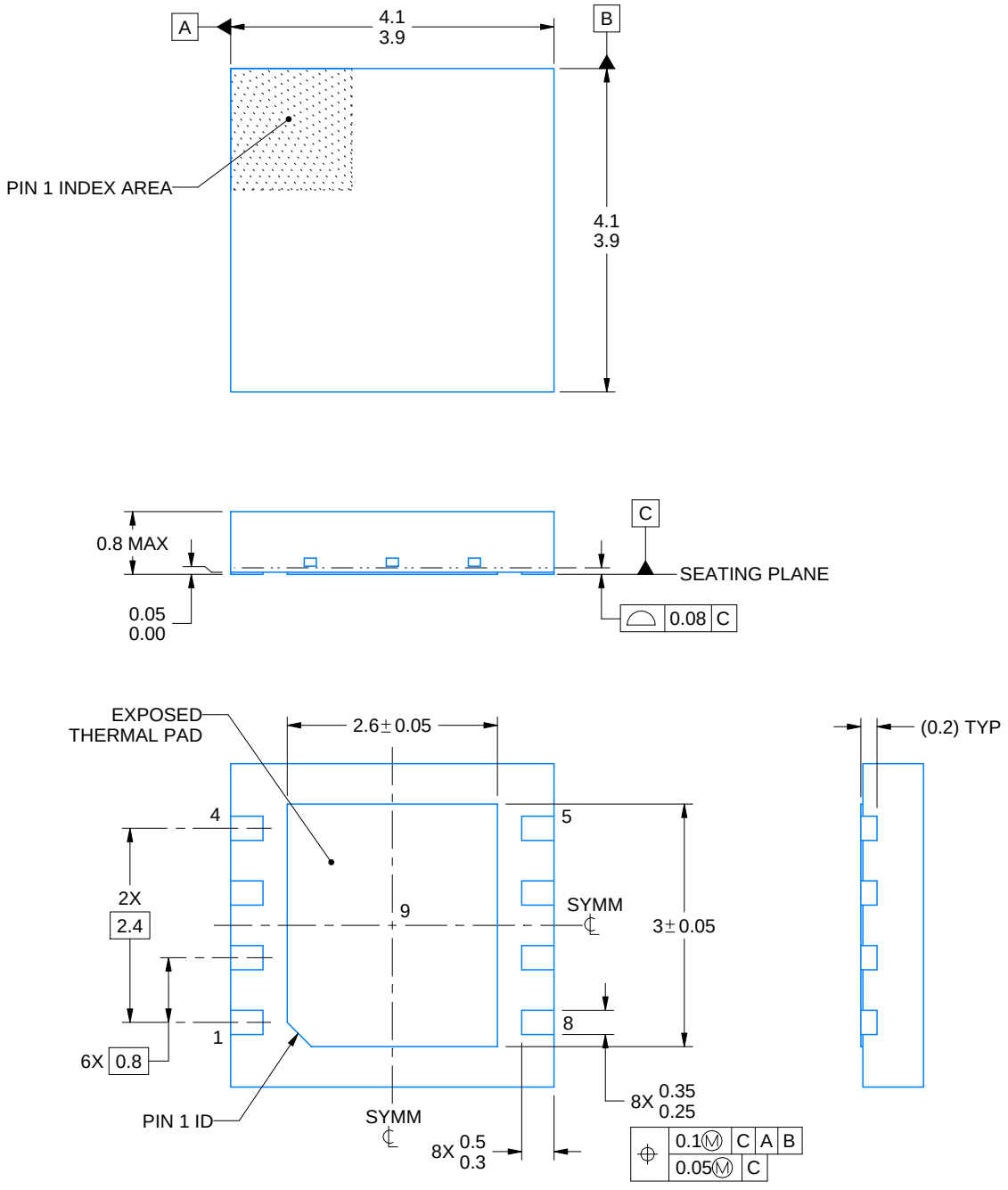
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

NGT0008A

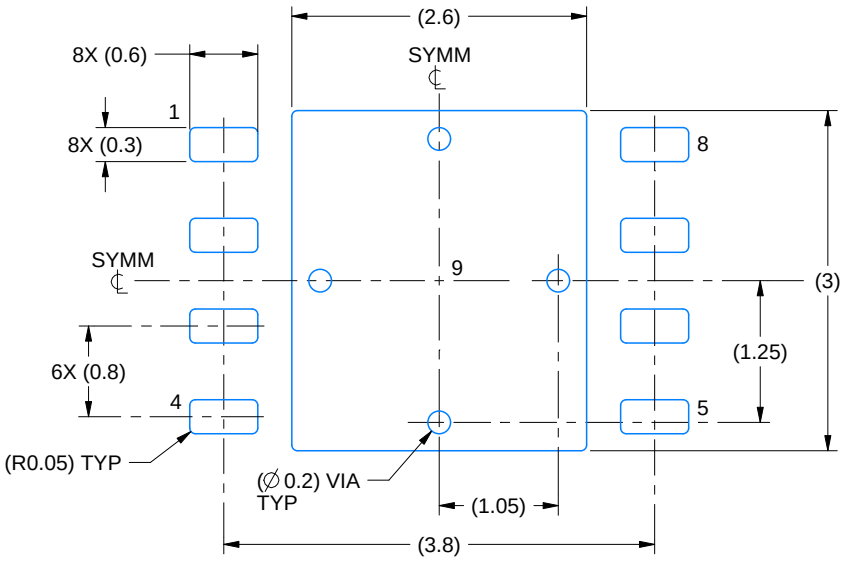
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

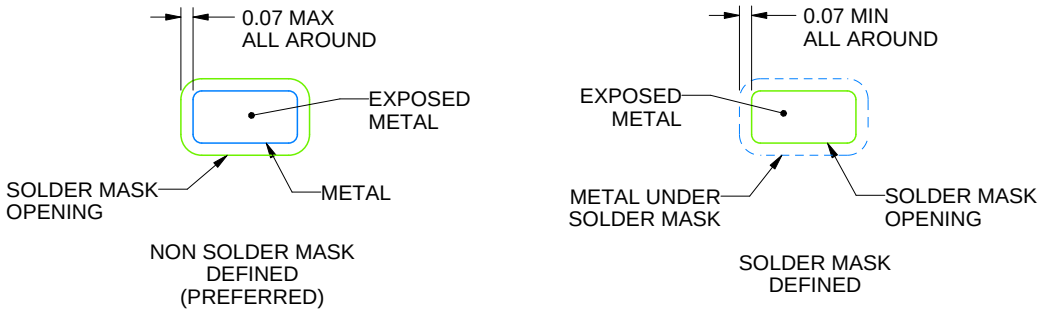


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

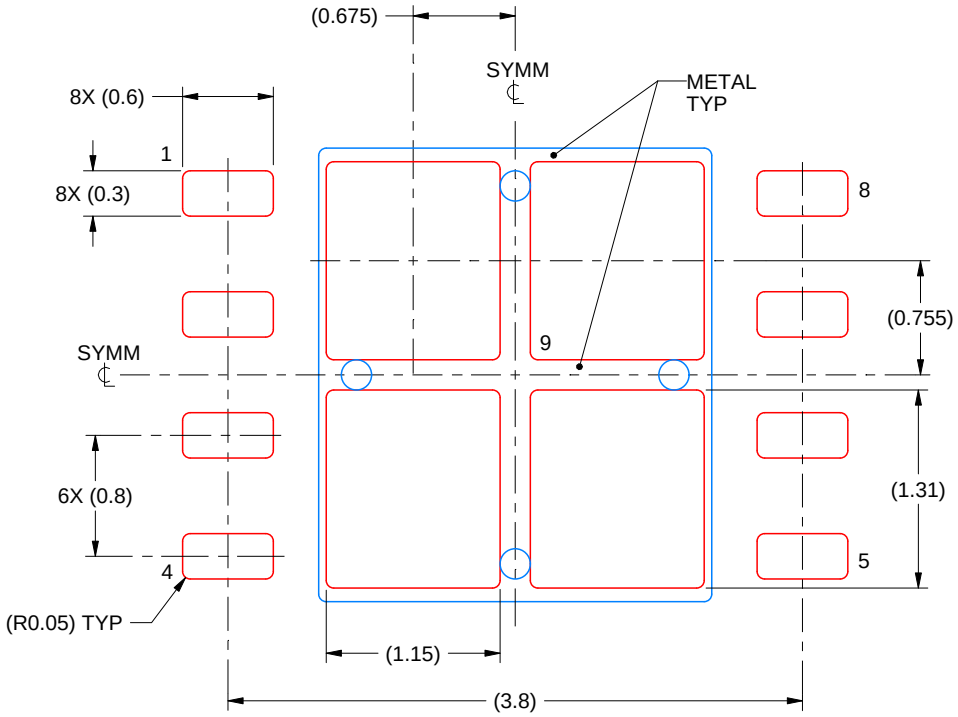


SOLDER MASK DETAILS

4214935/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214935/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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