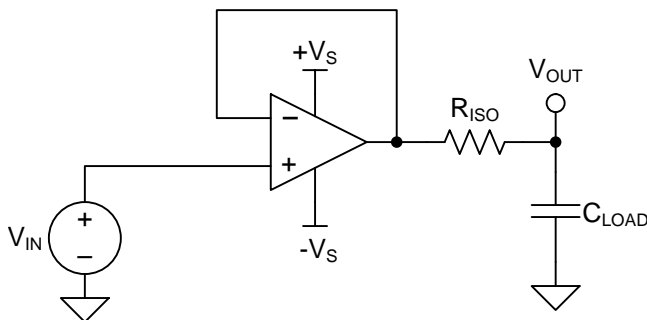


## OPA2171-EP 36V 单电源 SOT553 通用运算放大器

### 1 特性

- 电源电压范围：2.7V 至 36V， $\pm 1.35V$  至  $\pm 18V$
- 低噪声： $14nV/\sqrt{Hz}$
- 低偏移漂移： $0.3\mu V/^\circ C$ （典型值）
- 已过滤的射频干扰 (RFI) 输入
- 输入范围包括负电源
- 输入范围运行至正电源
- 轨至轨输出
- 增益带宽：3MHz
- 低静态电流：每个放大器 475 $\mu A$
- 高共模抑制：120dB（典型值）
- 低输入偏置电流：8pA
- 微型封装：VSSOP-8 双列封装
- 支持国防、航天和医疗应用：
  - 可控基线
  - 一个组装/测试场所
  - 一个制造场所
  - 在扩展 ( $-55^\circ C$  至  $125^\circ C$ ) 温度范围内可用
  - 延长的产品生命周期
  - 延长产品的变更通知周期
  - 产品可追溯性

具有  $R_{ISO}$  稳定性补偿的单位增益缓冲器



### 2 应用范围

- 电源模块内的跟踪放大器
- 商用电源
- 变频器放大器
- 桥式放大器
- 温度测量
- 应力计放大器
- 精密积分器
- 电池供电仪器
- 测试设备

### 3 说明

OPA2171-EP 是一款 36V 单电源低噪声运算放大器，能够在 2.7V ( $\pm 1.35V$ ) 至 36V ( $\pm 18V$ ) 的电源电压范围内运行。这个器件采用微型封装并且在保证低静态电流的情况下提供低偏移、漂移和带宽。单通道、双通道和四通道版本均具有相同的技术规格，可最大程度地提高设计灵活性。

大多数运算放大器仅有一个指定的电源电压，OPAx2171-EP 则有所不同，其可在 2.7V 至 36V 的电压范围内额定运行。超过电源轨的输入信号不会导致相位反向。OPA2171-EP 在电容负载高达 300pF 时可保持稳定。输入可在负电源轨以下 100mV 以及正电源轨之上 100mV 的满轨到轨输入上运行，但是在正电源轨 2V 之内运行时性能会受到影响。

OPA2171-EP 运算放大器额定工作温度范围为  $-55^\circ C$  至  $125^\circ C$ 。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
OPA2171-EP	超薄小外形尺寸封装 (VSSOP)(8)	2.30mm x 2.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



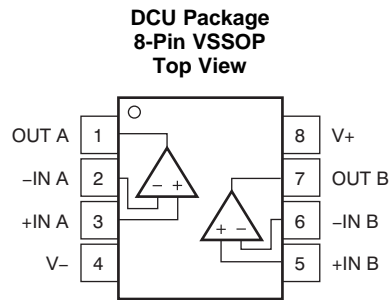
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## 4 修订历史记录

日期	修订版本	注释
2015 年 9 月	*	最初发布版本。

## 5 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
-IN A	2	I	Inverting input, channel A
-IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage		±20		V
Signal input pins	Voltage	(V-) - 0.5	(V+) + 0.5	V
	Current	-10	10	mA
Output short circuit <sup>(2)</sup>		Continuous		
Junction temperature		150		°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ - V-)	4.5 (±2.25)		36 (±18)	V
Operating temperature, T <sub>j</sub>	-55		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		OPA2171-EP	UNIT
		DCU (VSSOP)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	175.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	74.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	22.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case(bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

at  $T_J = 25^\circ\text{C}$ ,  $V_S = 2.7$  to  $36\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>					
Input offset voltage	$V_{OS}$		0.25	$\pm 1.8$	mV
Over temperature	$T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$		0.3	$\pm 2$	mV
Drift	$dV_{OS}/dT$	$T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$	0.3		$\mu\text{V}/^\circ\text{C}$
vs power supply	PSRR	$V_S = 4$ to $36\text{ V}$ , $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	1	$\pm 5$	$\mu\text{V}/\text{V}$
Channel separation, dc	dc		5		$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>					
Input bias current	$I_B$		$\pm 8$	$\pm 15$	pA
Over temperature	$T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$			$\pm 4$	nA
Input offset current	$I_{OS}$		$\pm 4$		pA
Over temperature	$T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$			$\pm 4$	nA
<b>NOISE</b>					
Input voltage noise	$f = 0.1$ to $10\text{ Hz}$		3		$\mu\text{V}_{PP}$
Input voltage noise density	$e_n$	$f = 100\text{ Hz}$	25		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	14		$\text{nV}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE</b>					
Common-mode voltage range <sup>(1)</sup>	$V_{CM}$	$(V-) - 0.1\text{ V}$		$(V+) - 2\text{ V}$	V
Common-mode rejection ratio	CMRR	$V_S = \pm 2\text{ V}$ , $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ , $T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$	87	104	dB
		$V_S = \pm 18\text{ V}$ , $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$ , $T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$	104	120	dB
<b>INPUT IMPEDANCE</b>					
Differential			$100 \parallel 3$		$\text{M}\Omega \parallel \text{pF}$
Common-mode			$6 \parallel 3$		$10^{12}\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>					
Open-loop voltage gain	$A_{OL}$	$V_S = 4$ to $36\text{ V}$ , $(V-) + 0.35\text{ V} < V_O < (V+) - 0.35\text{ V}$ , $T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$	110	130	dB
<b>FREQUENCY RESPONSE</b>					
Gain bandwidth product	GBP		3.0		MHz
Slew rate	SR	$G = +1$	1.5		$\text{V}/\mu\text{s}$
Settling time	$t_s$	To 0.1%, $V_S = \pm 18\text{ V}$ , $G = +1$ , 10-V step	6		$\mu\text{s}$
		To 0.01% (12 bit), $V_S = \pm 18\text{ V}$ , $G = +1$ , 10-V step	10		$\mu\text{s}$
Overload recovery time		$V_{IN} \times \text{Gain} > V_S$	2		$\mu\text{s}$
Total harmonic distortion + noise	THD+N	$G = +1$ , $f = 1\text{ kHz}$ , $V_O = 3V_{RMS}$	0.0002%		
<b>OUTPUT</b>					
Voltage output swing from rail	$V_O$	$V_S = 5\text{ V}$ , $R_L = 10\text{ k}\Omega$	30		mV
Over temperature		$R_L = 10\text{ k}\Omega$ , $A_{OL} \geq 110\text{ dB}$ , $T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$	$(V-) + 0.35$	$(V+) - 0.35$	V
Short-circuit current	$I_{SC}$		+25/-35		mA
Capacitive load drive	$C_{LOAD}$		See <a href="#">Typical Characteristics</a>		pF
Open-loop output resistance	$R_O$	$f = 1\text{ MHz}$ , $I_O = 0\text{ A}$	150		$\Omega$

(1) The input range can be extended beyond  $(V+) - 2\text{ V}$  up to  $V+$ . See [Typical Characteristics](#) and [Application and Implementation](#) for additional information.

**Electrical Characteristics (continued)**

 at  $T_J = 25^\circ\text{C}$ ,  $V_S = 2.7$  to  $36\text{ V}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>						
Specified voltage range	$V_S$		2.7		36	V
Quiescent current per amplifier	$I_Q$	$I_O = 0\text{ A}$		475	595	$\mu\text{A}$
Over temperature		$I_O = 0\text{ A}$ , $T_J = -55^\circ\text{C}$ to $125^\circ\text{C}$			650	$\mu\text{A}$
<b>TEMPERATURE</b>						
Operating temperature	$T_J$		-55		125	$^\circ\text{C}$

## 6.6 Typical Characteristics

**Table 1. Characteristic Performance Measurements**

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5
Offset Voltage vs Power Supply	Figure 6
$I_B$ and $I_{OS}$ vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 10
CMRR vs Temperature	Figure 11
PSRR vs Temperature	Figure 12
0.1-Hz to 10-Hz Noise	Figure 13
Input Voltage Noise Spectral Density vs Frequency	Figure 14
THD+N Ratio vs Frequency	Figure 15
THD+N vs Output Amplitude	Figure 16
Quiescent Current vs Temperature	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Open-Loop Gain and Phase vs Frequency	Figure 19
Closed-Loop Gain vs Frequency	Figure 20
Open-Loop Gain vs Temperature	Figure 21
Open-Loop Output Impedance vs Frequency	Figure 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 23, Figure 24
No Phase Reversal	Figure 25
Positive Overload Recovery	Figure 26
Negative Overload Recovery	Figure 27
Small-Signal Step Response (100 mV)	Figure 28, Figure 29
Large-Signal Step Response	Figure 30, Figure 31
Large-Signal Settling Time (10-V Positive Step)	Figure 32
Large-Signal Settling Time (10-V Negative Step)	Figure 33
Short-Circuit Current vs Temperature	Figure 34
Maximum Output Voltage vs Frequency	Figure 35
Channel Separation vs Frequency	Figure 36

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

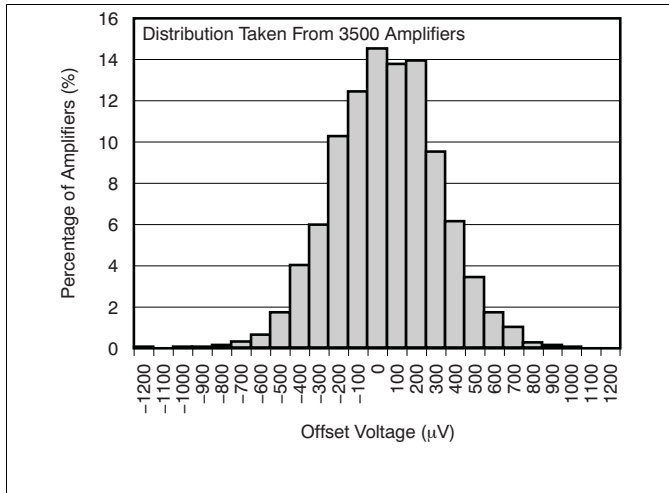


Figure 1. Offset Voltage Production Distribution

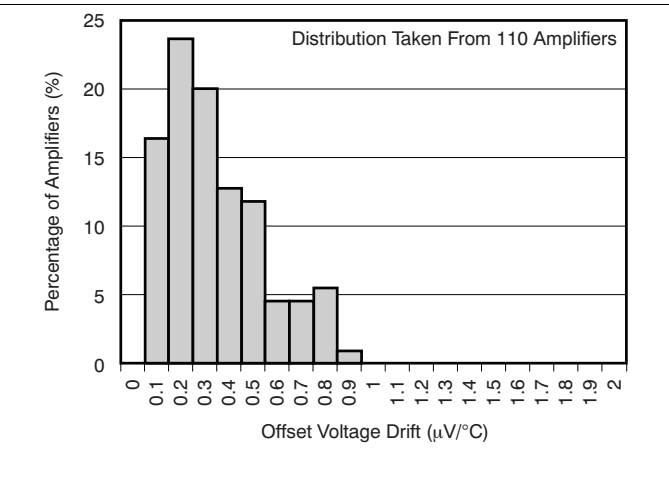


Figure 2. Offset Voltage Drift Distribution

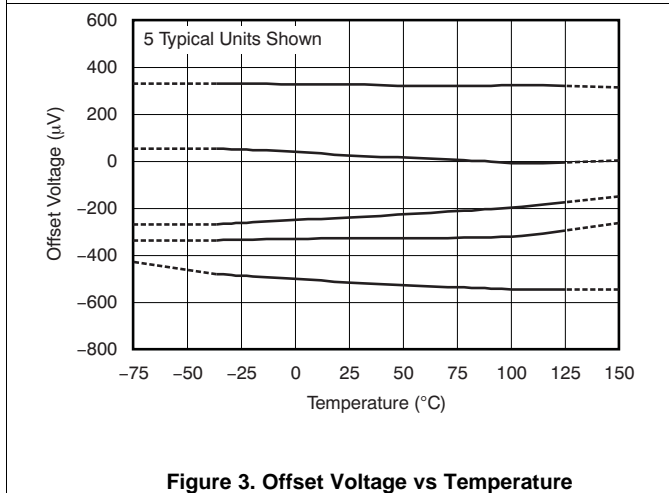


Figure 3. Offset Voltage vs Temperature

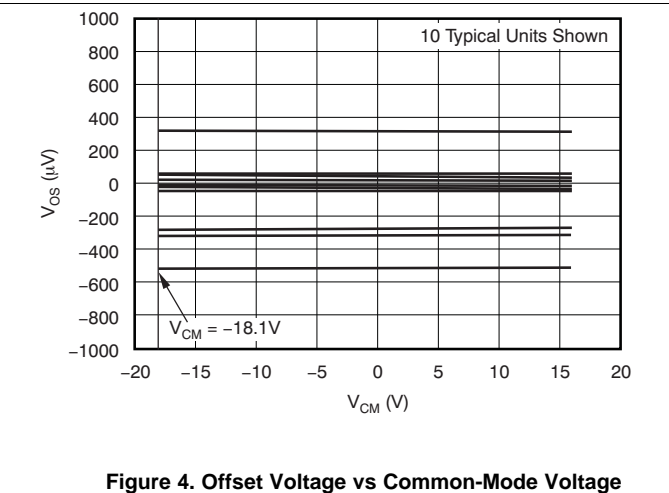


Figure 4. Offset Voltage vs Common-Mode Voltage

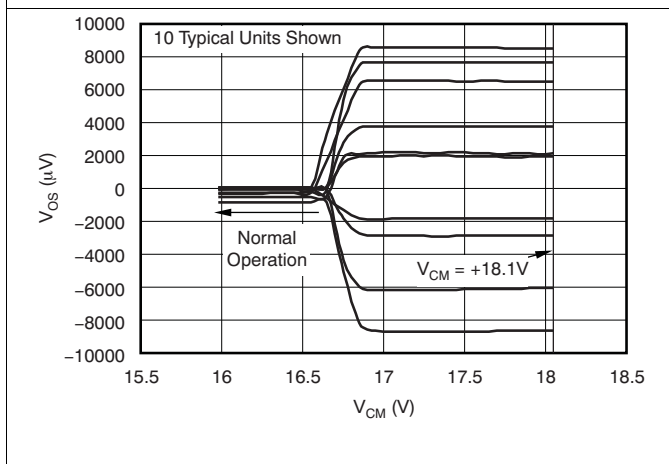


Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

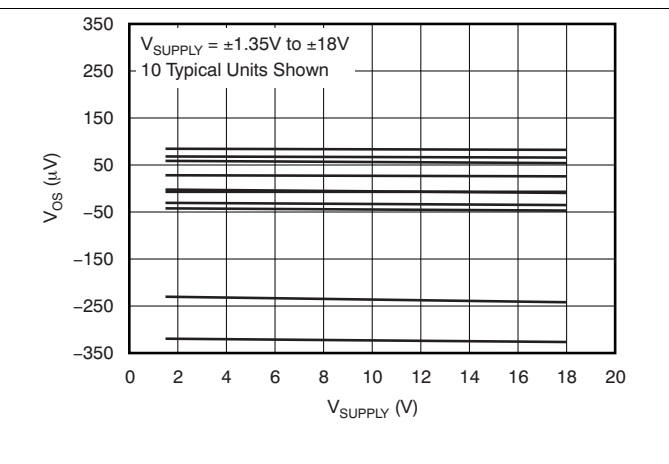


Figure 6. Offset Voltage vs Power Supply



$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

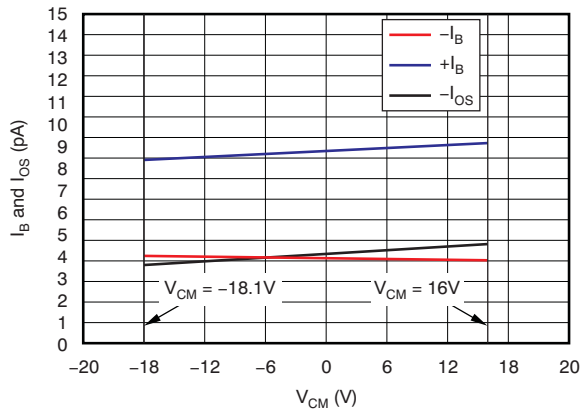


Figure 7.  $I_B$  and  $I_{OS}$  vs Common-Mode Voltage

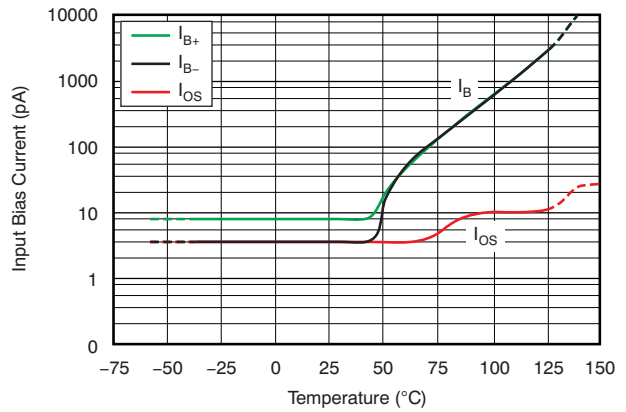


Figure 8. Input Bias Current vs Temperature

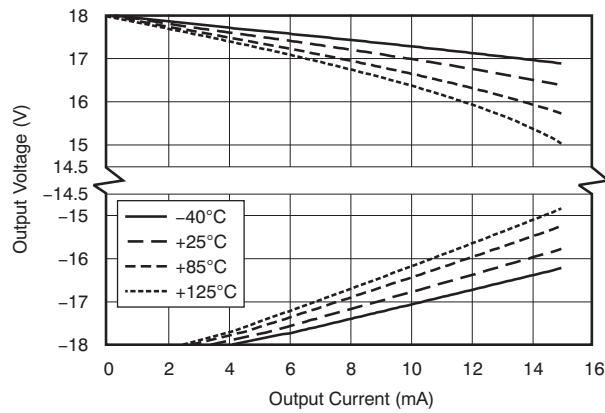


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

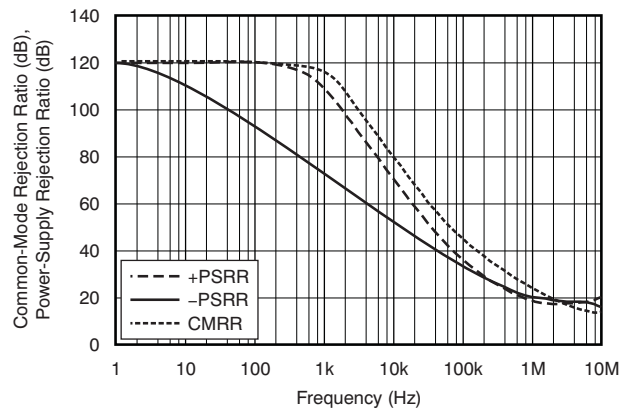


Figure 10. CMRR and PSRR vs Frequency (Referred-to Input)

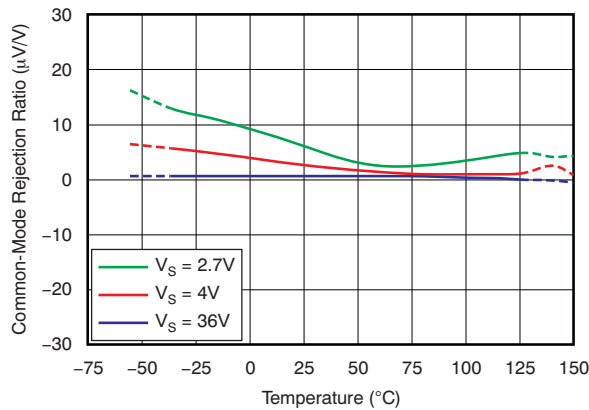


Figure 11. CMRR vs Temperature

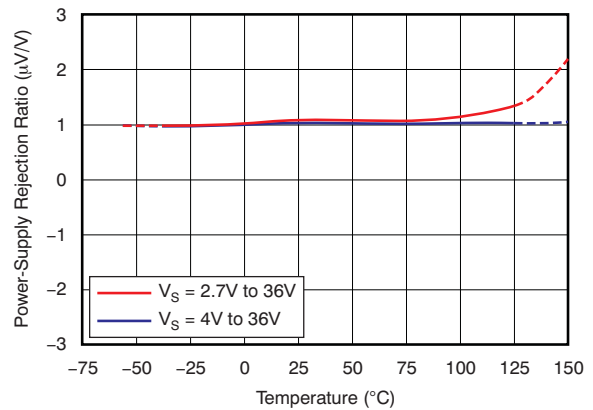


Figure 12. PSRR vs Temperature

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

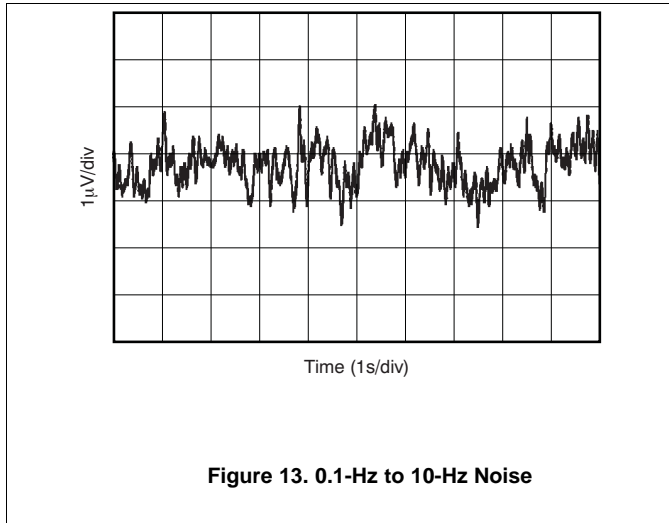


Figure 13. 0.1-Hz to 10-Hz Noise

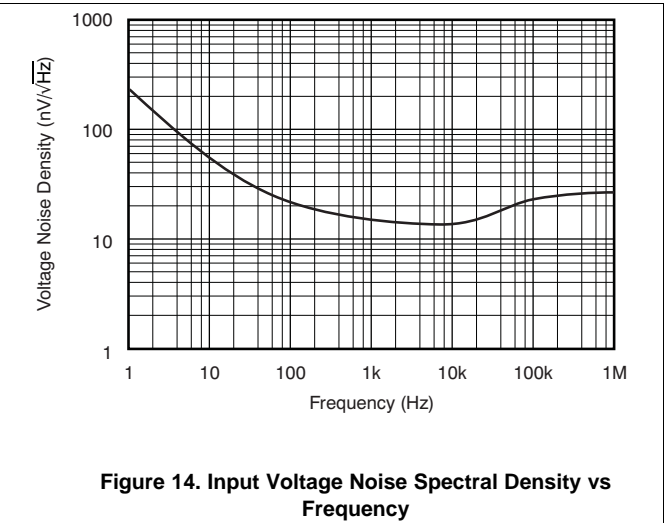


Figure 14. Input Voltage Noise Spectral Density vs Frequency

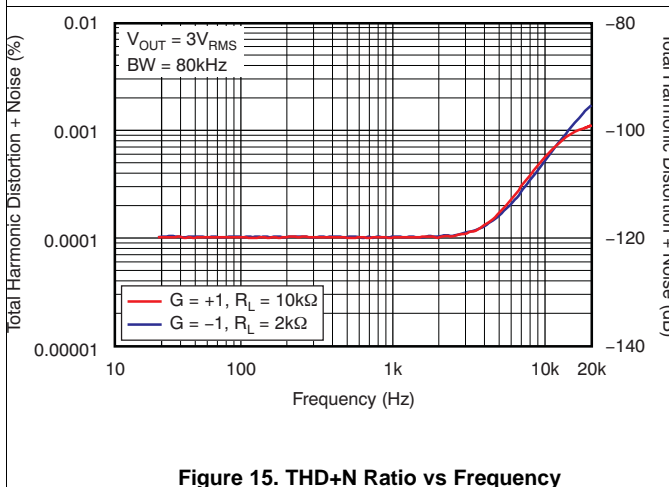


Figure 15. THD+N Ratio vs Frequency

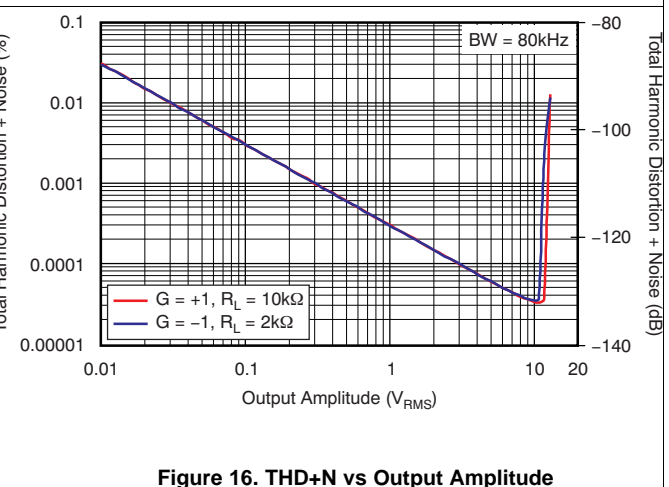


Figure 16. THD+N vs Output Amplitude

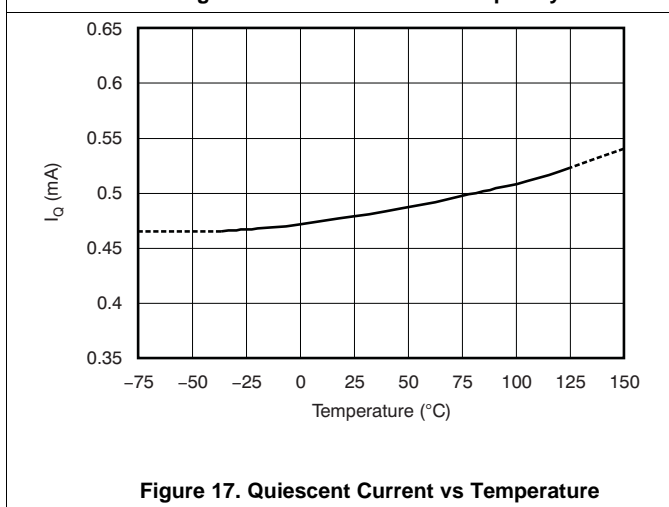


Figure 17. Quiescent Current vs Temperature

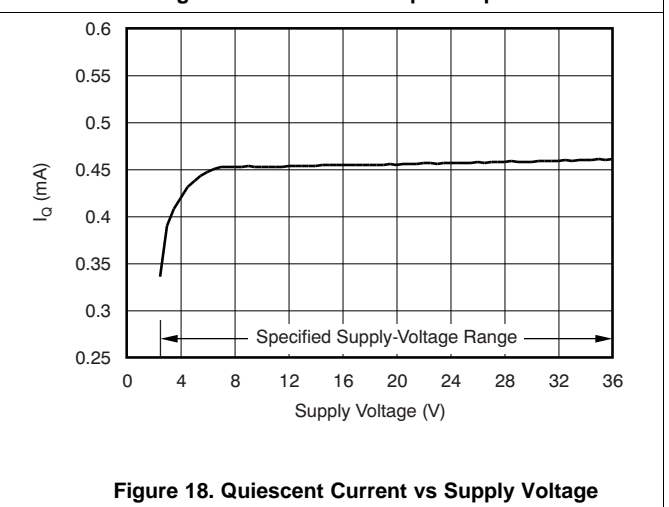


Figure 18. Quiescent Current vs Supply Voltage

$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

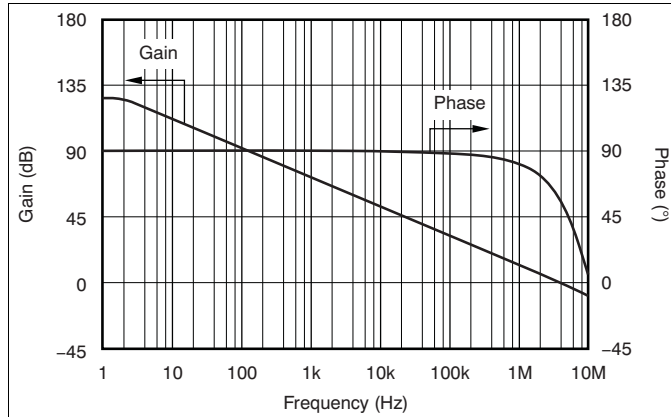


Figure 19. Open-Loop Gain and Phase vs Frequency

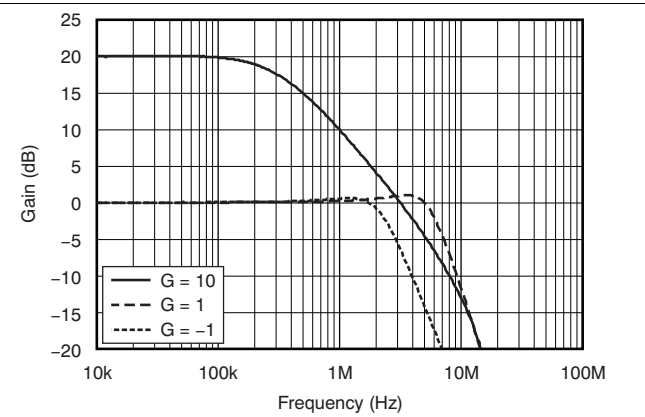


Figure 20. Closed-Loop Gain vs Frequency

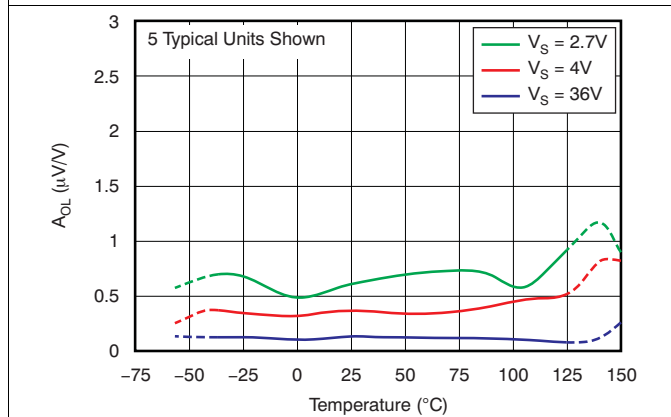


Figure 21. Open-Loop Gain vs Temperature

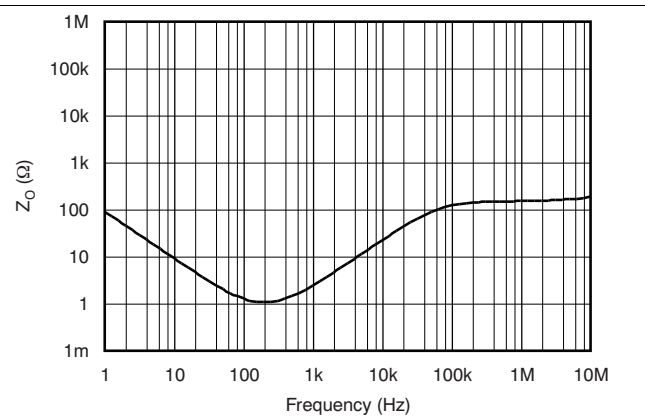


Figure 22. Open-Loop Output Impedance vs Frequency

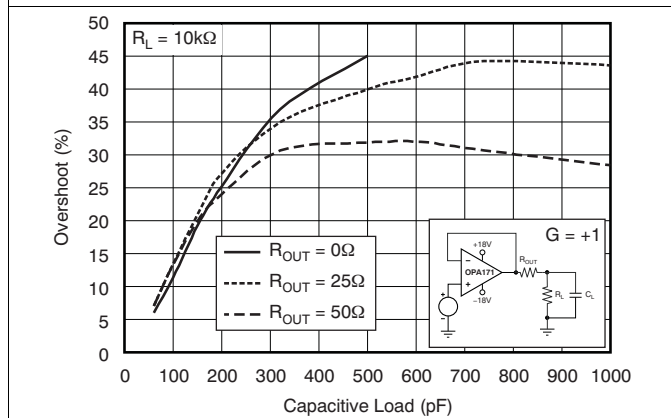


Figure 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

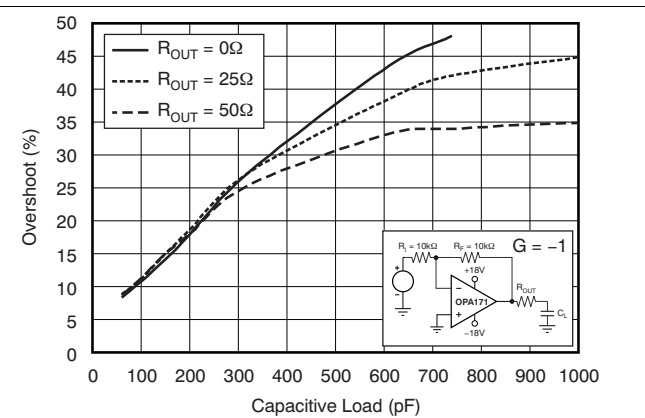


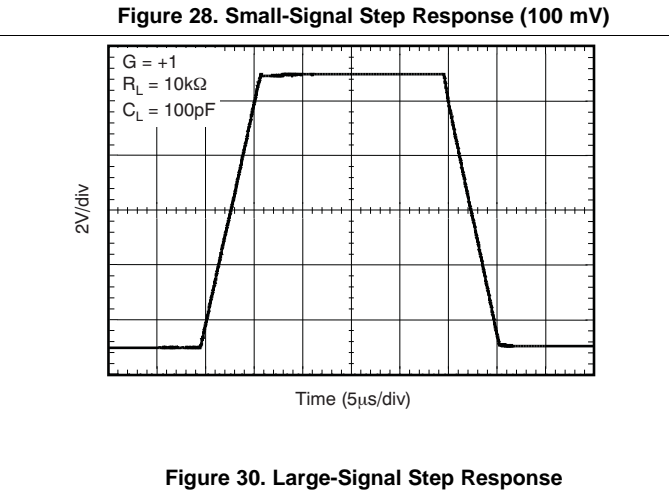
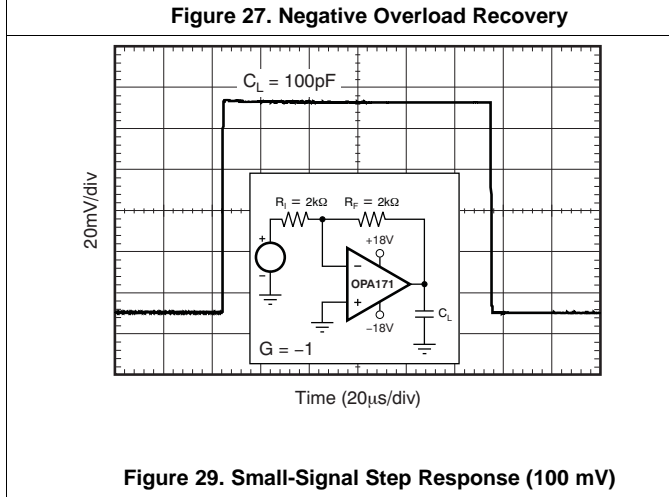
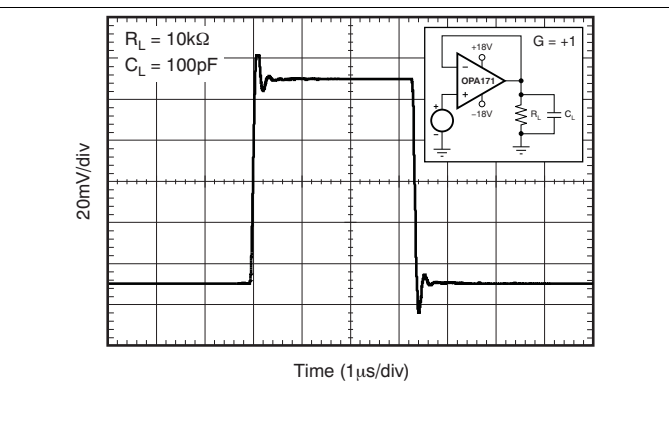
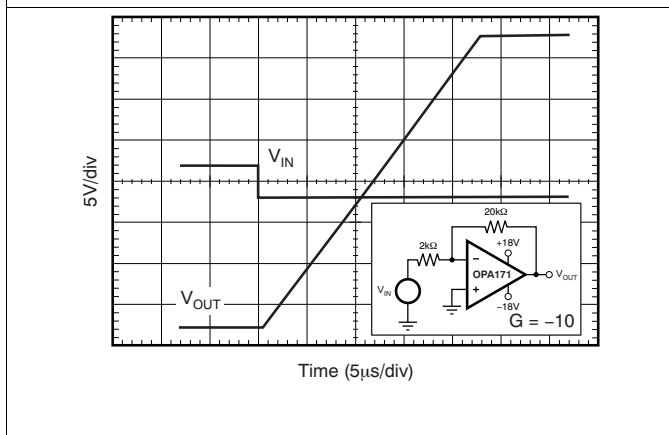
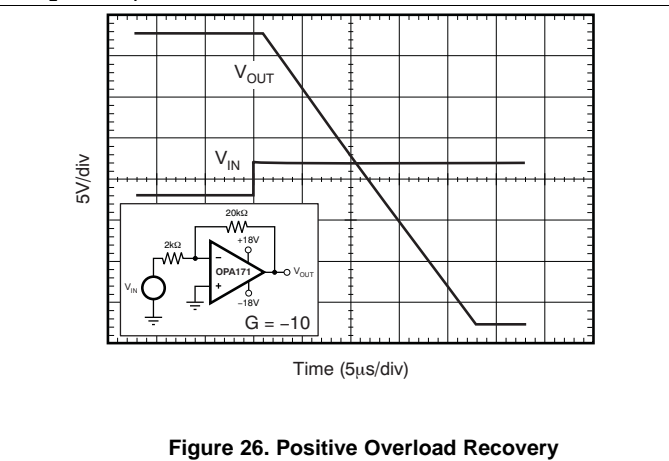
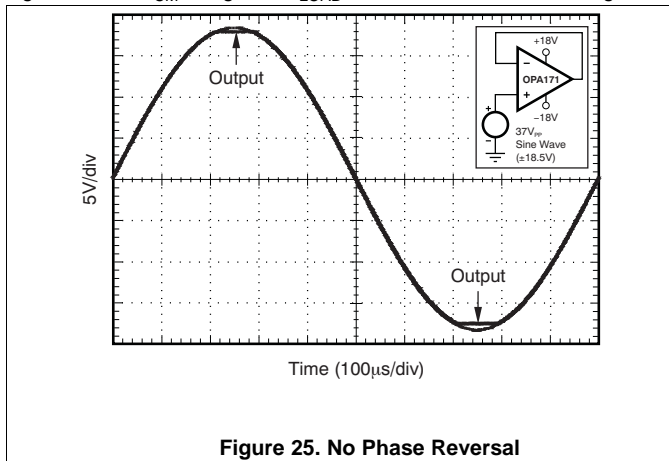
Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

# OPA2171-EP

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$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.



$V_S = \pm 18\text{ V}$ ,  $V_{CM} = V_S / 2$ ,  $R_{LOAD} = 10\text{ k}\Omega$  connected to  $V_S / 2$ , and  $C_L = 100\text{ pF}$ , unless otherwise noted.

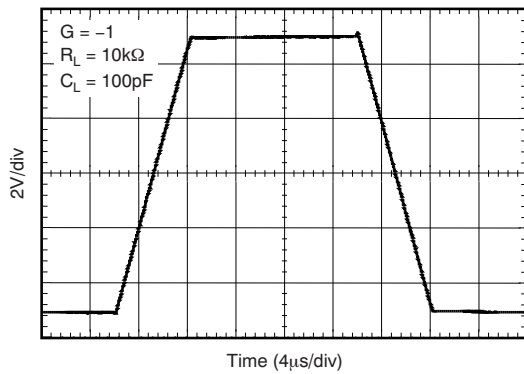


Figure 31. Large-Signal Step Response

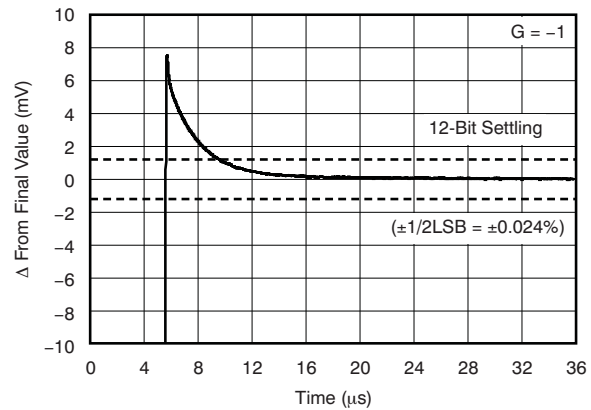


Figure 32. Large-Signal Settling Time (10-V Positive Step)

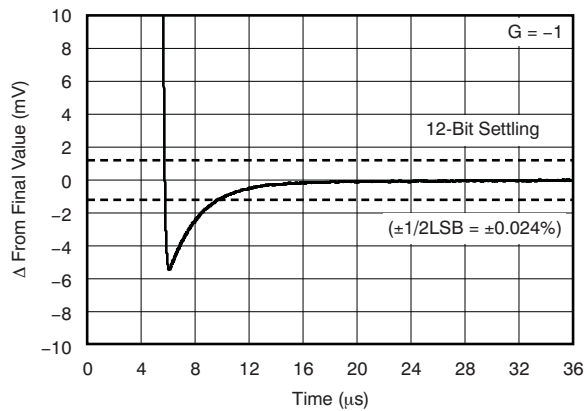


Figure 33. Large-Signal Settling Time (10-V Negative Step)

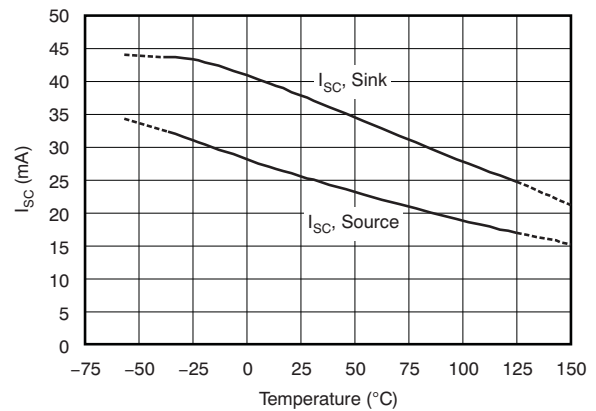


Figure 34. Short-Circuit Current vs Temperature

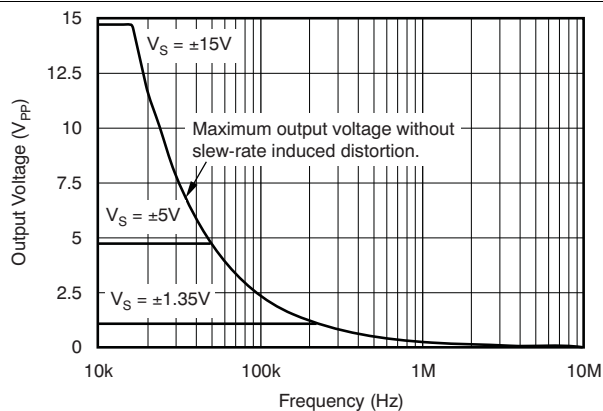


Figure 35. Maximum Output Voltage vs Frequency

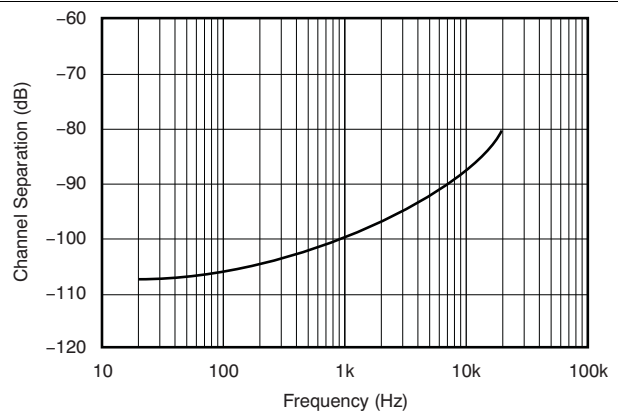


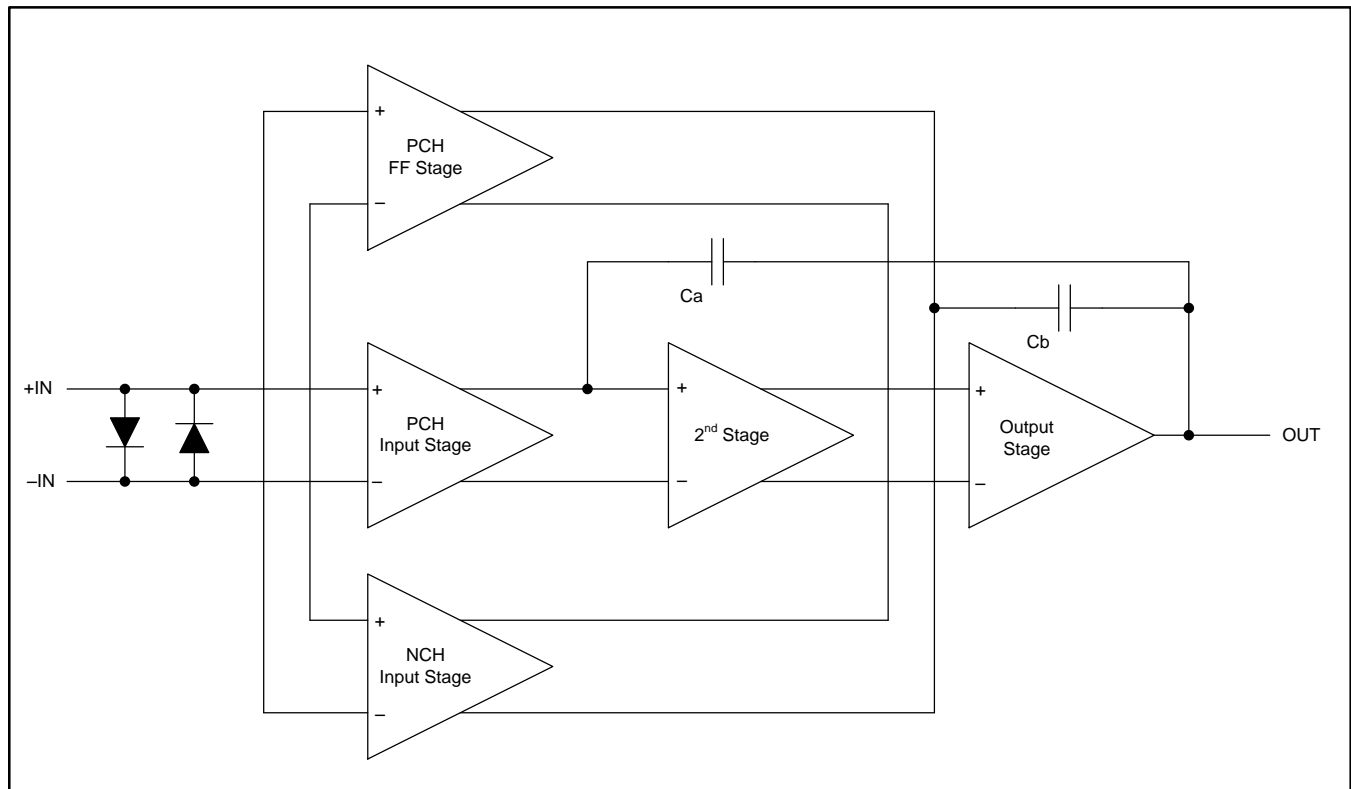
Figure 36. Channel Separation vs Frequency

## 7 Detailed Description

### 7.1 Overview

The OPA2171-EP operational amplifier provides high overall performance, making it ideal for many general-purpose applications. The excellent offset drift of only  $2 \mu\text{V}/^\circ\text{C}$  provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and  $A_{OL}$ . As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases,  $0.1\text{-}\mu\text{F}$  capacitors are adequate.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Operating Characteristics

The OPA2171-EP amplifier is specified for operation from 2.7 to 36 V ( $\pm 1.35$  to  $\pm 18$  V). Many of the specifications apply from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in [Typical Characteristics](#).

#### 7.3.2 Phase-Reversal Protection

The OPA2171-EP has an internal phase-reversal protection. Many operational amplifiers exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA2171-EP prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. [Figure 37](#) shows this performance.

Feature Description (continued)

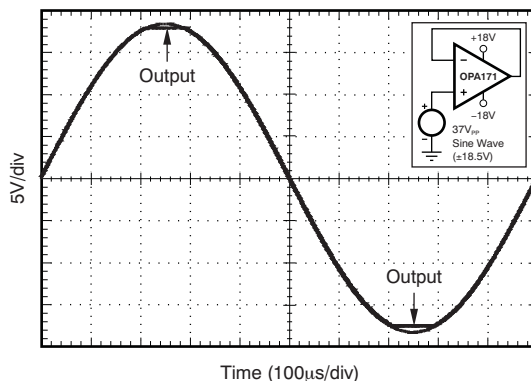


Figure 37. No Phase Reversal

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPA2171-EP extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. Table 2 summarizes the typical performance in this range.

Table 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
vs Temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1kHz		30		nV/√Hz

## 8 Application and Implementation

### NOTE

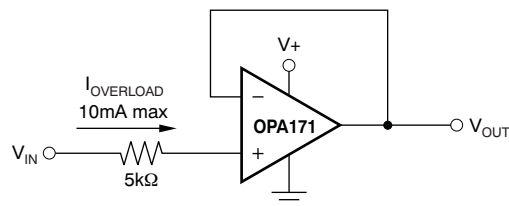
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Electrical Overstress

Designers often ask about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in *Absolute Maximum Ratings*. Figure 38 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.



**Figure 38. Input Current Protection**

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is uncertainty about the ability of the supply to absorb this current, external Zener diodes may be added to the supply pins. Select the Zener voltage such that the diode does not turn on during normal operation.

However, its Zener voltage should be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



## 8.2 Typical Application

Figure 39 shows a capacitive load drive solution using an isolation resistor. The OPA2171-EP device can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor ( $R_{ISO}$ ) to stabilize the output of an op amp.  $R_{ISO}$  modifies the open loop gain of the system to ensure the circuit has sufficient phase margin.

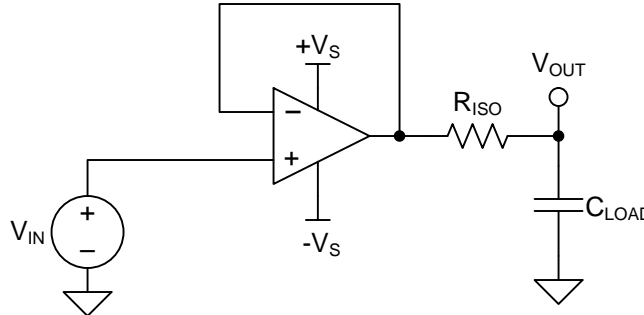


Figure 39. Unity-Gain Buffer with  $R_{ISO}$  Stability Compensation

### 8.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V ( $\pm 15$  V)
- Capacitive loads: 100 pF, 1000 pF, 0.01  $\mu$ F, 0.1  $\mu$ F, and 1  $\mu$ F
- Phase margin: 45° and 60°

### 8.2.2 Detailed Design Procedure

Figure 39 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 39. Not shown in Figure 39 is the open-loop output resistance of the op amp,  $R_o$ .

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole ( $f_p$ ) is determined by  $(R_o + R_{ISO})$  and  $C_{LOAD}$ . Components  $R_{ISO}$  and  $C_{LOAD}$  determine the frequency of the zero ( $f_z$ ). A stable system is obtained by selecting  $R_{ISO}$  such that the rate of closure (ROC) between the open-loop gain ( $A_{OL}$ ) and  $1/\beta$  is 20 dB/decade. Figure 40 depicts the concept. The  $1/\beta$  curve for a unity-gain buffer is 0 dB.

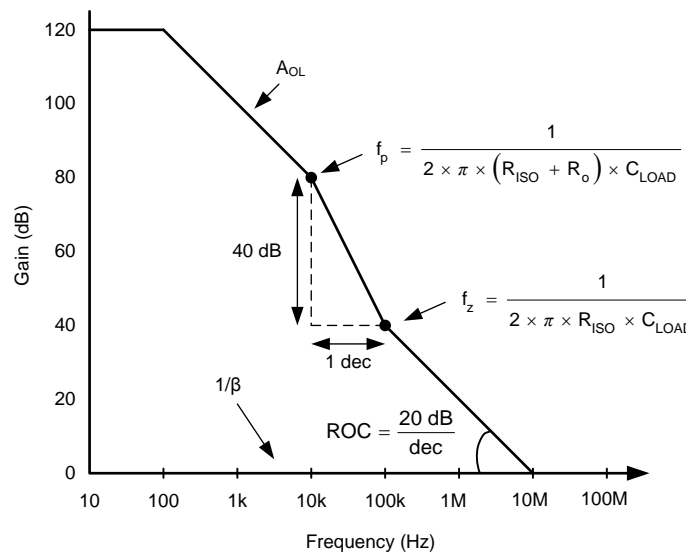


Figure 40. Unity-Gain Amplifier with  $R_{ISO}$  Compensation

**Typical Application (continued)**

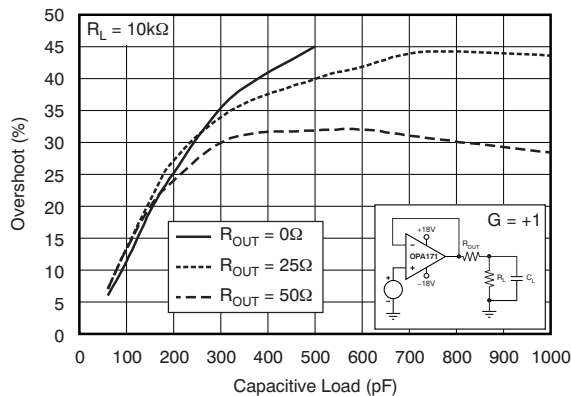
ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of  $R_o$ . In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA171, refer to the Precision Design, *Capacitive Load Drive Solution using an Isolation Resistor (TIPD128)*.

**Table 3. Phase Margin versus Overshoot and AC Gain Peaking**

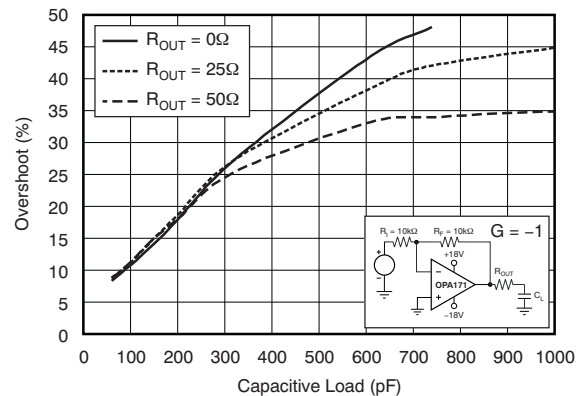
PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

**8.2.2.1 Capacitive Load and Stability**

The dynamic characteristics of the OPA2171-EP have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example,  $R_{OUT}$  equal to 50  $\Omega$ ) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of  $R_{OUT}$ . Also, refer to *Applications Bulletin AB-028 (SBOA015)*, available for download from [www.ti.com](http://www.ti.com) for details of analysis techniques and application circuits.



**Figure 41. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**



**Figure 42. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

### 8.2.3 Application Curve

The OPA2171-EP device meets the supply voltage requirements of 30 V. The OPA2171-EP device was tested for various capacitive loads and  $R_{ISO}$  was adjusted to achieve an overshoot corresponding to [Table 3](#). [Figure 43](#) shows the test results.

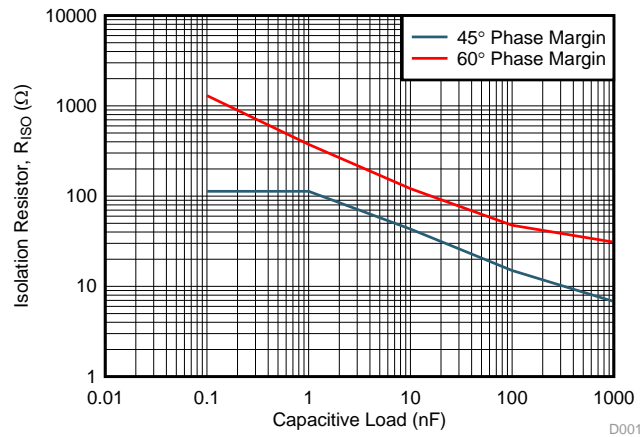


Figure 43.  $R_{ISO}$  vs  $C_{LOAD}$

## 9 Power Supply Recommendations

The OPA2171-EP is specified for operation from 4.5 V to 36 V ( $\pm 2.25$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

### CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

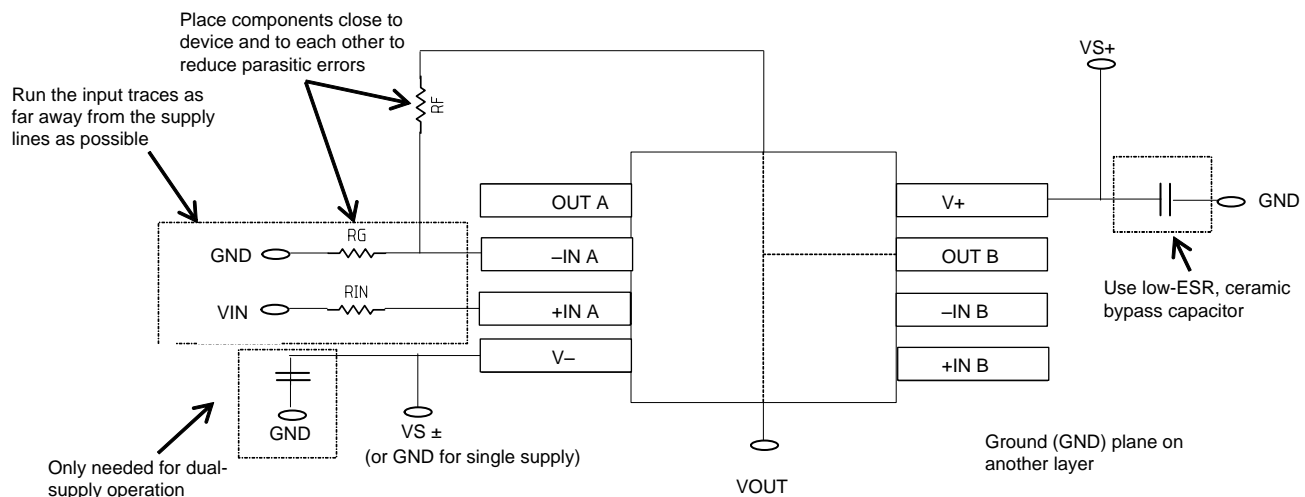
Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the [Layout](#) section.

## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, TI recommends good printed circuit board (PCB) layout practices. Low-loss, 0.1- $\mu$ F bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

### 10.2 Layout Example



**Figure 44. Operational Amplifier Board Layout for Noninverting Configuration**

## 11 器件和文档支持

### 11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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### 11.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不  
对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏

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DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2171MDCUTEP	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ZGAA	<a href="#">Samples</a>
V62/15605-01XE	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ZGAA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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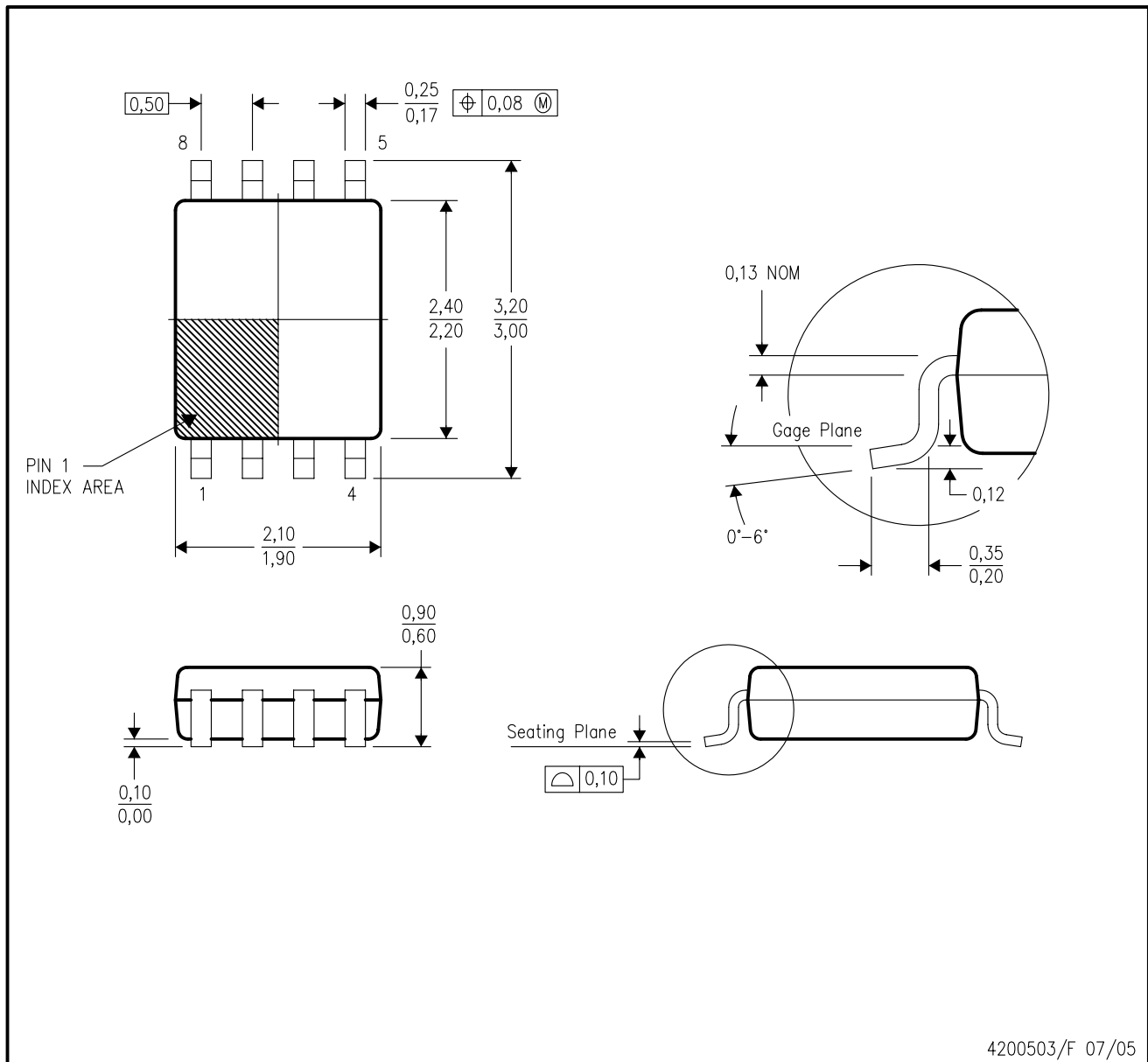
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DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

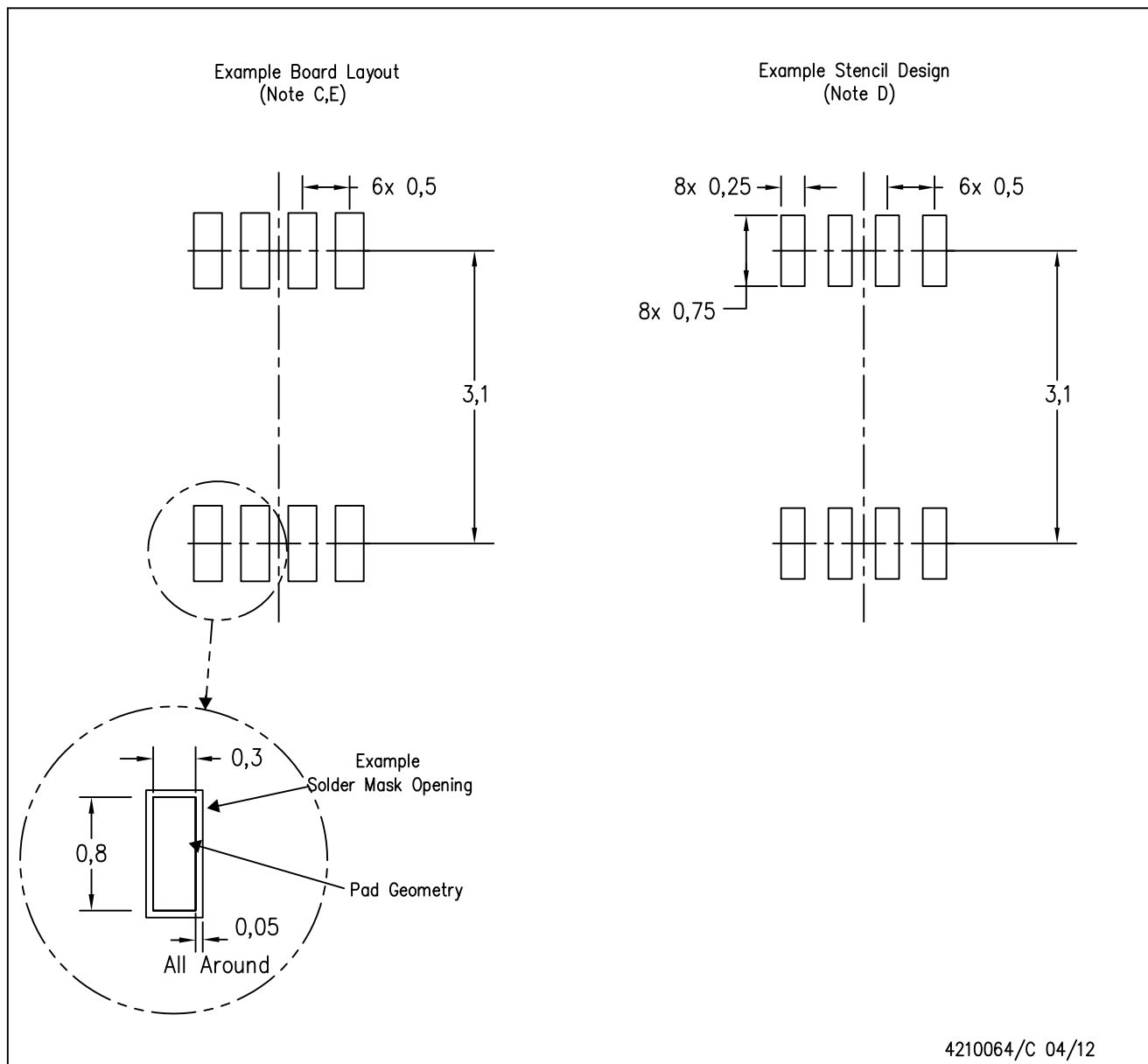


4200503/F 07/05

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



4210064/C 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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