单位增益稳定，低噪音，电压反馈运算放大器

查询样品：**OPA820-HT**

特性

- 高带宽
  （在**25°C**时为**240 MHz**和在**210°C**时为**100 MHz**，**G = 2**）
- 高输出电流
  （**25°C**时为**±110 mA**而在**210°C**时为**50 mA**）
- 低输入噪音
  （在**25°C**时为**2.5 nV/√Hz** 而在**210°C**时为**4.5 nV/√Hz**）
- 低电源电流
  （在**25°C**时为**5.6mA**而在**210°C**时为**6.8mA**）
- 灵活的电源电压：
  - 双电源时为**±2.5 V**至**±5 V**
  - 单电源时为**+5 V**

应用范围

- 潜孔钻井
- 极端温度环境下的应用

支持极端温度环境下的应用

- 可控基线
- 一个组装/测试场所
- 一个制造场所
- 可在极端温度范围 **(–55°C/210°C)** 下工作(1)
- 延长的产品生命周期
- 延长产品的变更通知周期
- 产品可追溯性
- 德州仪器高温产品利用高度优化的硅（芯片）解决方案，此解决方案对设计和制造工艺进行了提升以在拓展的温度范围内大大地提高性能。 在最大额定温度下，所有器件可连续正常运行**1000**小时。

(1) 可定制工作温度范围

说明

OPA820提供了一个宽频带，单位增益稳定，电压反馈放大器，此放大器在使用6.8mA低电流电源供电时具有非常低的输入噪音电压和高输出电流。 OPA820可在低功率器件上进行具有出色DC精度的高速运算。 在最差情况下，输入偏置电压为±3.5mV而偏置电流为±700nA，这为脉冲放大器应用提供了出色的绝对DC精度。

最小输入和输出电压摆幅净空使得OPA820运行在一个单一5V电源上，其输出摆幅>2V_{PP}。 虽然不是轨到轨(RR)输出，此摆幅可在保证其功耗和噪音低于典型的RR输出运算放大器的前提下支持大多数新上市的模数转换器(ADC)输入范围。

OPA820额定工作温度范围是–55°C至210°C。

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils.	Silicon with backgrind	Floating	TiW/AlCu (0.5%)	1100 nm

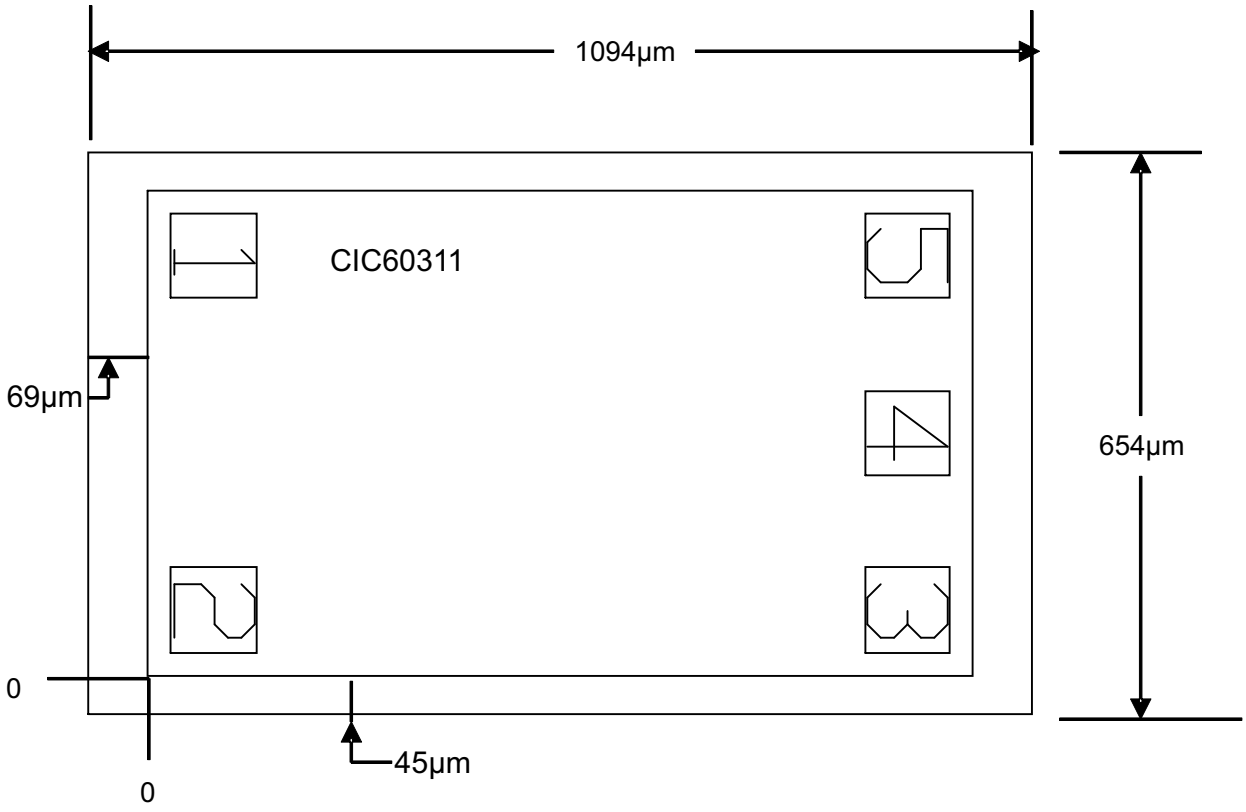

Table 1. Bond Pad Coordinates in Microns

DISCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
Inverting Input	1	27	439	125	537
NonInverting Input	2	27	125	125	125
Output	3	831	27	929	125
$-V_S$	4	831	233	929	331
$+V_S$	5	831	439	929	537

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	KGD (bare die)	OPA820SKD3	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

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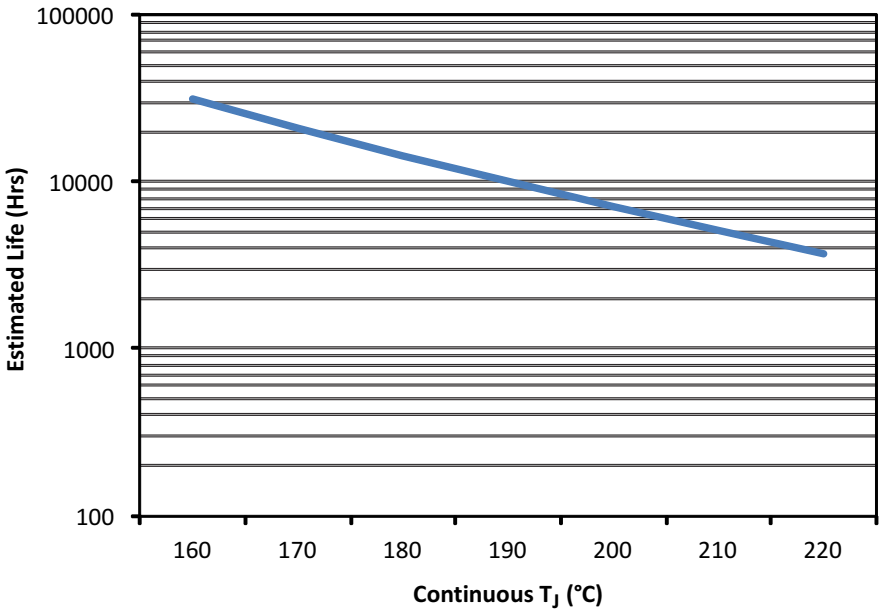
ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		UNIT
Supply voltage, $V_{S–}$ to V_{S+}	±6.5	V
Differential input voltage, V_{ID}	±1.2	V
Input common-mode voltage range	$\pm V_S$	V
Maximum continuous operating current at 210°C	50	mA
Internal power dissipation	See Thermal Characteristic specifications	
Junction temperature, T_J	210	°C
Operating Free-air Temperature Range, T_A	–55 to 210	°C
Storage Temperature Range, T_{STG}	–65 to 210	°C
Lead temperature (soldering, 10 s)	300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



A. See datasheet for absolute maximum and minimum recommended operating conditions.

B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

C. The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wear out for the specific device process and design characteristics.

Figure 1. OPA820-HT Operating Life Derating Chart

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ELECTRICAL CHARACTERISTICS: V_S = ±5 V

R_F = 402 Ω, R_L = 100 Ω, and G = 2, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			210°C			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX	MIN	TYP	MAX		
AC PERFORMANCE									
Small-Signal Bandwidth	G = 1, V_O = 0.1V_{PP}, R_F = 0 Ω		800					MHz	C
	G = 2, V_O = 0.1V_{PP}		240			100		MHz	C
	G = 10, V_O = 0.1V_{PP}		30					MHz	C
Gain Bandwidth Product	G ≥ 20	150	270			202		MHz	C
Bandwidth for 0.1dB Gain Flatness	G = 2, V_O = 0.1V_{PP}		38					MHz	C
Peaking at a Gain of +1	V_O = 0.1V_{PP}, R_F = 0 Ω		0.5					dB	C
Large-Signal Bandwidth	G = 2, V_O = 2V_{PP}		85					MHz	C
Slew Rate	G = 2, 2-V Step		240			185		V/µs	C
Rise and Fall Time	G = 2, V_O = 0.2-V Step		10.5			11.5		ns	C
Settling Time to 0.02%	G = 2, V_O = 2-V Step		22			28		ns	C
Settling Time to 0.1%	G = 2, V_O = 2-V Step		18			25		ns	C
Harmonic Distortion	G = 2, f = 1 MHz, V_O = 2V_{PP}								
2nd harmonic	R_L = 200 Ω		-85	-79		-77		dBc	C
	R_L = 500 Ω		-90	-81		-90		dBc	C
3rd harmonic	R_L = 200 Ω		-95	-88		-78		dBc	C
	R_L = 500 Ω		-110	-100		-98		dBc	C
Input Voltage Noise	f > 100 kHz		2.5	2.9		4.5		nV/√Hz	C
Input Current Noise	f > 100 kHz		1.7	3				pA/√Hz	C
Differential Gain	G = 2, PAL, V_O = 1.4V_{PP}, R_L = 150 Ω		0.01					%	C
Differential Phase	G = 2, PAL, V_O = 1.4V_{PP}, R_L = 150 Ω		0.03					°	C
DC PERFORMANCE(2)									
Open-Loop Voltage Gain (A_{OL})	V_O = 0 V, Input-Referred	59	62		52	57		dB	A
Input Offset Voltage	V_{CM} = 0 V		±1.8	±3.5		±1.8	±3.5	mV	A
Average input offset voltage drift	V_{CM} = 0 V		7			7		µV/°C	C
Input Bias Current	V_{CM} = 0 V		39			39		µA	C
Average input bias current drift	V_{CM} = 0 V		50			50		nA/°C	C
Input Offset Current	V_{CM} = 0 V		±700			±700		nA	C
Inverting Input Bias Current Drift	V_{CM} = 0 V		50			50		nA/°C	C

(1) Test levels: **(A)** 100% tested. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

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ELECTRICAL CHARACTERISTICS: V_S = ±5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, and G = 2, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			210°C			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT									
Common-Mode Input Range (CMIR)(3)		±3.9			±3.2			V	A
Common-Mode Rejection Ratio	V_{CM} = 0 V, Input-Referred	73			71			dB	A
Input Impedance									
Differential mode	V_{CM} = 0 V		18 || 0.8					kΩ || pf	C
Common mode	V_{CM} = 0 V		6 || 1					MΩ || pf	
OUTPUT									
Output Voltage Swing	No Load	±3.5	±3.7		±3.4			V	A
	R_L = 100 Ω	±3.5	±3.6		±3.4				
Short-Circuit Output Current	Output Shorted to Ground		±90			±50		mA	C
Closed-Loop Output Impedance	G = 2, f ≤ 100 kHz		0.04					Ω	C
POWER SUPPLY									
Maximum Operating Voltage				±5			±5	V	A
Maximum Quiescent Current	V_S = ±5 V			6.6			6.8	mA	A
Minimum Quiescent Current	V_S = ±5 V	5			5			mA	A
Power-Supply Rejection Ratio (±PSRR)	Input Referred	62			61			dB	A

(3) Tested < 3 dB below minimum specified CMRR at ±CMIR limits.

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ELECTRICAL CHARACTERISTICS: V_S = 5 V

R_F = 402 Ω, R_L = 100 Ω, and G = 2, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			210°C			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX	MIN	TYP	MAX		
AC PERFORMANCE									
Small-Signal Bandwidth	G = 1, V_O = 0.1V_{PP}, R_F = 0 Ω		800					MHz	C
	G = 2, V_O = 0.1V_{PP}		240			100		MHz	C
	G = 10, V_O = 0.1V_{PP}		30					MHz	C
Gain Bandwidth Product	G ≥ 20	150	270			202		MHz	C
Bandwidth for 0.1dB Gain Flatness	G = 2, V_O = 0.1V_{PP}		38					MHz	C
Peaking at a Gain of +1	V_O = 0.1V_{PP}, R_F = 0 Ω		0.5					dB	C
Large-Signal Bandwidth	G = 2, V_O = 2V_{PP}		85					MHz	C
Slew Rate	G = 2, 2-V Step		240			185		V/µs	C
Rise and Fall Time	G = 2, V_O = 0.2-V Step		10.5			11.5		ns	C
Settling Time to 0.02%	G = 2, V_O = 2-V Step		22			28		ns	C
Settling Time to 0.1%	G = 2, V_O = 2-V Step		18			24		ns	C
Harmonic Distortion	G = 2, f = 1 MHz, V_O = 2V_{PP}								
2nd harmonic	R_L = 200 Ω		-85			-76		dBc	C
	R_L = 500 Ω		-90			-75		dBc	C
3rd harmonic	R_L = 200 Ω		-95			-92		dBc	C
	R_L = 500 Ω		-110			-91		dBc	C
Input Voltage Noise	f > 100 kHz		2.5			4.5		nV/√Hz	C
Input Current Noise	f > 100 kHz		1.7					pA/√Hz	C
Differential Gain	G = 2, PAL, V_O = 1.4V_{PP}, R_L = 150 Ω		0.01					%	C
Differential Phase	G = 2, PAL, V_O = 1.4V_{PP}, R_L = 150 Ω		0.03					°	C
DC PERFORMANCE(2)									
Open-Loop Voltage Gain (A_{OL})	V_O = 0 V, Input-Referred	60	65		58	64		dB	A
Input Offset Voltage	V_{CM} = 0 V		1.8	3.5		1.8	3.5	mV	A
Average input offset voltage drift	V_{CM} = 0 V		7			7		µV/°C	C
Input Bias Current	V_{CM} = 0 V		39			39		µA	C
Average input bias current drift	V_{CM} = 0 V		50			50		nA/°C	C
Input Offset Current	V_{CM} = 0 V		±700			±700		nA	C
Inverting Input Bias Current Drift	V_{CM} = 0 V		50			50		nA/°C	C

(1) Test levels: **(A)** 100% tested. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
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ELECTRICAL CHARACTERISTICS: V_S = 5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, and G = 2, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			210°C			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX	MIN	TYP	MAX		
INPUT									
Common-Mode Input Range (CMIR)(3)		3.9			3.2			V	A
Common-Mode Rejection	V_{CM} = 0 V, Input-Referred	72			70			dB	A
Input Impedance									
Differential mode	V_{CM} = 0 V		18 || 0.8					kΩ || pf	C
Common mode	V_{CM} = 0 V		6 || 1.0					MΩ || pf	
OUTPUT									
Output Voltage Swing	No Load	3.4	3.7		3.4			V	A
	R_L = 100 Ω	3.4	3.6		3.4				
Short-Circuit Output Current	Output Shorted to Ground		±60			±37		mA	C
Closed-Loop Output Impedance	G = 2, f ≤ 100 kHz		0.04					Ω	C
POWER SUPPLY									
Maximum Operating Voltage				5			5	V	A
Maximum Quiescent Current	V_S = ±5 V			5.8			6.5	mA	A
Minimum Quiescent Current	V_S = ±5 V	3.8			4			mA	A
Power-Supply Rejection Ratio (±PSRR)	Input Referred	62			61			dB	C

(3) Tested < 3 dB below minimum specified CMRR at ±CMIR limits.

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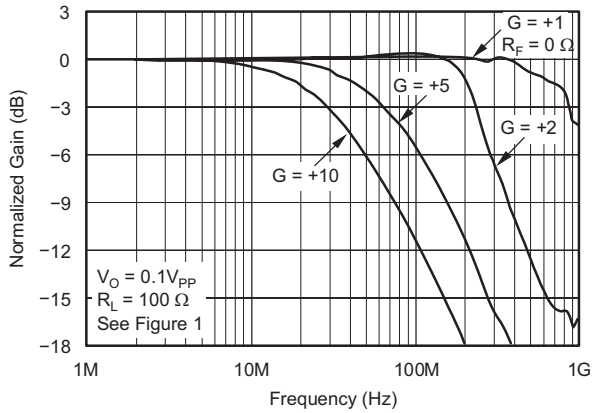
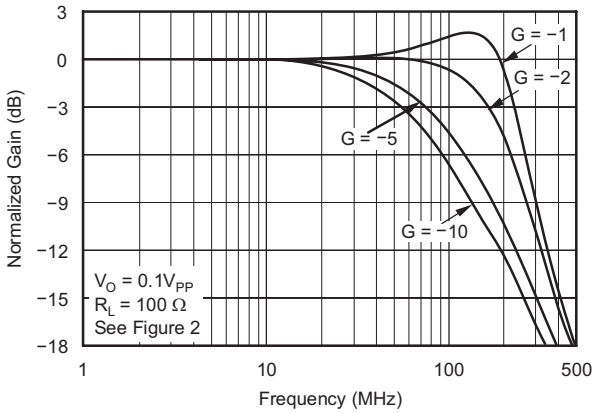
TYPICAL CHARACTERISTICS: V_S = ±5 V

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

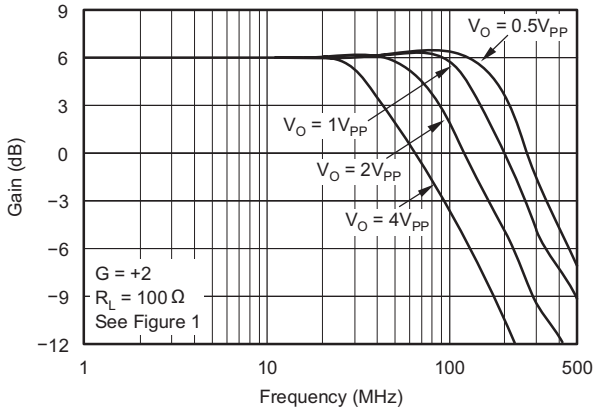
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



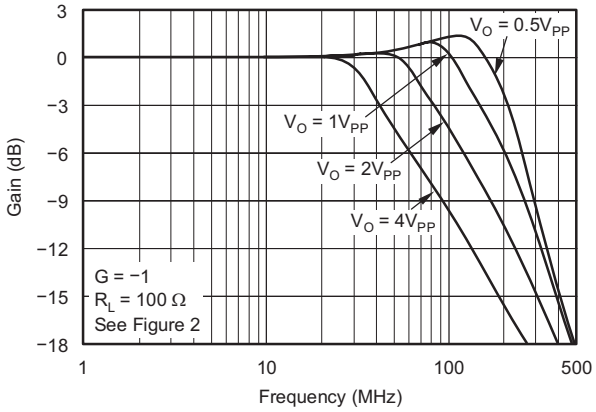
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



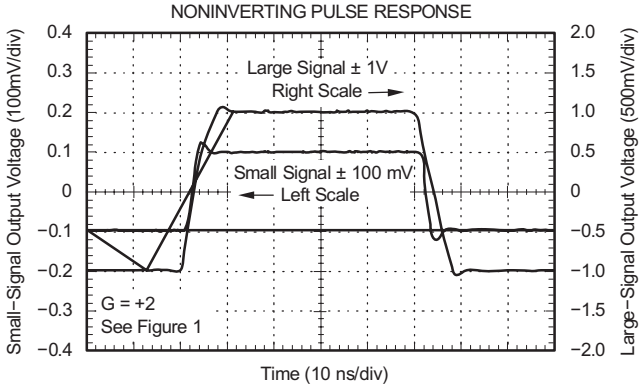
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



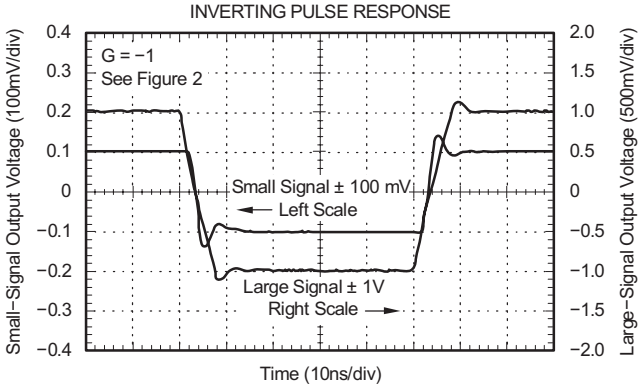
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



INVERTING PULSE RESPONSE



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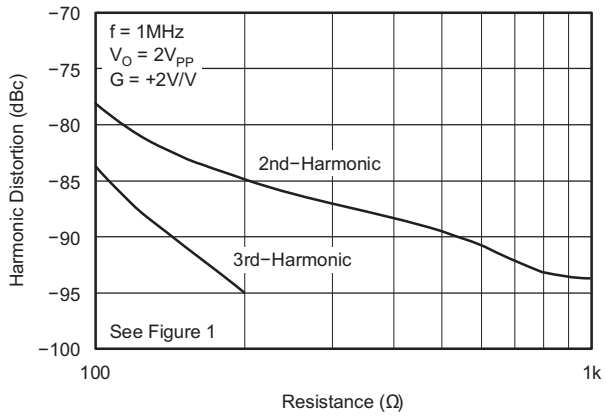
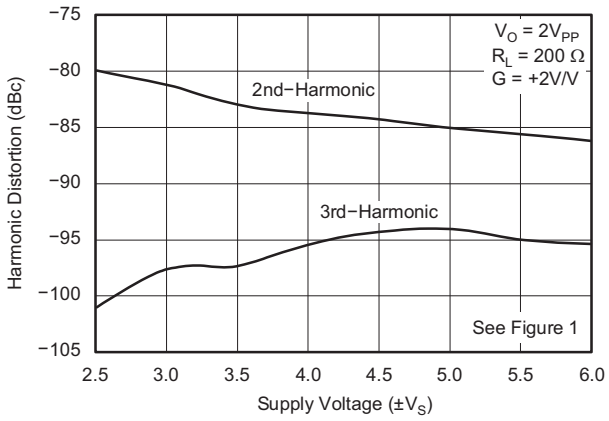
TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

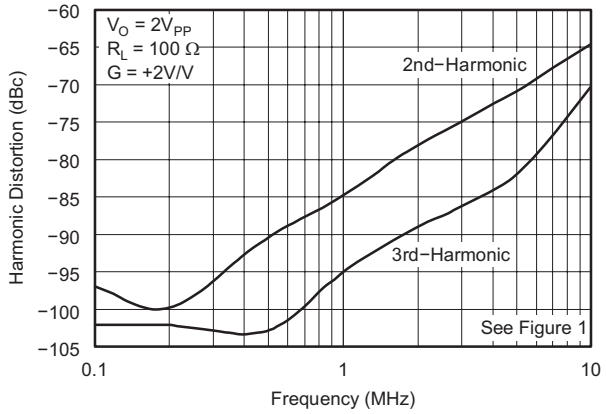
HARMONIC DISTORTION vs LOAD RESISTANCE



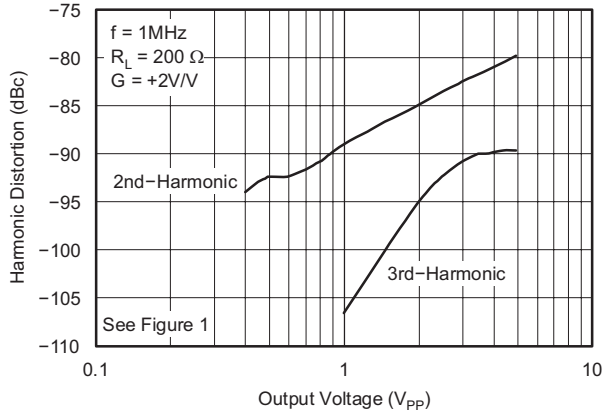
1MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



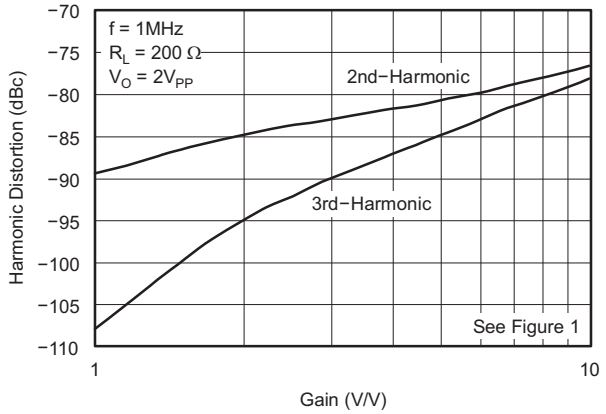
HARMONIC DISTORTION vs FREQUENCY



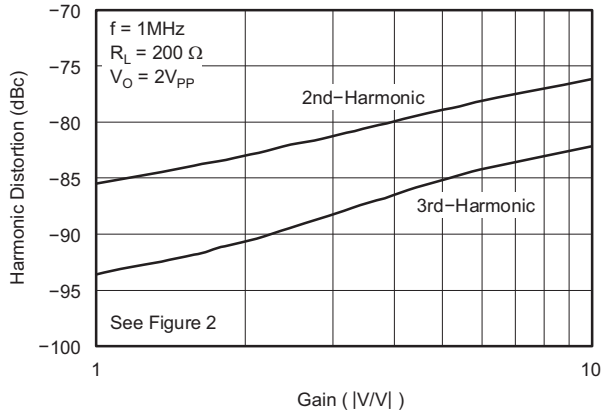
HARMONIC DISTORTION vs OUTPUT VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



HARMONIC DISTORTION vs INVERTING GAIN



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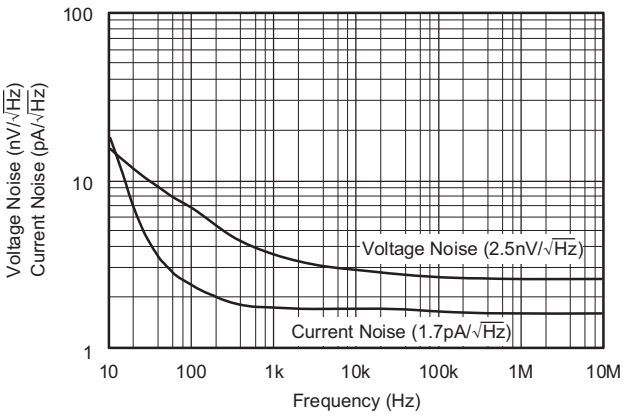
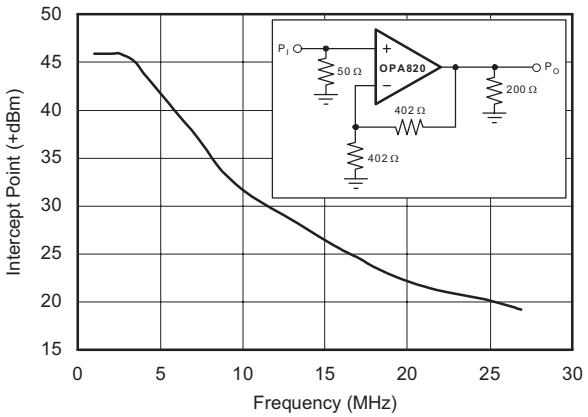
TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

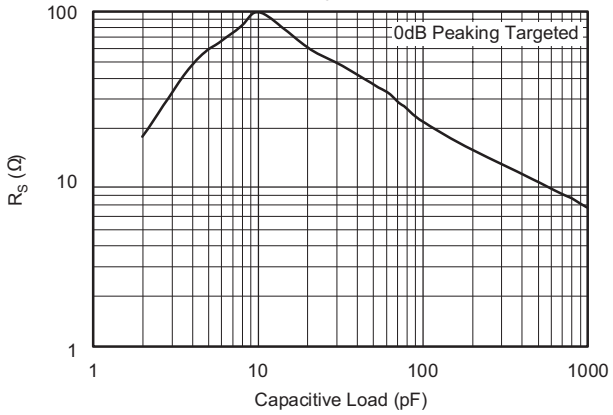
INPUT VOLTAGE AND CURRENT NOISE



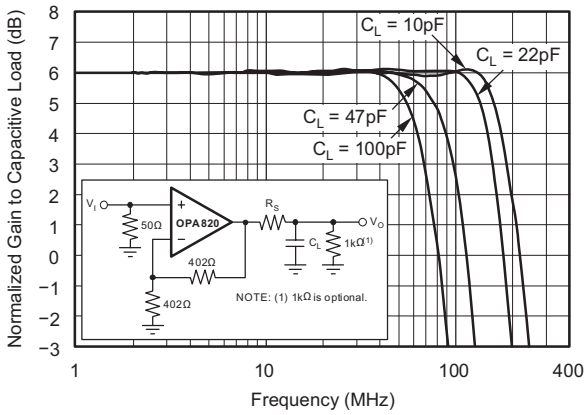
TWO−TONE, 3RD−ORDER INTERMODULATION INTERCEPT



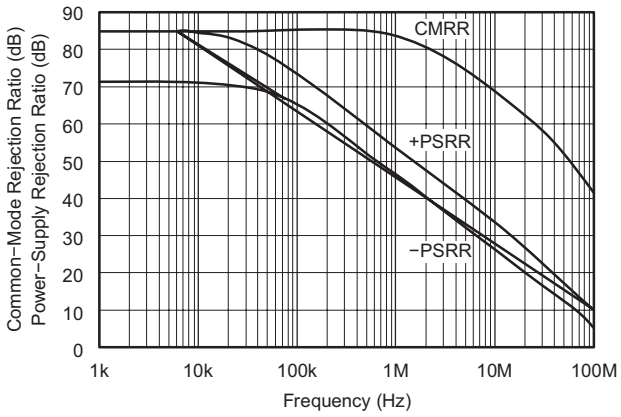
RECOMMENDED R_S vs CAPACITIVE LOAD



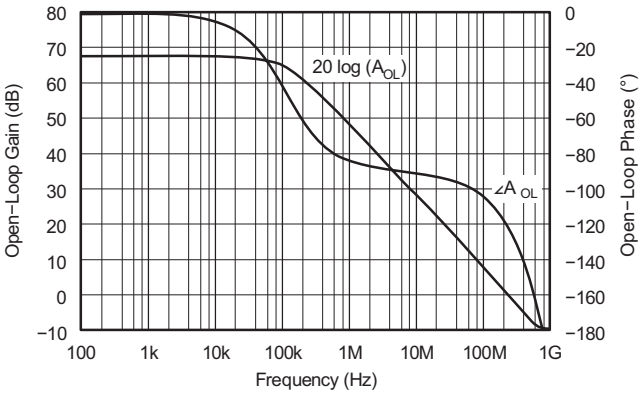
FREQUENCY RESPONSE vs CAPACITIVE LOAD



CMRR AND PSRR vs FREQUENCY



OPEN−LOOP GAIN AND PHASE



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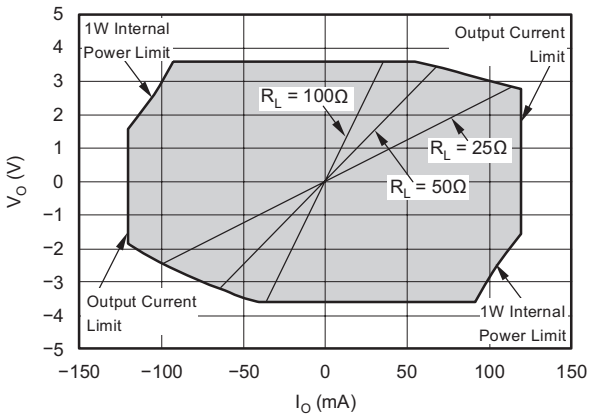
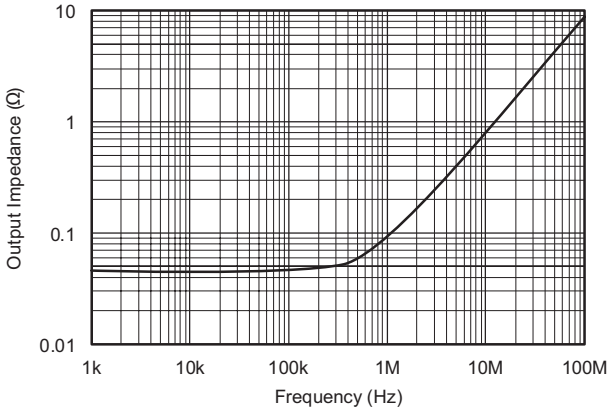
TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

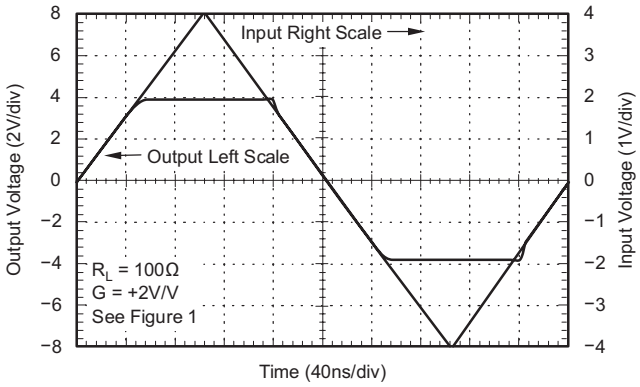
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



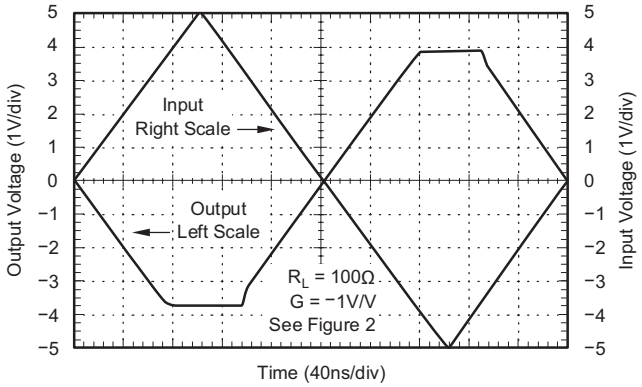
CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY



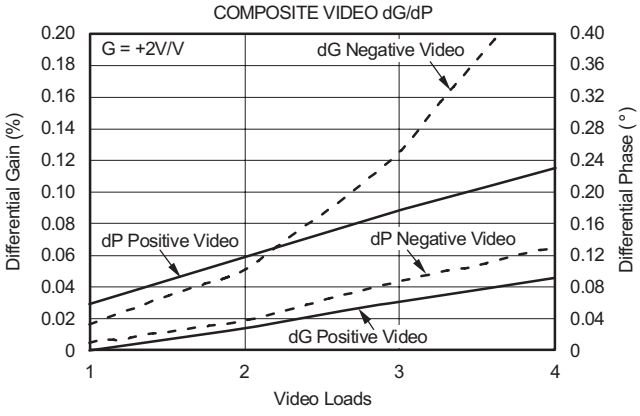
NONINVERTING OVERDRIVE RECOVERY



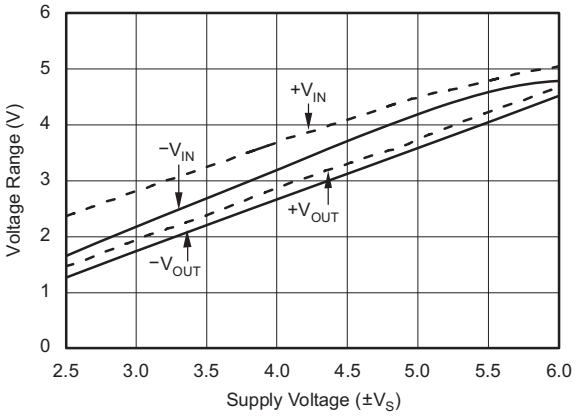
INVERTING OVERDRIVE RECOVERY



COMPOSITE VIDEO dG/dP



COMMON−MODE INPUT RANGE AND OUTPUT SWING vs SUPPLY VOLTAGE



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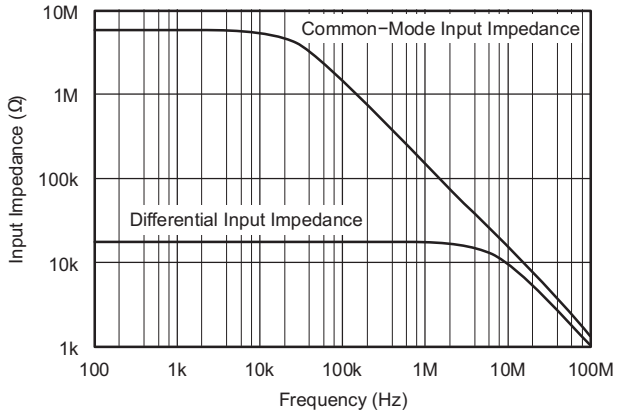
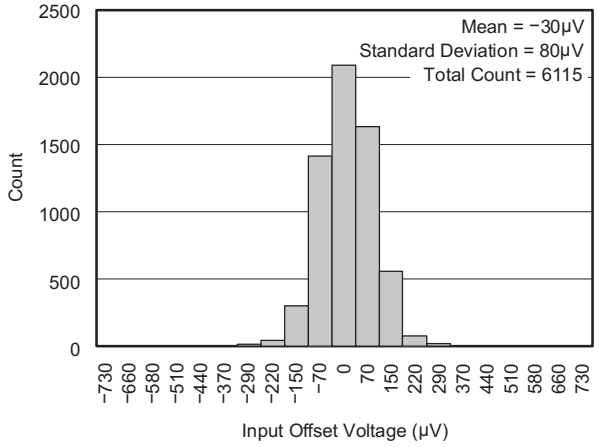
TYPICAL CHARACTERISTICS: V_S = ±5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

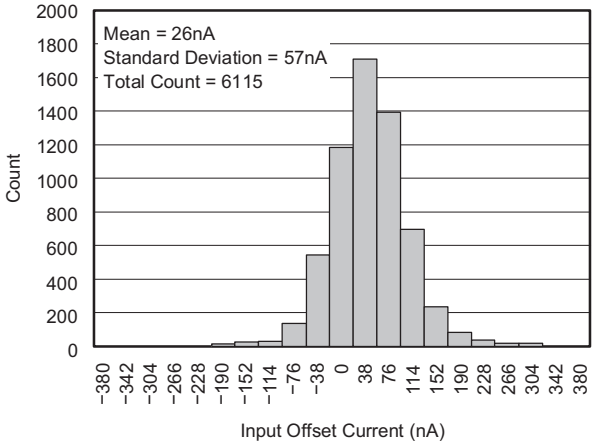
COMMON−MODE AND DIFFERENTIAL INPUT IMPEDANCE



TYPICAL INPUT OFFSET VOLTAGE DISTRIBUTION



TYPICAL INPUT OFFSET CURRENT DISTRIBUTION



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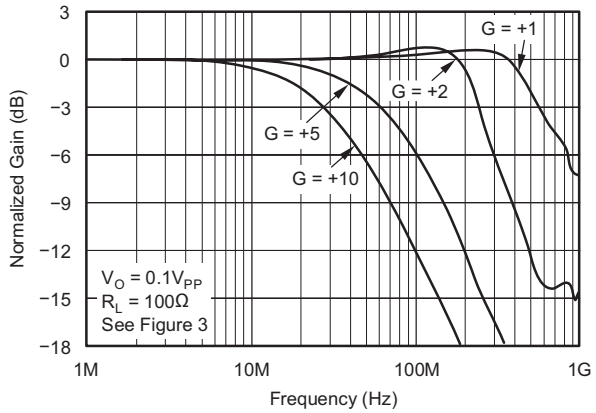
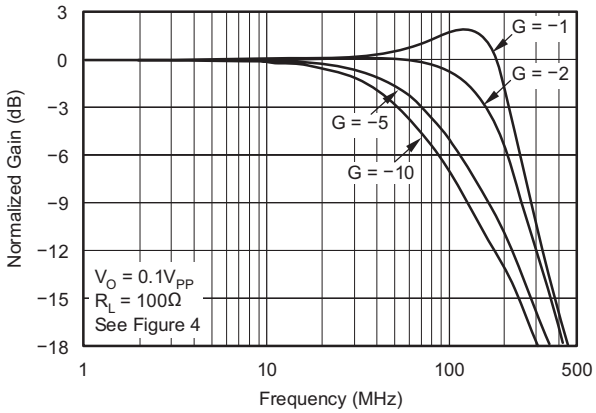
TYPICAL CHARACTERISTICS: V_S = 5 V

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

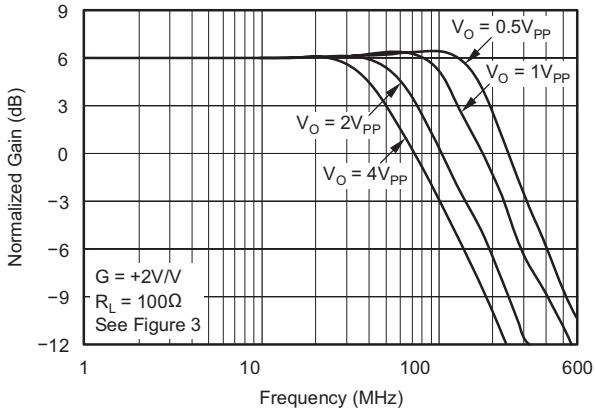
NONINVERTING SMALL−SIGNAL FREQUENCY RESPONSE



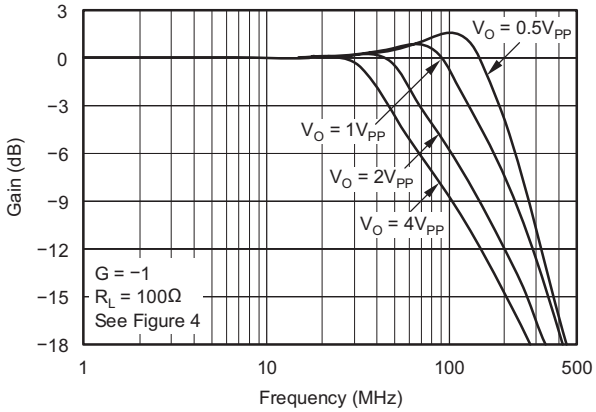
INVERTING SMALL−SIGNAL FREQUENCY RESPONSE



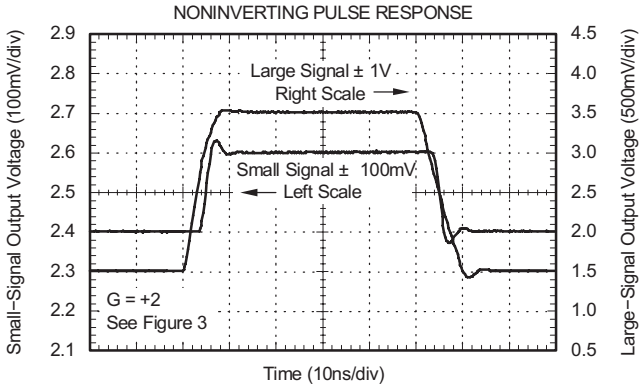
NONINVERTING LARGE−SIGNAL FREQUENCY RESPONSE



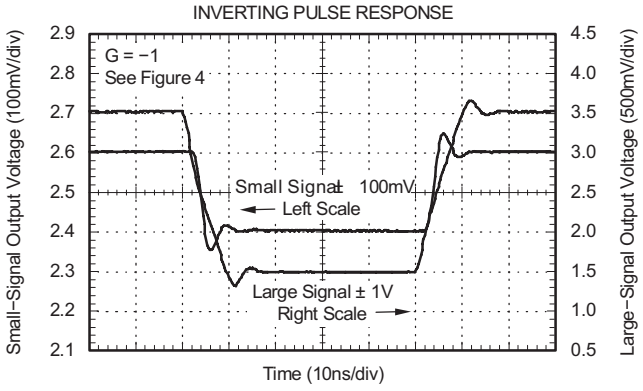
INVERTING LARGE−SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



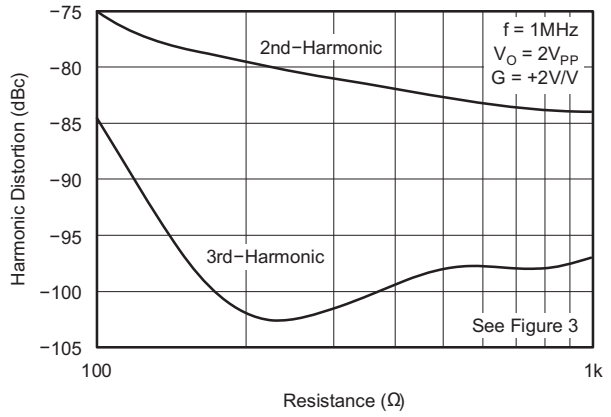
INVERTING PULSE RESPONSE



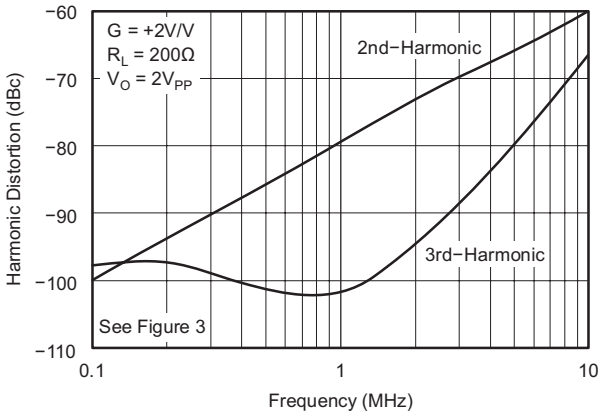
TYPICAL CHARACTERISTICS: V_S = 5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

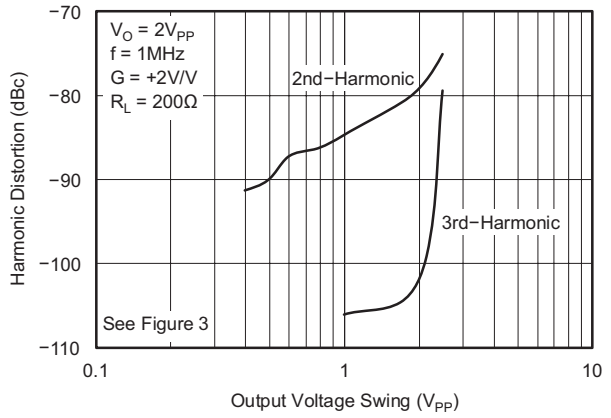
HARMONIC DISTORTION vs LOAD RESISTANCE



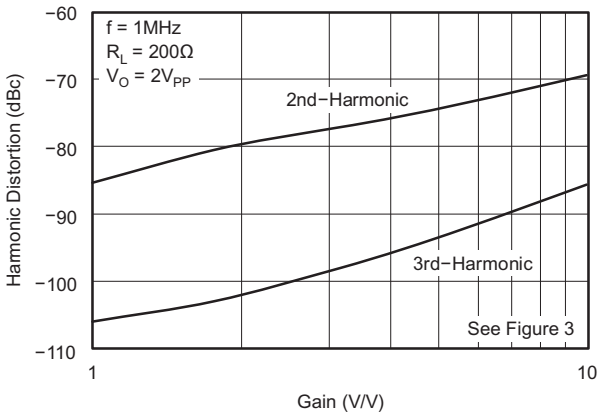
HARMONIC DISTORTION vs FREQUENCY



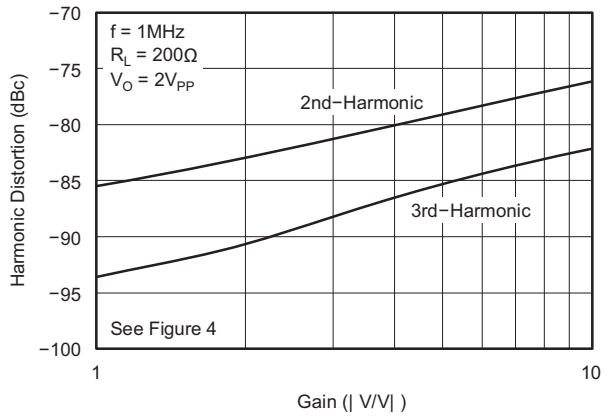
HARMONIC DISTORTION vs OUTPUT VOLTAGE



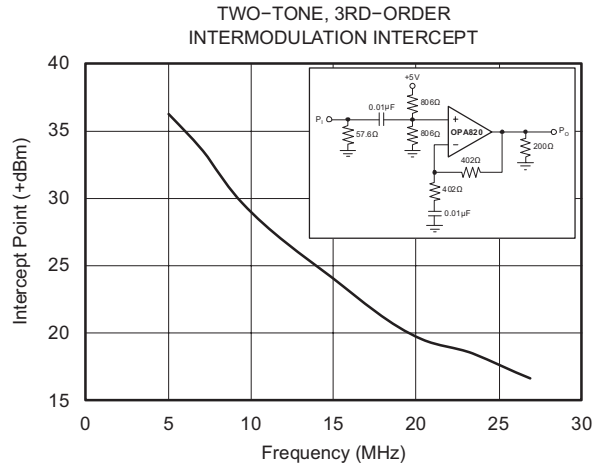
HARMONIC DISTORTION vs NONINVERTING GAIN



HARMONIC DISTORTION vs INVERTING GAIN



TWO−TONE, 3RD−ORDER INTERMODULATION INTERCEPT



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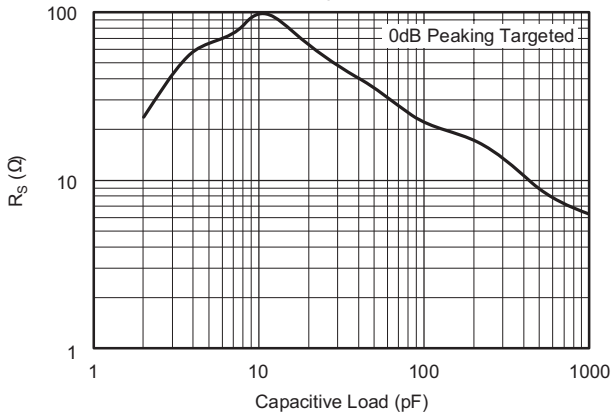
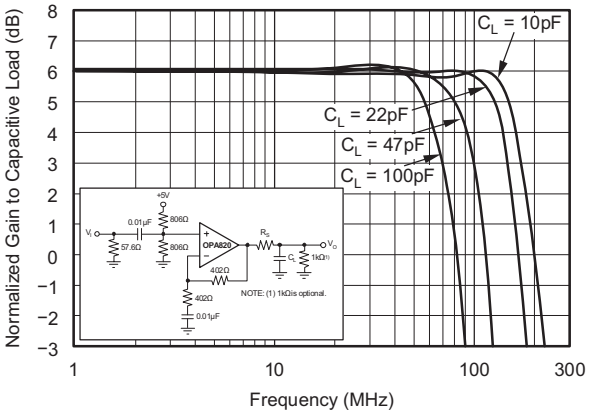
TYPICAL CHARACTERISTICS: V_S = 5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2 and T_A = 25°C unless otherwise noted.

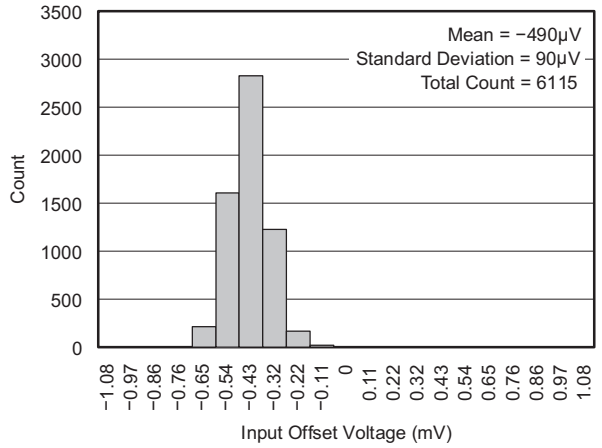
RECOMMENDED R_S vs CAPACITIVE LOAD



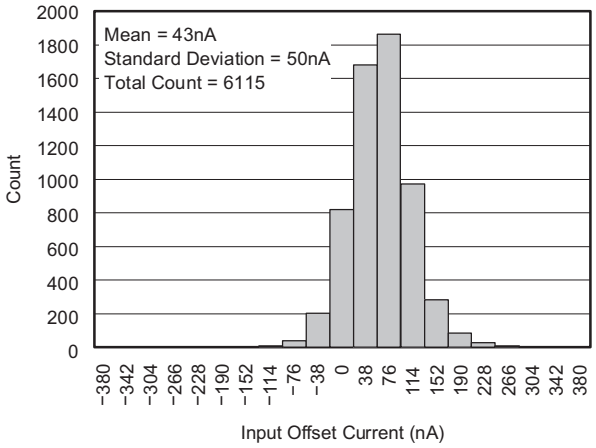
FREQUENCY RESPONSE vs CAPACITIVE LOAD



TYPICAL INPUT OFFSET VOLTAGE DISTRIBUTION



TYPICAL INPUT OFFSET CURRENT DISTRIBUTION



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APPLICATION INFORMATION

Wideband Voltage-Feedback Operation

The combination of speed and dynamic range offered by the OPA820 is easily achieved in a wide variety of application circuits, providing that simple principles of good design practice are observed. For example, good power-supply decoupling, as shown in Figure 2, is essential to achieve the lowest possible harmonic distortion and smooth frequency response.

Proper PC board layout and careful component selection will maximize the performance of the OPA820 in all applications, as discussed in the following sections of this data sheet.

Figure 2 shows the gain of +2 configuration used as the basis for most of the typical characteristics. Most of the curves were characterized using signal sources with 50-Ω driving impedance and with measurement equipment presenting 50-Ω load impedance. In Figure 2, the 50-Ω shunt resistor at the V_I terminal matches the source impedance of the test generator while the 50-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet specifications refer to the voltage swings at the output pin (V_O in Figure 2). The 100-Ω load, combined with the 804-Ω total feedback network load, presents the OPA820 with an effective load of approximately 90 Ω in Figure 2.

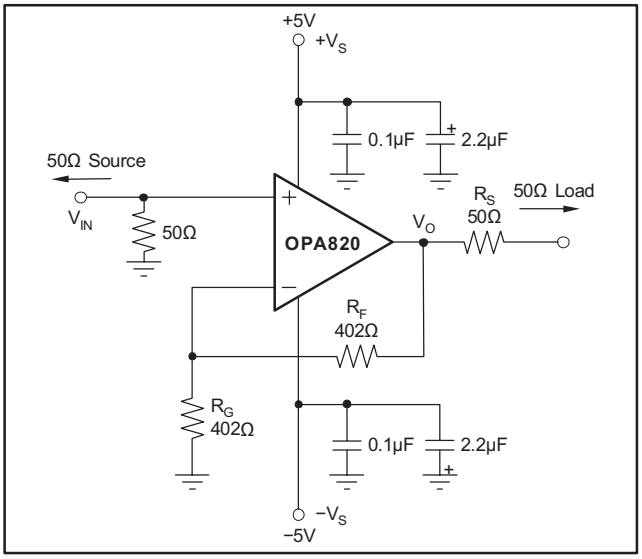

Figure 2. Gain of +2, High-Frequency Application and Characterization Circuit

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Wideband Inverting Operation

Operating the OPA820 as an inverting amplifier has several benefits and is particularly useful when a matched 50-Ω source and input impedance is required. Figure 3 shows the inverting gain of −1 circuit used as the basis of the inverting mode typical characteristics.

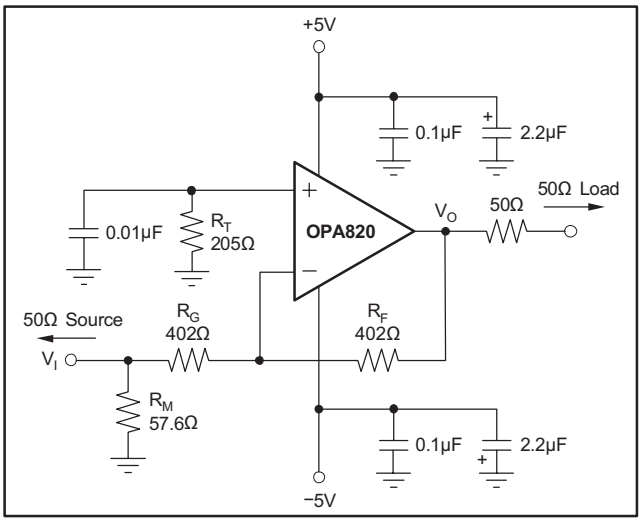

Figure 3. Inverting G = −1 Specifications and Test Circuit

In the inverting case, just the feedback resistor appears as part of the total output load in parallel with the actual load. For the 100-Ω load used in the typical characteristics, this gives a total load of 80 Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case 402 Ω for a gain of −1) while an additional input matching resistor (R_M) can be used to set the total input impedance equal to the source if desired. In this case, R_M = 57.6 Ω in parallel with the 402-Ω gain setting resistor gives a matched input impedance of 50 Ω. This matching is only needed when the input needs to be matched to a source impedance, as in the characterization testing done using the circuit of Figure 3.

The OPA820 offers extremely good DC accuracy as well as low noise and distortion. To take full advantage of that DC precision, the total DC impedance looking out of each of the input nodes must be matched to get bias current cancellation. For the circuit of Figure 32, this requires the 205-Ω resistor shown to ground on the noninverting input. The calculation for this resistor includes a DC-coupled 50-Ω source impedance along with R_G and R_M. Although this resistor will provide cancellation for the bias current, it must be well decoupled (0.01 µF in Figure 3) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50 Ω at higher gains, the bandwidth for the circuit in Figure 3 will far exceed the bandwidth at that same gain magnitude for the noninverting circuit of Figure 2. This occurs due to the lower noise gain for the circuit of Figure 3 when the 50-Ω source impedance is included in the analysis. For instance, at a signal gain of −10 (R_G = 50 Ω, R_M = open, R_F = 499 Ω) the noise gain for the circuit of Figure 3 will be 1 + 499 Ω/(50 Ω + 50 Ω) = 6 as a result of adding the 50-Ω source in the noise gain equation. This gives considerable higher bandwidth than the noninverting gain of +10. Using the 240-MHz gain bandwidth product for the OPA820, an inverting gain of −10 from a 50-Ω source to a 50-Ω R_G gives 55-MHz bandwidth, whereas the noninverting gain of +10 gives 30 MHz.

Wideband Single-Supply Operation

Figure 4 shows the AC-coupled, single 5-V supply, gain of +2 V/V circuit configuration used as a basis for the 5 V only Electrical and Typical Characteristics. The key requirement for single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 4 establishes an input midpoint bias using a simple resistive divider from the 5-V supply (two 806-Ω resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 0.9 V of the negative supply and 0.5 V of the positive supply, giving a $3.6V_{PP}$ input

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signal range. The input impedance matching resistor (57.6 Ω) used in Figure 4 is adjusted to give a 50-Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1. This puts the input DC bias voltage (2.5 V) on the output as well. On a single 5-V supply, the output voltage can swing to within 1.3 V of either supply pin while delivering more than 80-mA output current giving 2.4-V output swing into 100 Ω (5.6-dBm maximum at the matched load).

Figure 5 shows the AC-coupled, single 5-V supply, gain of −1 V/V circuit configuration used as a basis for the 5 V only Typical Characteristic curves. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.01-µF decoupling capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5-V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC blocked by the input capacitor, will also appear at the output pin.

The single-supply test circuits of Figure 4 and Figure 4 show 5-V operation. These same circuits can be used over a singlesupply range of 5 V to 12 V. Operating on a single 12-V supply, with the Absolute Maximum Supply voltage specification of 13 V, gives adequate design margin for the typical ±5% supply tolerance.

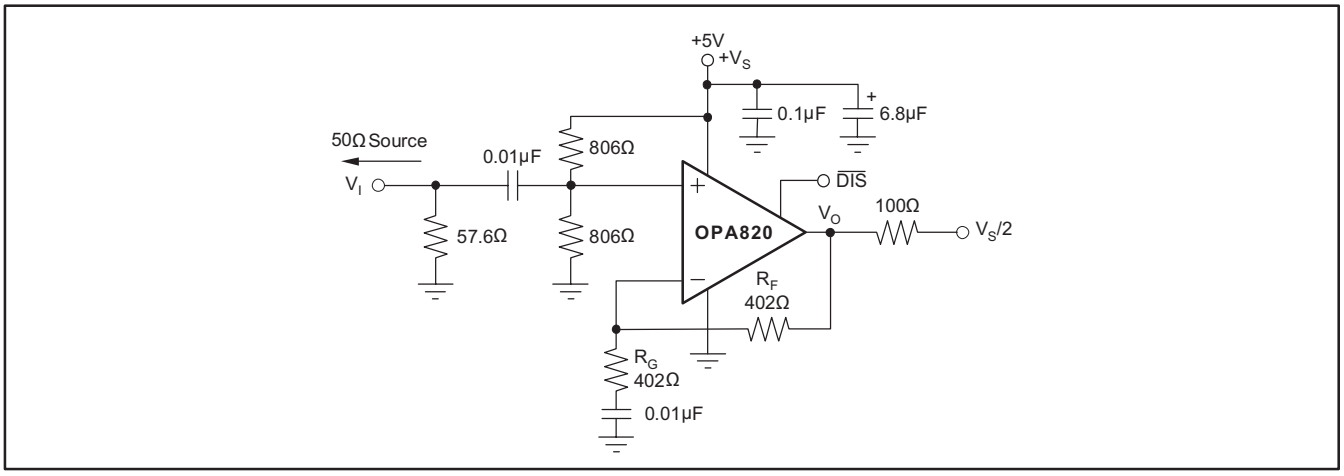

Figure 4. AC-Coupled, G = +2 V/V, Single-Supply Specifications and Test Circuit

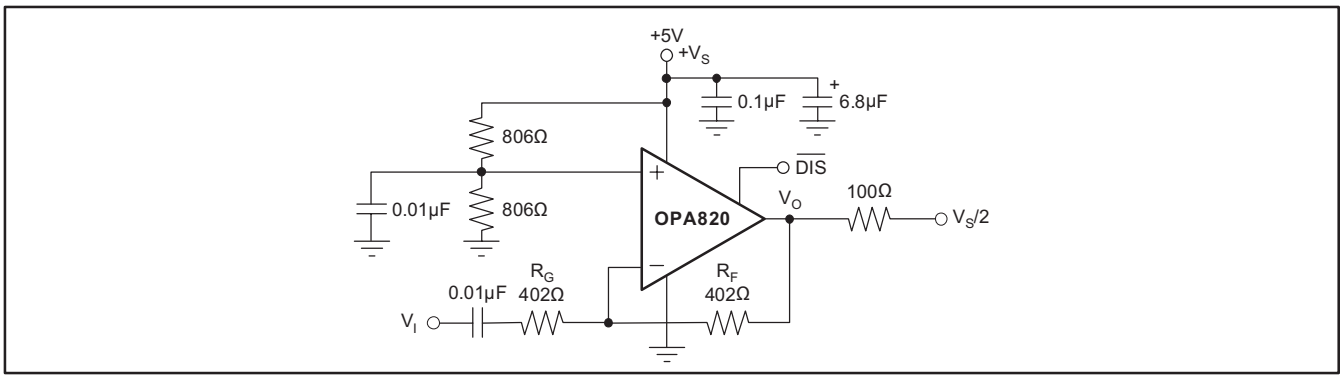

Figure 5. AC-Coupled, G = −1 V/V, Single-Supply Specifications and Test Circuit

Buffering High-Performance ADCs

To achieve full performance from a high dynamic range ADC, considerable care must be exercised in the design of the input amplifier interface circuit. The example circuit on the front page shows a typical AC-coupled interface to a very high dynamic range converter. This AC-coupled example allows the OPA820 to be operated using a signal range that swings symmetrically around ground (0 V). The $2V_{PP}$ swing is then level-shifted through the blocking capacitor to a midscale reference level, which is created by a well-decoupled resistive divider off the converter's internal reference voltages. To have a negligible effect (1 dB) on the rated spurious-free dynamic range (SFDR) of the converter, the amplifier's SFDR should be at least 18 dB greater than the converter. The OPA820 has minimal effect on the rated distortion of the ADS850, given its 79-dB SFDR at $2V_{PP}$, 1 MHz. The

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> 90-dB (< 1MHz) SFDR for the OPA820 in this configuration implies a < 3-dB degradation (for the system) from the converter's specification. For further SFDR improvement with the OPA820, a differential configuration is suggested.

Successful application of the OPA820 for ADC driving requires careful selection of the series resistor at the amplifier output, along with the additional shunt capacitor at the ADC input. To some extent, selection of this RC network will be determined empirically for each converter. Many high performance CMOS ADCs, such as the ADS850, perform better with the shunt capacitor at the input pin. This capacitor provides low source impedance for the transient currents produced by the sampling process. Improved SFDR is often obtained by adding this external capacitor, whose value is often recommended in this converter data sheet. The external capacitor, in combination with the built-in capacitance of the ADC input, presents a significant capacitive load to the OPA820. Without a series isolation resistor, an undesirable peaking or loss of stability in the amplifier may result.

Since the DC bias current of the CMOS ADC input is negligible, the resistor has no effect on overall gain or offset accuracy. Refer to the typical characteristic R_S vs Capacitive Load to obtain a good starting value for the series resistor. This will ensure flat frequency response to the ADC input. Increasing the external capacitor value will allow the series resistor to be reduced. Intentionally bandlimiting using this RC network can also be used to limit noise at the converter input.

Video Line Driving

Most video distribution systems are designed with 75-Ω series resistors to drive a matched 75-Ω cable. In order to deliver a net gain of 1 to the 75-Ω matched load, the amplifier is typically set up for a voltage gain of +2, compensating for the 6-dB attenuation of the voltage divider formed by the series and shunt 75-Ω resistors at either end of the cable.

The circuit of Figure 2 applies to this requirement if all references to 50-Ω resistors are replaced by 75-Ω values. Often, the amplifier gain is further increased to 2.2, which recovers the additional DC loss of a typical long cable run. This change would require the gain resistor (R_G) in Figure 2 to be reduced from 402 Ω to 335 Ω. In either case, both the gain flatness and the differential gain/phase performance of the OPA820 will provide exceptional results in video distribution applications. Differential gain and phase measure the change in overall small-signal gain and phase for the color sub-carrier frequency (3.58 MHz in NTSC systems) versus changes in the large-signal output level (which represents luminance information in a composite video signal). The OPA820, with the typical 150-Ω load of a single matched video cable, shows less than 0.01%/0.01° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance would be observed for multiple video signals, as shown in Figure 6.

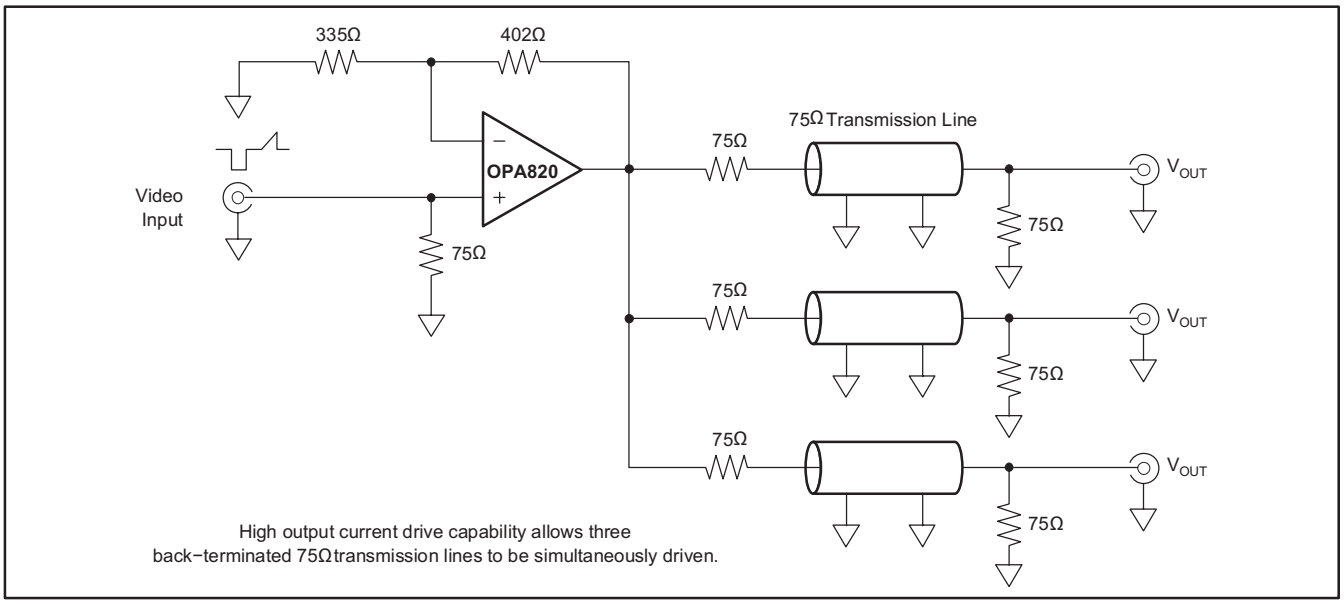

Figure 6. Video Distribution Amplifier

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Single Operational Amplifier Differential Amplifier

The voltage-feedback architecture of the OPA820, with its high common-mode rejection ratio (CMRR), will provide exceptional performance in differential amplifier configurations. Figure 7 shows a typical configuration. The starting point for this design is the selection of the R_F value in the range of 200 Ω to 2 kΩ. Lower values reduce the required R_G, increasing the load on the V_2 source and on the OPA820 output. Higher values increase output noise as well as the effects of parasitic board and device capacitances. Following the selection of R_F, R_G must be set to achieve the desired inverting gain for V_2. Remember that the bandwidth will be set approximately by the gain bandwidth product (GBP) divided by the noise gain ($1 + R_F/R_G$). For accurate differential operation (that is, good CMRR), the ratio R_2/R_1 must be set equal to R_F/R_G.

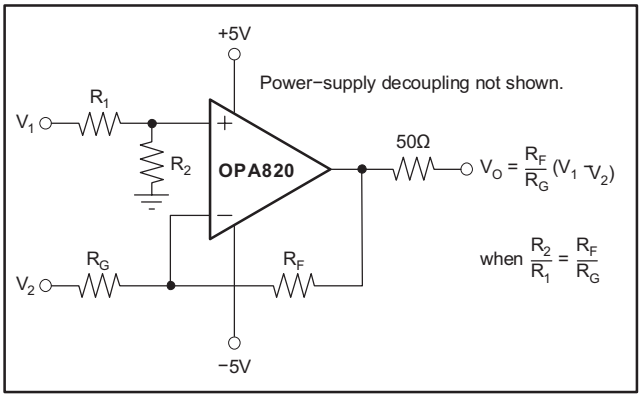

Figure 7. High-Speed, Single Differential Amplifier

Usually, it is best to set the absolute values of R_2 and R_1 equal to R_F and R_G, respectively; this equalizes the divider resistances and cancels the effect of input bias currents. However, it is sometimes useful to scale the values of R_2 and R_1 in order to adjust the loading on the driving source, V_1. In most cases, the achievable low-frequency CMRR will be limited by the accuracy of the resistor values. The 85-dB CMRR of the OPA820 itself will not determine the overall circuit CMRR unless the resistor ratios are matched to better than 0.003%. If it is necessary to trim the CMRR, then R_2 is the suggested adjustment point.

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DAC Transimpedance Amplifier

High-frequency digital-to-analog converters (DACs) require a low-distortion output amplifier to retain their SFDR performance into real-world loads. See Figure 8 for a single-ended output drive implementation. In this circuit, only one side of the complementary output drive signal is used. The diagram shows the signal output current connected into the virtual ground-summing junction of the OPA820, which is set up as a transimpedance stage or I-V converter. The unused current output of the DAC is connected to ground. If the DAC requires its outputs to be terminated to a compliance voltage other than ground for operation, then the appropriate voltage level may be applied to the non-inverting input of the OPA820.

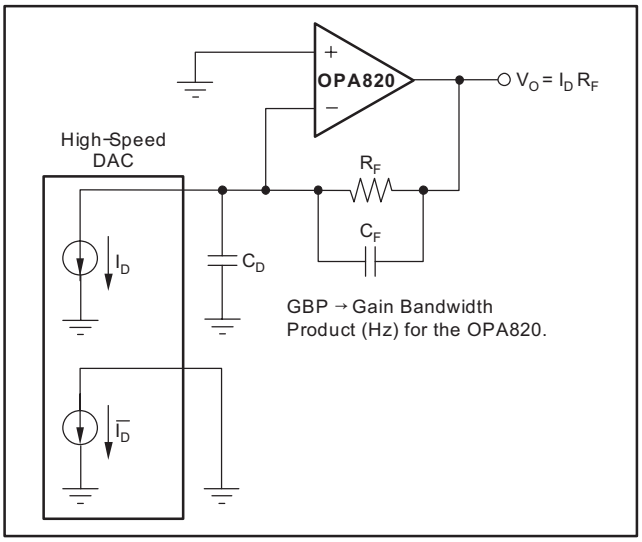

Figure 8. Wideband, Low-Distortion DAC Transimpedance Amplifier

The DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D) will produce a zero in the noise gain for the OPA820 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise-gain peaking. To achieve a flat transimpedance frequency response, this pole in the feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

which will give a corner frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (2)$$

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Active Filters

Most active filter topologies will have exceptional performance using the broad bandwidth and unity-gain stability of the OPA820. Topologies employing capacitive feedback require a unity-gain stable, voltage-feedback op amp. Sallen-Key filters simply use the operational amplifier as a noninverting gain stage inside an RC network. Either current- or voltage-feedback op amps may be used in Sallen-Key implementations.

Figure 9 shows an example Sallen-Key low-pass filter, in which the OPA820 is set up to deliver a low-frequency gain of +2. The filter component values have been selected to achieve a maximally-flat Butterworth response with a 5-MHz, −3-dB bandwidth. The resistor values have been slightly adjusted to compensate for the effects of the 240-MHz bandwidth provided by the OPA820 in this configuration. This filter may be combined with the ADC driver suggestions to provide moderate (2-pole) Nyquist filtering, limiting noise, and out-of-band harmonics into the input of an ADC. This filter will deliver the exceptionally low harmonic distortion required by high SFDR ADCs such as the ADS850 (14-bit, 10 MSPS, 82-dB SFDR).

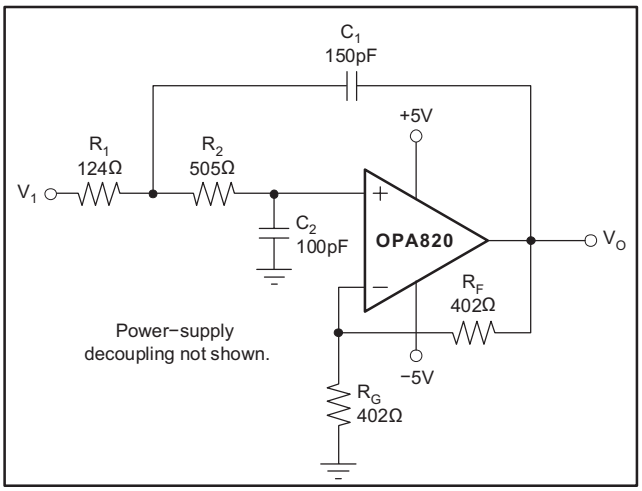

Figure 9. 5-MHz Butterworth Low-Pass Active Filter

Another type of filter, a high-Q bandpass filter, is shown in Figure 10. The transfer function for this filter is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{S\frac{R_3 + R_4}{R_1 R_4 C_1}}{S^2 + S\frac{1}{R_1 C_1} + \frac{R_3}{R_2 R_4 R_5 C_1 C_2}} \quad (3)$$

with

$$\omega_O^2 = \frac{R_3}{R_2 R_4 R_5 C_1 C_2} \quad (4)$$

and

$$\frac{\omega_O}{Q} = \frac{1}{R_1 C_1} \quad (5)$$

For the values chosen in Figure 10:

$$f_O = \frac{\omega_O}{2\pi} \simeq 1\text{MHz} \quad (6)$$

and Q = 100.

See Figure 11 for the frequency response of the filter shown in Figure 10.

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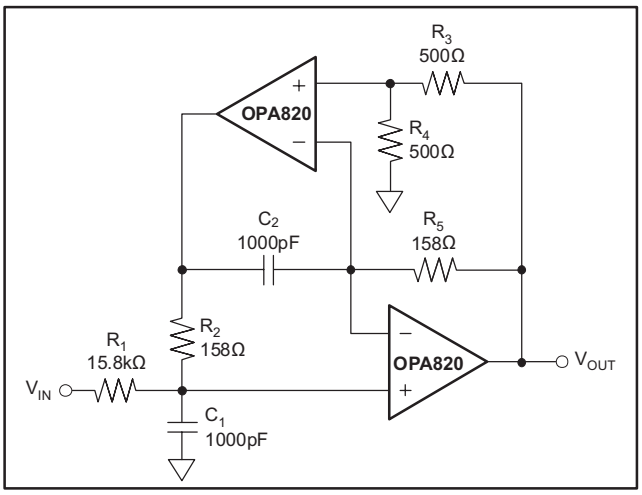

Figure 10. High-Q 1-MHz Bandpass Filter

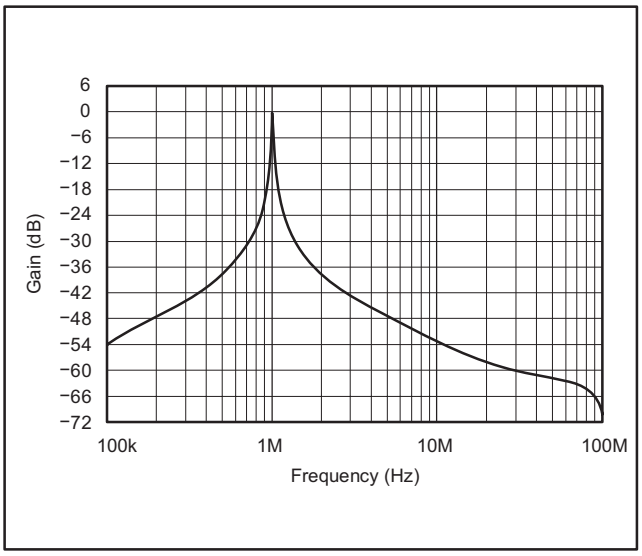

Figure 11. High-Q 1-MHz Bandpass Filter Frequency Response

DESIGN-IN TOOLS

Macromodels and Applications Support

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA820 and its circuit designs. This is particularly true for video and R_F amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA820 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small-signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

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OPERATING SUGGESTIONS

Optimizing Resistor Values

Since the OPA820 is a unity-gain stable, voltage-feedback operational amplifier, a wide range of resistor values may be used for the feedback and gain-setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. Usually, the feedback resistor value should be between 200 Ω and 1 kΩ. Below 200 Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA820. Above 1 kΩ, the typical parasitic capacitance (approximately 0.2 pF) across the feedback resistor may cause unintentional band limiting in the amplifier response. A direct short is suggested as a feedback for A_V = +1 V/V.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 2) to be less than about 200 Ω. The combined impedance $R_F||R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2-pF total parasitic on the inverting node, holding $R_F||R_G$ < 200 Ω will keep this pole above 400 MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be noted. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G may be set equal to the required termination value. However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50-Ω input matching resistor (= R_G) would require a 100-Ω feedback resistor, which would contribute to output loading in parallel with the external load. In such a case, it would be preferable to increase both the R_F and R_G values, and then achieve the input matching impedance with a third resistor to ground (see Figure 3). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

Bandwidth vs Gain

Voltage-feedback operational amplifiers exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP shown in the specifications. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low signal gains, most amplifiers will exhibit a more complex response with lower phase margin. The OPA820 is optimized to give a maximally-flat, 2nd-order Butterworth response in a gain of 2. In this configuration, the OPA820 has approximately 64° of phase margin and will show a typical −3-dB bandwidth of 240 MHz. When the phase margin is 64°, the closed-loop bandwidth is approximately $\sqrt{2}$ greater than the value predicted by dividing GBP by the noise gain.

Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 30-MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 280 MHz.

Output Drive Capability

The OPA820 has been optimized to drive the demanding load of a doubly-terminated transmission line. When a 50-Ω line is driven, a series 50 Ω into the cable and a terminating 50-Ω load at the end of the cable are used. Under these conditions, the cable impedance will appear resistive over a wide frequency range, and the total effective load on the OPA820 is 100 Ω in parallel with the resistance of the feedback network. The electrical characteristics show a ±3.6-V swing into this load—which will then be reduced to a ±1.8-V swing at the termination resistor. The ±75-mA output drive over temperature provides adequate current drive margin for this load. Higher voltage swings (and lower distortion) are achievable when driving higher impedance loads.

A single video load typically appears as a 150-Ω load (using standard 75-Ω cables) to the driving amplifier. The OPA820 provides adequate voltage and current drive to support up to three parallel video loads (50-Ω total load) for an NTSC signal. With only one load, the OPA820 achieves an exceptionally low 0.01%/0.03° dG/dP error.

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Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an operational amplifier is capacitive loading. A high-speed, high open-loop gain amplifier like the OPA820 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. In simple terms, the capacitive load reacts with the open-loop output resistance of the amplifier to introduce an additional pole into the loop and thereby decrease the phase margin. This issue has become a popular topic of application notes and articles, and several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S vs Capacitive Load and the resulting frequency response at the load. The criterion for setting the recommended resistor is maximum bandwidth, flat frequency response at the load. Since there is now a passive low-pass filter between the output pin and the load capacitance, the response at the output pin itself is typically somewhat peaked, and becomes flat after the roll-off action of the RC network. This is not a concern in most applications, but can cause clipping if the desired signal swing at the load is very close to the amplifier's swing limit. Such clipping would be most likely to occur in pulse response applications where the frequency peaking is manifested as an overshoot in the step response.

Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the OPA820. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA820 output pin (see the Board Layout section).

Distortion Performance

The OPA820 is capable of delivering an exceptionally low distortion signal at high frequencies and low gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions. Most of these plots are limited to 100-dB dynamic range. The OPA820 distortion does not rise above −90 dBc until either the signal level exceeds 0.9 V and/or the fundamental frequency exceeds 500 kHz. Distortion in the audio band is ≤ −100 dBc.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is the sum of $R_F + R_G$, whereas in the inverting configuration this is just R_F (see Figure 2). Increasing the output voltage swing increases harmonic distortion directly. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again, a 6-dB increase in gain will increase the 2nd- and 3rd-harmonic by 6 dB even with a constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases because of the roll-off in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open-loop pole at approximately 100 kHz. Starting from the −85-dBc 2nd-harmonic for $2V_{PP}$ into 200 Ω, G = +2 distortion at 1 MHz (from the Typical Characteristics), the 2nd-harmonic distortion will not show any improvement below 100 kHz and will then be:

$$-100\ \text{dB} - 20\ \log\ (1\ \text{MHz}/100\ \text{kHz}) = -105\ \text{dBc}$$

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Noise Performance

The OPA820 complements its low harmonic distortion with low input noise terms. Both the input-referred voltage noise and the two input-referred current noise terms combine to give a low output noise under a wide variety of operating conditions. Figure 12 shows the operational amplifier noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

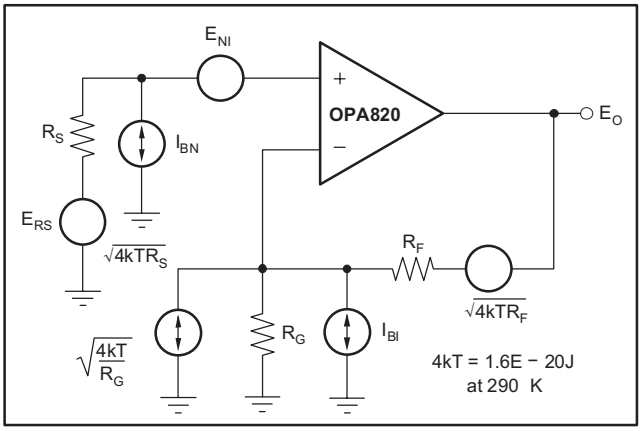

Figure 12. Operational Amplifier Noise Analysis Model

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 7 shows the general form for this output noise voltage using the terms presented in Figure 12.

$$E_O = \sqrt{[E^2_{NI} + (I_{BN}R_S)^2 + 4kTR_S]NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (7)$$

Dividing this expression by the noise gain (NG = 1 + R_F/R_G) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 8.

$$E_N = \sqrt{E^2_{NI} + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (8)$$

Evaluating these two equations for the OPA820 circuit presented in Figure 2 will give a total output spot noise voltage of 6.44 nV/√Hz and an equivalent input spot noise voltage of 3.22 nV/√Hz.

DC Offset Control

The OPA820 can provide excellent DC signal accuracy because of its high open-loop gain, high common-mode rejection, high power-supply rejection, and low input offset voltage and bias current offset errors. To take full advantage of this low input offset voltage, careful attention to input bias current cancellation is also required. The high-speed input stage for the OPA820 has a moderately high input bias current (9 μA typ into the pins) but with a very close match between the two input currents—typically 100-nA input offset current. The total output offset voltage may be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 2 would be to insert a 175-Ω series resistor into the noninverting input from the 50-Ω terminating resistor. When the 50-Ω source resistor is DC-coupled, this will increase the source impedance for the noninverting input bias current to 200 Ω. Since this is now equal to the impedance looking out of the inverting input ($R_F||R_G$), the circuit will cancel the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using a 402-Ω feedback resistor, this output error will now be less than ±0.4 μA × 402 Ω = ±160 μV at 25°C.

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Thermal Analysis

The OPA820 will not require heatsinking or airflow in most applications. Maximum desired junction temperature would set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 210°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (PD) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. PDL will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_{S2}/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

Board Layout

Achieving optimum performance with a high-frequency amplifier such as the OPA820 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a. **Minimize parasitic capacitance to any AC ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b. **Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1-µF decoupling capacitors.** At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c. **Careful selection and placement of external components will preserve the high-frequency performance of the OPA820.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 1.5 kΩ, this parasitic capacitance can add a pole and/or a zero below 500 MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load-driving considerations. It has been suggested here that a good starting point for design would be to set $R_G||R_F = 200$ Ω. Using this setting will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance.

d. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5 pF) may not need an R_S since the OPA820 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on

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board material and trace dimensions, a matching series resistor into the trace from the output of the OPA820 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e. **Socketing a high-speed part like the OPA820 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA820 onto the board.

Input and ESD Protection

The OPA820 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 13.

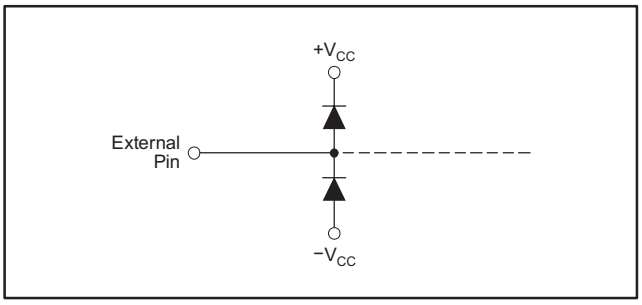

Figure 13. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (for example, in systems with ±15-V supply parts driving into the OPA820), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Figure 14 shows an example protection circuit for I/O voltages that may exceed the supplies.

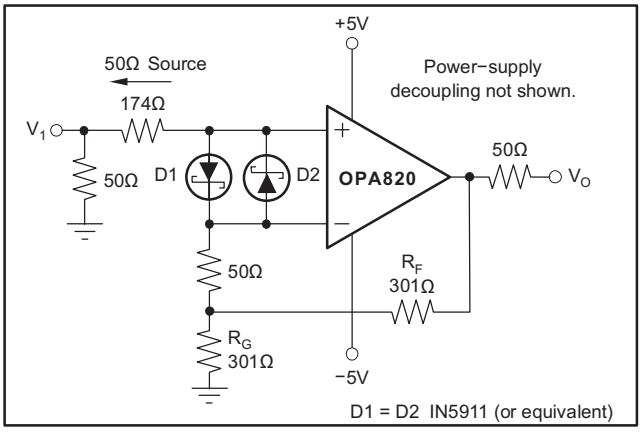

Figure 14. Gain of +2 With Input Protection

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA820SKGD3	ACTIVE	XCEPT	KGD	0	400	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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