

REF2125 具有干净启动功能的低漂移、低功耗、小型串联电压基准

1 特性

- 初始精度: $\pm 0.05\%$ (最大值)
- 温度系数: $6\text{ppm}/^\circ\text{C}$ (最大值)
- 运行温度范围: -40°C 至 $+125^\circ\text{C}$
- 输出电流: $\pm 10\text{mA}$
- 低静态电流: $95\mu\text{A}$ (最大值)
- 宽输入电压: 12V
- 输出 $1/f$ 噪声 (0.1Hz 至 10Hz): $5\mu\text{V}_{\text{pp}}/\text{V}$
- 出色的长期稳定性 ($30\text{ppm}/1000$ 小时)
- 小型 5 引脚 SOT-23 封装

2 应用

- 精密数据采集系统
- 电源监控
- PLC 模拟 I/O 模块
- 工业仪表
- 场发射器
- 测试设备
- 4 - 20mA 环路传感器
- LCR 表

3 说明

REF2125 器件是低温度漂移($6\text{ppm}/^\circ\text{C}$)、低功耗、高精度 CMOS 电压基准, 具有 $\pm 0.05\%$ 初始精度、低运行电流以及小于 $95\mu\text{A}$ 的功耗。该器件还提供 $5\mu\text{V}_{\text{p-p}}/\text{V}$ 的极低输出噪声, 这使得它在用于高分辨率数据转换器和噪声关键应用时能够保持高度的信号完整性。

该器件的低输出电压迟滞和低长期输出电压漂移进一步提高了稳定性和系统可靠性。此外, 器件的小尺寸和低运行电流 ($95\mu\text{A}$) 使其非常适合便携式和电池供电的应用。

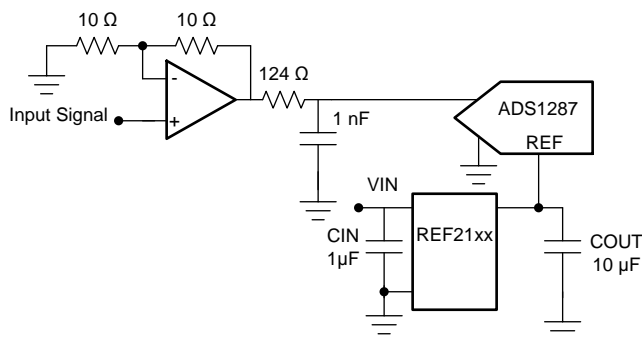
REF2125 具有宽额定温度范围 (-40°C 至 $+125^\circ\text{C}$)。有关其他电压选项, 请联系 TI 销售代表。

器件信息(1)

部件名称	封装	封装尺寸 (标称值)
REF2125	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

简化电路原理图



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目录

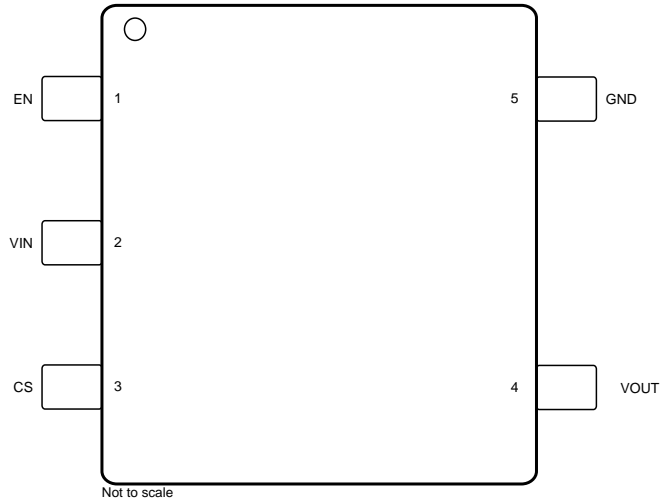
1	特性	1	8.1	Overview	15
2	应用	1	8.2	Functional Block Diagram	15
3	说明	1	8.3	Feature Description	15
4	修订历史记录	2	8.4	Device Functional Modes	16
5	Pin Configuration and Functions	3	9	Applications and Implementation	18
6	Specifications	4	9.1	Application Information	18
6.1	Absolute Maximum Ratings	4	9.2	Typical Application: Basic Voltage Reference Connection	18
6.2	ESD Ratings	4	10	Power-Supply Recommendations	19
6.3	Recommended Operating Conditions	4	11	Layout	20
6.4	Thermal Information	4	11.1	Layout Guidelines	20
6.5	Electrical Characteristics	5	11.2	Layout Example	20
6.6	Typical Characteristics	7	12	器件和文档支持	21
7	Parameter Measurement Information	11	12.1	文档支持	21
7.1	Solder Heat Shift	11	12.2	接收文档更新通知	21
7.2	Long-Term Stability	12	12.3	社区资源	21
7.3	Thermal Hysteresis	12	12.4	商标	21
7.4	Power Dissipation	13	12.5	静电放电警告	21
7.5	Noise Performance	14	12.6	Glossary	21
8	Detailed Description	15	13	机械、封装和可订购信息	21

4 修订历史记录

日期	修订版本	说明
2017 年 9 月	*	初始发行版

5 Pin Configuration and Functions

**DBV Package
5-Pin SOT-23
Top View**



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	EN	Input	Enable connection. Enables or disables the device.
2	VIN	Power	Input supply voltage connection.
3	CS	Input	Clean start pin. Connect to a resistor or capacitor to enable the clean start feature.
4	VOUT	Output	Reference voltage output.
5	GND	Ground	Ground connection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	IN	$V_{REF} + 0.05$	13	V
	EN	-0.3	IN + 0.3	
Output voltage	V_{REF}	-0.3	5.5	V
Output short circuit current			20	mA
Temperature	Operating, T_A	-55	150	°C
	Storage T_{stg}	-65	170	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Supply input voltage ($I_L = 0$ mA, $T_A = 25^\circ\text{C}$)	$V_{REF} + V_{DO}$ ⁽¹⁾		12	V
EN	Enable voltage	0		IN	V
I_L	Output current	-10		10	mA
T_A	Operating temperature	-40	25	125	°C

- (1) Dropout voltage.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF2125	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

At $T_A = 25^\circ\text{C}$ unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT						
	Output voltage accuracy	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	-0.05%		0.05%	
	Output voltage temperature coefficient ⁽¹⁾		2.5		6	ppm/ $^\circ\text{C}$
LINE AND LOAD REGULATION						
$\Delta V_{(O\Delta VIN)}$	Line regulation	$V_{IN} = 2.55\text{ V to }12\text{ V}, T_A = 25^\circ\text{C}$		2		ppm/V
		$V_{IN} = V_{REF} + V_{DO}^{(2)} \text{ to } 12\text{ V}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			15	
$\Delta V_{(O\Delta IL)}$	Load regulation	$I_L = 0\text{ mA to }10\text{ mA}, V_{IN} = 3\text{ V}, T_A = 25^\circ\text{C}$	Sourcing	20		ppm/mA
		$I_L = 0\text{ mA to }10\text{ mA}, V_{IN} = 3\text{ V}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	Sourcing		30	
		$I_L = 0\text{ mA to }-10\text{ mA}, V_{IN} = V_{REF} + V_{DO}^{(2)}, T_A = 25^\circ\text{C}$	Sinking	40		
		$I_L = 0\text{ mA to }-10\text{ mA}, V_{IN} = V_{REF} + V_{DO}^{(2)}, -40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	Sinking		70	
I_{SC}	Short-circuit current ⁽³⁾	$V_{REF} = 0, C_{CS} = \text{No connect}, T_A = 25^\circ\text{C}$		18		mA
		$R_{CS} = 500\text{ k}\Omega, T_A = 25^\circ\text{C}$		7		mA
		$C_{CS} = \text{GND}, T_A = 25^\circ\text{C}$		0.5		mA
NOISE						
e_n p-p	Output voltage noise ⁽⁴⁾	$f = 0.1\text{ Hz to }10\text{ Hz}$		5		$\mu\text{V p-p/V}$
		$f = 10\text{ Hz to }10\text{ kHz}$		24		$\mu\text{V rms}$
e_n	Output voltage noise density	$f = 1\text{ kHz}$		0.25		ppm/ $\sqrt{\text{Hz}}$
HYSTERESIS AND LONG TERM STABILITY						
	Long-term stability ⁽⁵⁾	1000 hours		30		ppm
	Output voltage hysteresis ⁽⁶⁾	$T_A = 25^\circ\text{C to }-40^\circ\text{C to }125^\circ\text{C to }25^\circ\text{C}, \text{ Cycle }1$		30		ppm
		$T_A = 25^\circ\text{C to }-40^\circ\text{C to }125^\circ\text{C to }25^\circ\text{C}, \text{ Cycle }2$		10		
TURNON						
t_{ON}	Turnon time	0.1% of output voltage settling, $C_L = 10\text{ }\mu\text{F}$, REF2125		2.5		ms
CAPACITIVE LOAD						
C_L	Stable output capacitor value	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.1	10	μF
OUTPUT VOLTAGE						
V_{REF}	Output voltage	REF2125		2.5		V

(1) Temperature drift is specified according to the box method. See [Feature Description](#) for more details.

(2) Dropout voltage under test condition is 100mV.

(3) In clean start section it is referred as I_{PEAK} .

(4) The peak-to-peak noise measurement procedure is explained in more detail in [Noise Performance](#).

(5) Long-term stability measurement procedure is explained in more in detail in [Long-Term Stability](#).

(6) The thermal hysteresis measurement procedure is explained in more detail in [Thermal Hysteresis](#).

Electrical Characteristics (continued)

 At $T_A = 25^\circ\text{C}$ unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{IN}	Input voltage			$V_{REF} + V_{DO}$		12	V
I_L	Output current capacity	$V_{IN} = V_{REF} + V_{DO}^{(2)}$ to 12 V	Sourcing	10			mA
		$V_{IN} = V_{REF} + V_{DO}^{(2)}$ to 12 V	Sinking	-10			
I_Q	Quiescent current	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	Active mode		72	95	μA
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	Shutdown mode		2.5	3	
V_{DO}	Dropout voltage	$I_L = 0\text{ mA}, T_A = 25^\circ\text{C}$			50		mV
		$I_L = 0\text{ mA}, -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				100	
		$I_L = 10\text{ mA}, -40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				500	
V_{EN}	ENABLE pin voltage	Voltage reference in active mode (EN = 1)		1.6			V
		Voltage reference in shutdown mode (EN = 0)				0.5	
I_{EN}	ENABLE pin leakage current	ENABLE = V_{IN} , $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			1	2	μA

6.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = 12\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\ \mu\text{F}$, $C_{IN} = 0.1\ \mu\text{F}$ (unless otherwise noted)

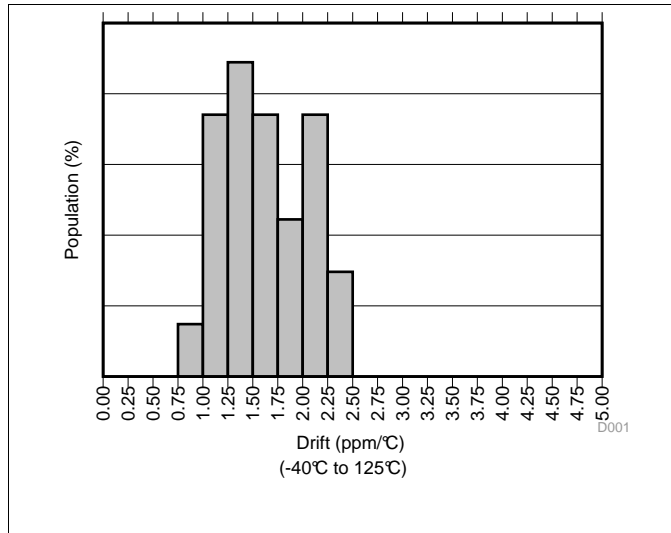


Figure 1. Temperature Drift

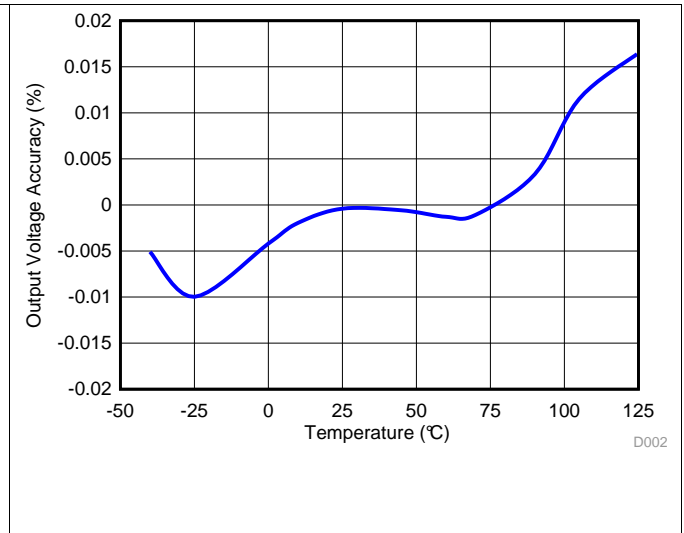


Figure 2. Output Voltage Accuracy vs Temperature

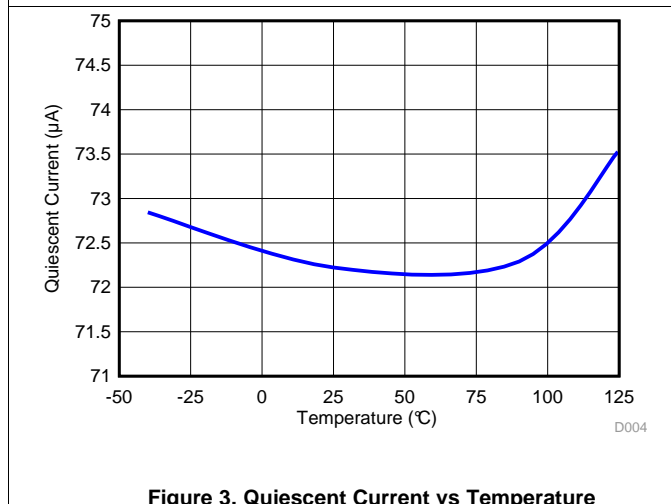


Figure 3. Quiescent Current vs Temperature

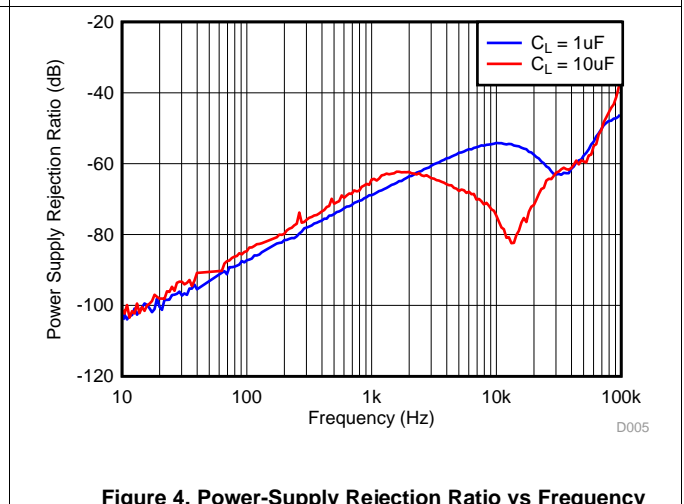


Figure 4. Power-Supply Rejection Ratio vs Frequency

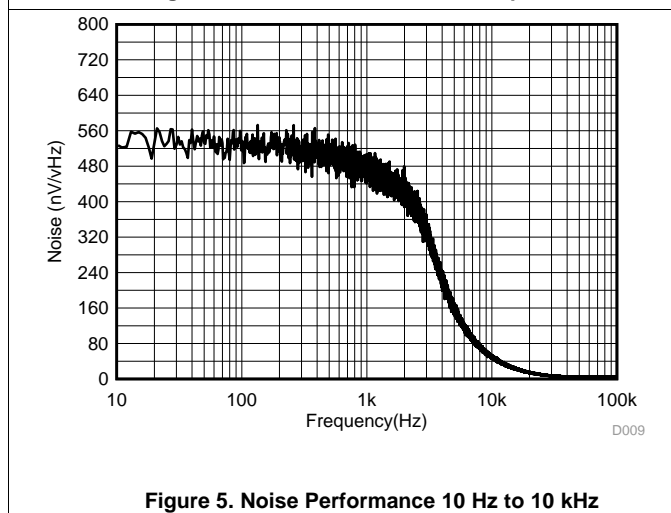


Figure 5. Noise Performance 10 Hz to 10 kHz

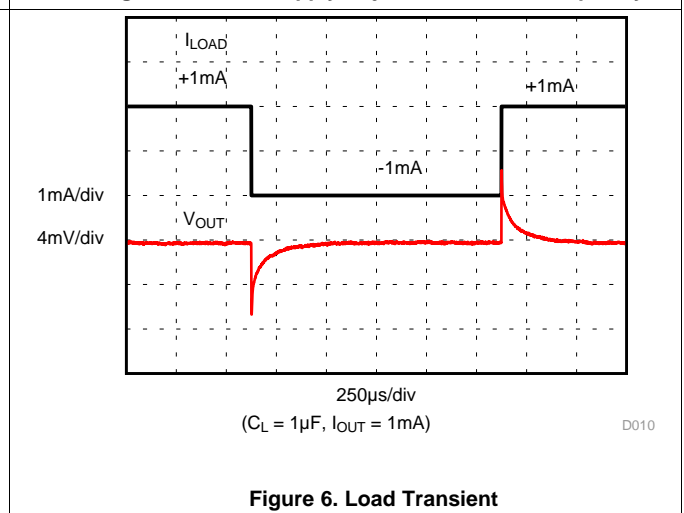
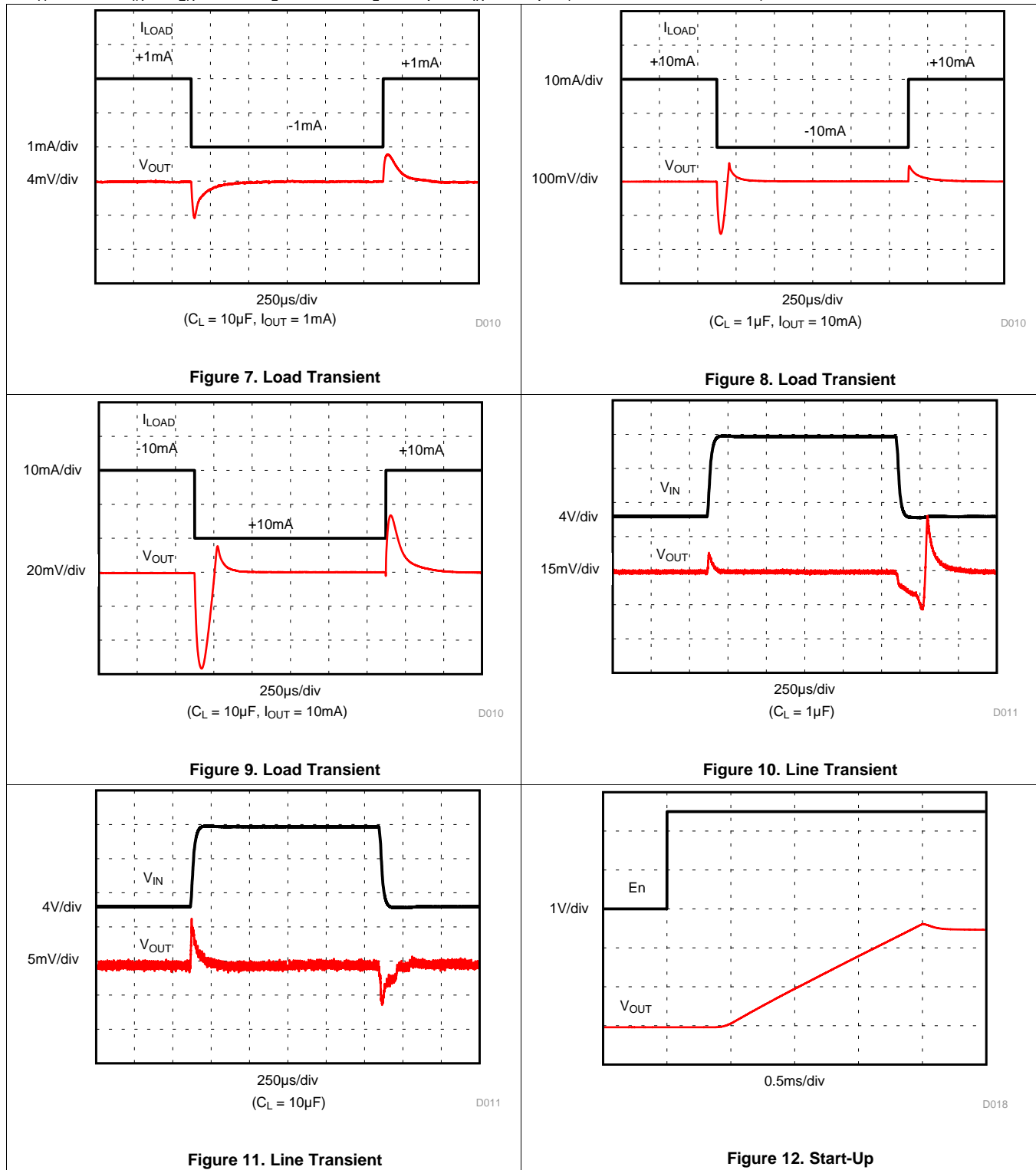


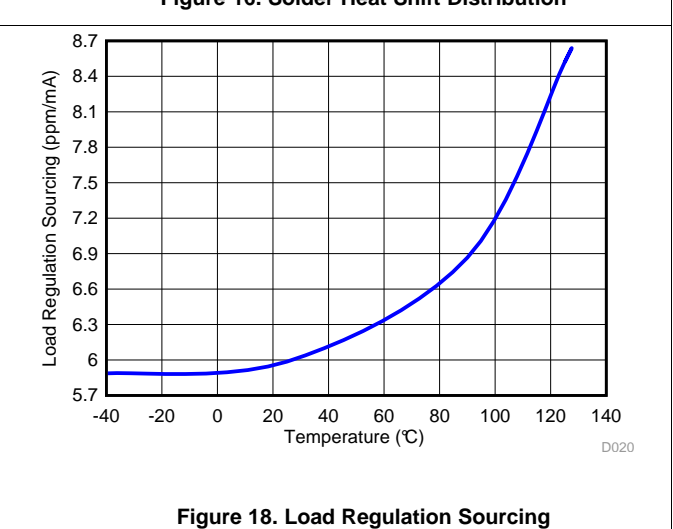
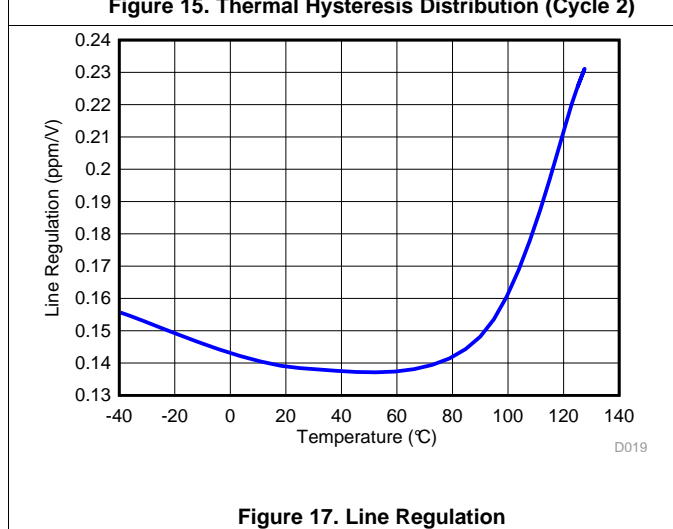
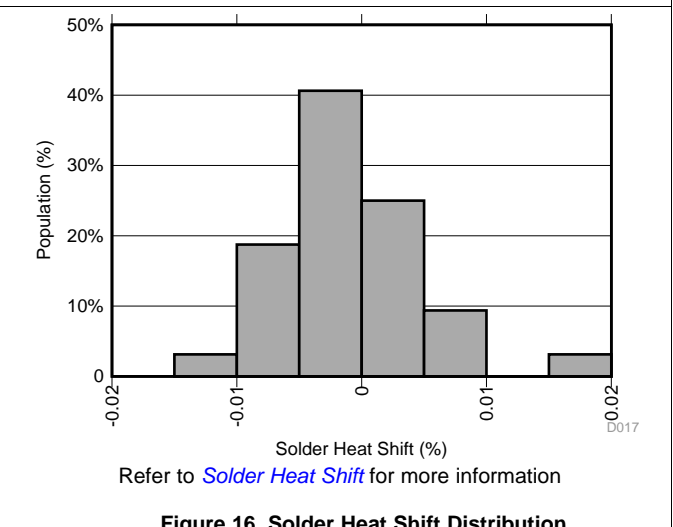
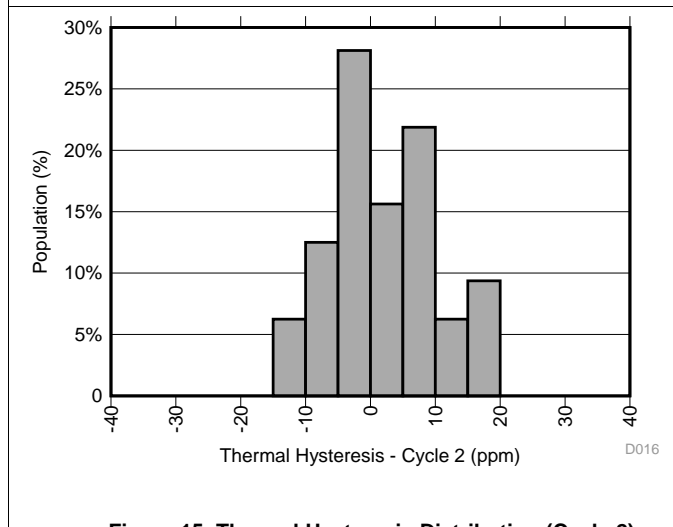
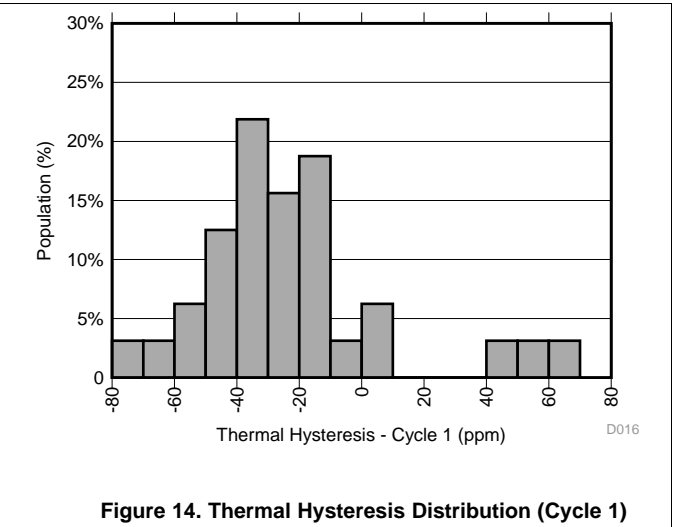
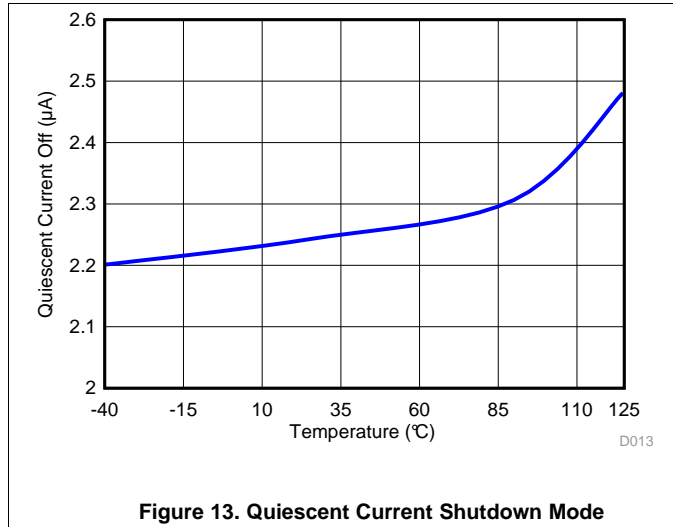
Figure 6. Load Transient

Typical Characteristics (continued)

 at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = 12\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\ \mu\text{F}$, $C_{IN} = 0.1\ \mu\text{F}$ (unless otherwise noted)


Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = 12\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\ \mu\text{F}$, $C_{IN} = 0.1\ \mu\text{F}$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{IN} = V_{EN} = 12\text{ V}$, $I_L = 0\text{ mA}$, $C_L = 10\ \mu\text{F}$, $C_{IN} = 0.1\ \mu\text{F}$ (unless otherwise noted)

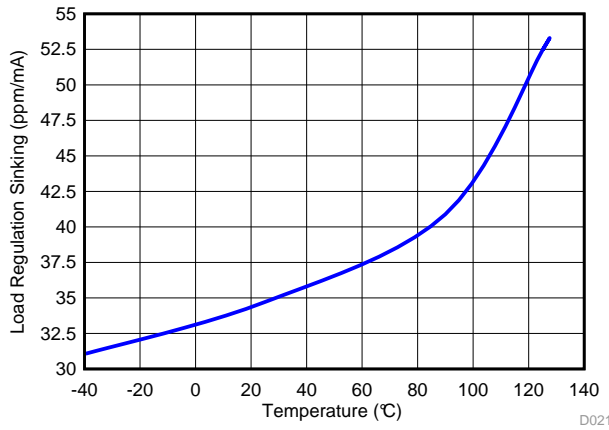


Figure 19. Load Regulation Sinking

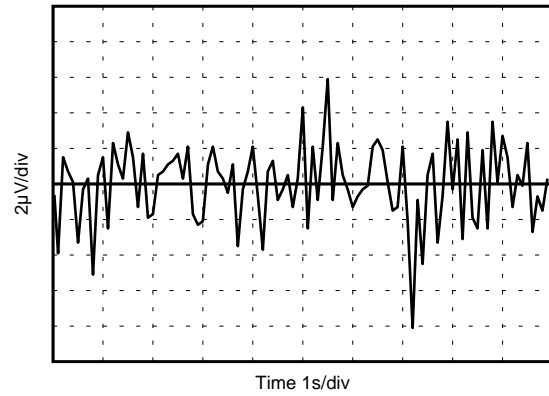


Figure 20. 0.1-Hz to 10-Hz Noise (V_{REF})

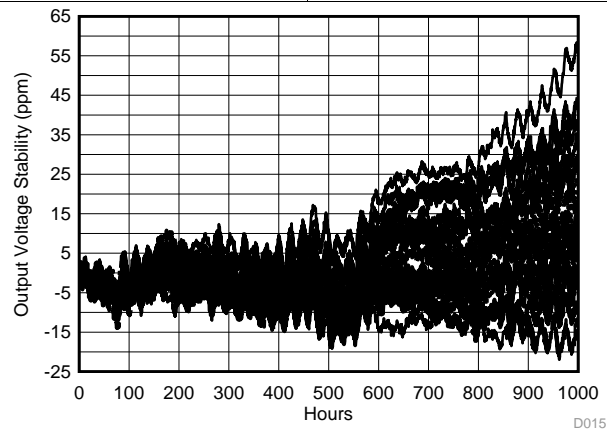


Figure 21. Long Term Stability - 1000 hours (V_{REF})

7 Parameter Measurement Information

7.1 Solder Heat Shift

The materials used in the manufacture of the REF2125 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on four printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 22. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm.

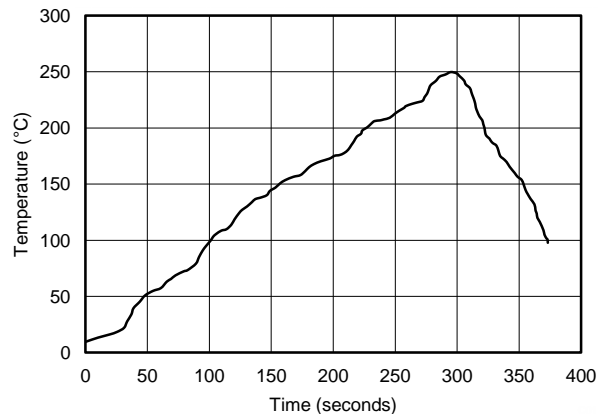


Figure 22. Reflow Profile

The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in Figure 23. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, solder the device in the second pass to minimize its exposure to thermal stress.

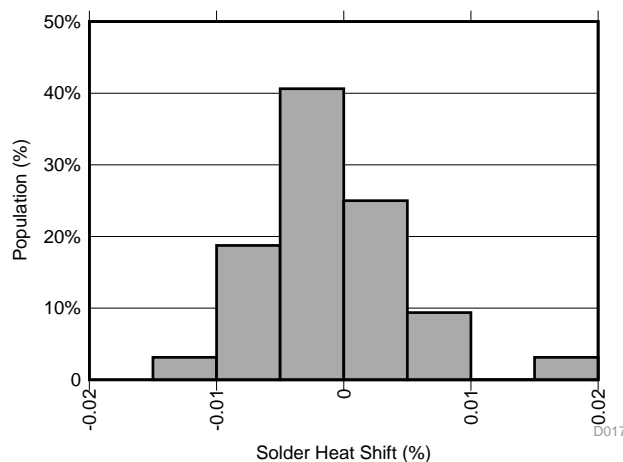


Figure 23. Solder Heat Shift Distribution, V_{REF} (%)

7.2 Long-Term Stability

One of the key parameters of the REF2125 reference is long-term stability. Typical characteristic expressed as curves shows the typical drift value for the REF2125 is 30 ppm from 0 to 1000 hours. This parameter is characterized by measuring 32 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 30 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time

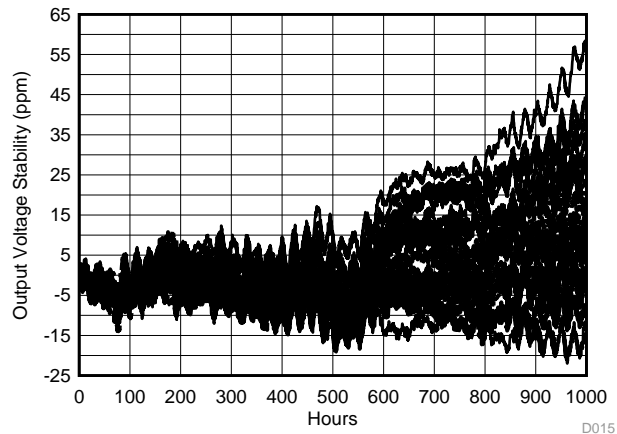


Figure 24. Long Term Stability - 1000 hours (V_{REF})

7.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF2125 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by Equation 1:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \times 10^6 \text{ (ppm)}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C. (1)

Typical thermal hysteresis distribution is as shown in [Figure 25](#).

Thermal Hysteresis (continued)

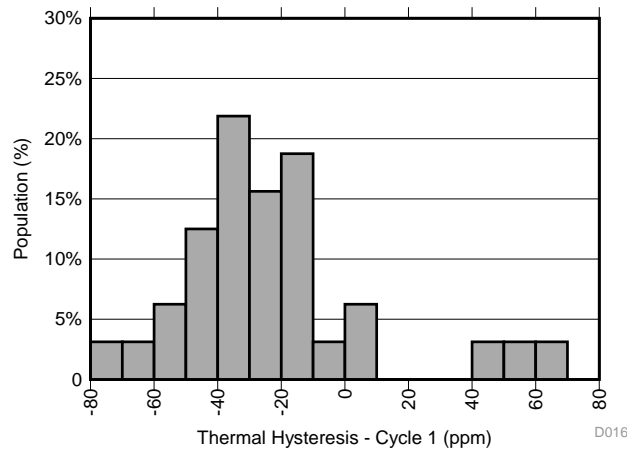


Figure 25. Thermal Hysteresis Distribution (V_{REF})

7.4 Power Dissipation

The REF2125 voltage reference is capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceed its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with [Equation 2](#):

$$T_J = T_A + P_D \times R_{\theta JA}$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- R_{θJA} is the package (junction-to-air) thermal resistance (2)

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the part be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

7.5 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in [Figure 26](#). Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in [Figure 26](#).

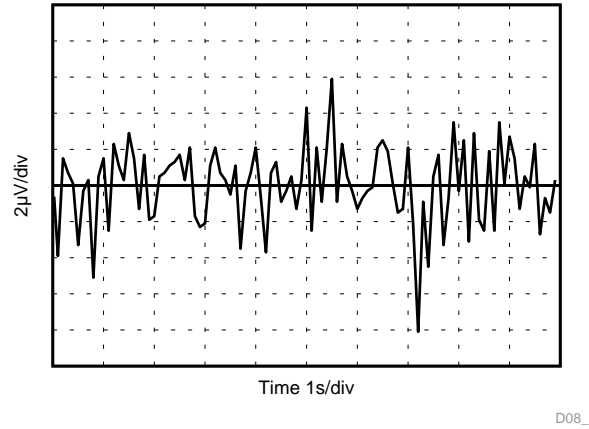


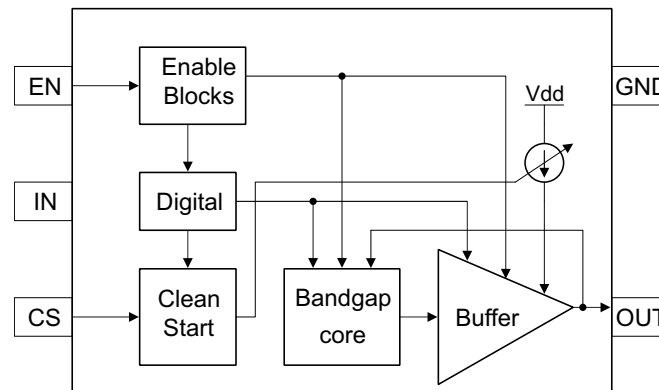
Figure 26. 0.1-Hz to 10-Hz Noise (V_{REF})

8 Detailed Description

8.1 Overview

The REF2125 is part of a family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The [Functional Block Diagram](#) is a simplified block diagram of the REF2125 showing basic band-gap topology.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Supply Voltage

The REF2125 family of references features an extremely low dropout voltage. The REF2125 can be operated with a supply of only 1 mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The REF2125 features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 72 μA , and the maximum quiescent current over temperature is just 95 μA . Supply voltages below the specified levels can cause the REF2125 to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

8.3.2 Low Temperature Drift

The REF2125 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by [Equation 3](#):

$$\text{Drift} = \left(\frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \times \text{Temperature Range}} \right) \times 10^6 \quad (3)$$

8.3.3 Load Current

The REF2125 family is specified to deliver a current load of ± 10 mA per output. The V_{REF} output of the device are protected from short circuits by limiting the output short-circuit current to 18 mA. The device temperature increases according to [Equation 4](#):

$$T_J = T_A + P_D \times R_{\theta JA}$$

where

- T_J = junction temperature ($^{\circ}\text{C}$),
 - T_A = ambient temperature ($^{\circ}\text{C}$),
 - P_D = power dissipated (W), and
 - $R_{\theta JA}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)
- (4)

The REF2125 maximum junction temperature must not exceed the absolute maximum rating of 150 $^{\circ}\text{C}$.

Feature Description (continued)

8.3.4 Clean Start Feature

In many applications (for example, loop powered applications), the supply at VIN has inductive impedance. This can cause the supply to dip during start-up because of the large output capacitor connected to the voltage reference and the inductive supply. The REF2125 family has an internal clean start block to control the peak of the inrush current during start-up. This feature is illustrated in [Functional Block Diagram](#). The peak of inrush current can be calculated as [Equation 5](#):

$$I_{PEAK} \approx 466\mu A + 13.54\mu A \times R_{CS}$$

where

- I_{PEAK} = Peak of inrush current (μA), has a range of [0.5 mA, 19 mA],
- R_{CS} = External resistor connected to the CS pin (5)

During power up, I_{PEAK} is split between the device current and output current. The output current (I_{OUT}) is split between output capacitor and load current (I_{LOAD}). The device current can be estimated to be $I_Q + I_{OUT}/183$, where I_Q is quiescent current at no load. Hence for a given I_{LOAD} it is important to choose R_{CS} such that I_{PEAK} is larger than I_{LOAD} . Above equations capture typical characteristics and hence it is suggested to include $\pm 25\%$ margins while budgeting for inrush current and also while choosing R_{CS} for a given I_{LOAD} . This inrush current continues to stay at the limiting value (I_{PEAK}) till output reaches close to V_{REF} (2.5 V).

When a C_{CS} is also connected in parallel to R_{CS} , The inrush current limit shall rise exponentially to the steady state value (I_{PEAK}) as calculated using above equations, with a time constant of $R_{CS} \times C_{CS}$. Hence the initial (and maximum) rate of rise of inrush current shall be $I_{PEAK} / (R_{CS} \times C_{CS})$. Because the inrush current rate is limited, the loop powered supply dip is controlled.

8.4 Device Functional Modes

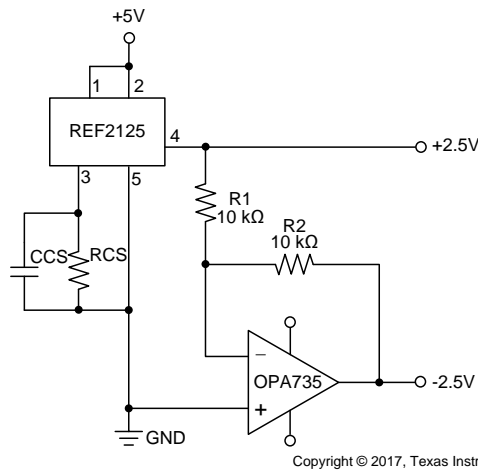
8.4.1 EN Pin

When the ENABLE pin of the REF2125 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF2125 can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 2 μA in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the [Thermal Information](#) for logic high and logic low voltage levels.

8.4.2 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF2125 and OPA735 can be used to provide a dual-supply reference from a 5-V supply. [Figure 27](#) shows the REF2125 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF2125 complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

Device Functional Modes (continued)



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Figure 27. REF2125 and OPA735 Create Positive and Negative Reference Voltages

9 Applications and Implementation

NOTE

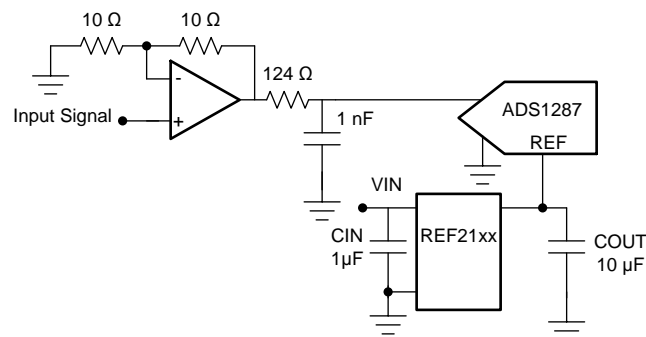
Information in the following applications and setups sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail. Basic applications includes positive/negative voltage reference and data acquisition systems. For more information see application sections in the REF32xx data sheet.

9.2 Typical Application: Basic Voltage Reference Connection

The circuit shown in [Figure 28](#) shows the basic configuration for the REF2125 references. Connect bypass capacitors according to the guidelines in [Input and Output Capacitors](#).



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Figure 28. Basic Reference Connection

9.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5 V
Output voltage V_{OUT}	2.5 V
REF2125 input capacitor	1 μ F
REF2125 output capacitor	10 μ F

9.2.2 Detailed Design Procedure

9.2.2.1 Input and Output Capacitors

A 1- μ F to 10- μ F electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1- μ F ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least 0.1 μ F must be connected to the output to improve stability and help filter out high frequency noise. An additional 1- μ F to 10- μ F electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the turnon time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1- μF ceramic capacitor in parallel to reduce overall ESR on the output.

9.2.2.2 V_{IN} Slew Rate Considerations

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

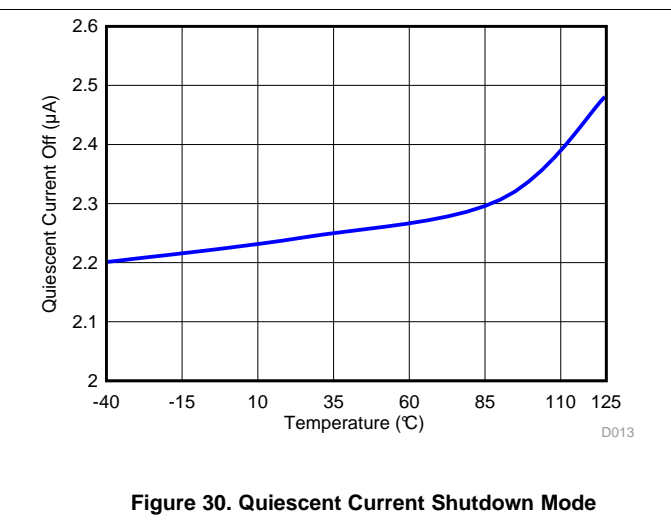
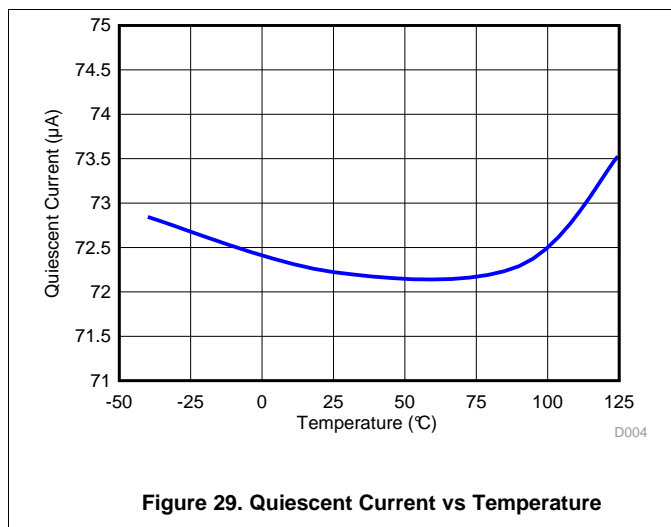
To avoid such conditions, ensure that the input voltage wave-form has both a rising and falling slew rate close to 6 V/ms.

9.2.2.3 Shutdown/Enable Feature

The REF2125 references can be switched to a low power shut-down mode when a voltage of 0.5 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 1.6 V or higher. During shutdown, the supply current drops to less than 2 μA , useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.5 V and 1.6 V because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly. If not using the shutdown feature, however, the ENABLE pin can simply be tied to the IN pin, and the reference remains operational continuously.

9.2.3 Application Curves



10 Power-Supply Recommendations

The REF2125 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. TI recommends a supply bypass capacitor ranging between 0.1 μF to 10 μF .

11 Layout

11.1 Layout Guidelines

Figure 31 illustrates an example of a PCB layout for a data acquisition system using the REF2125. Some key considerations are:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors at V_{IN} , V_{REF} of the REF2125.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

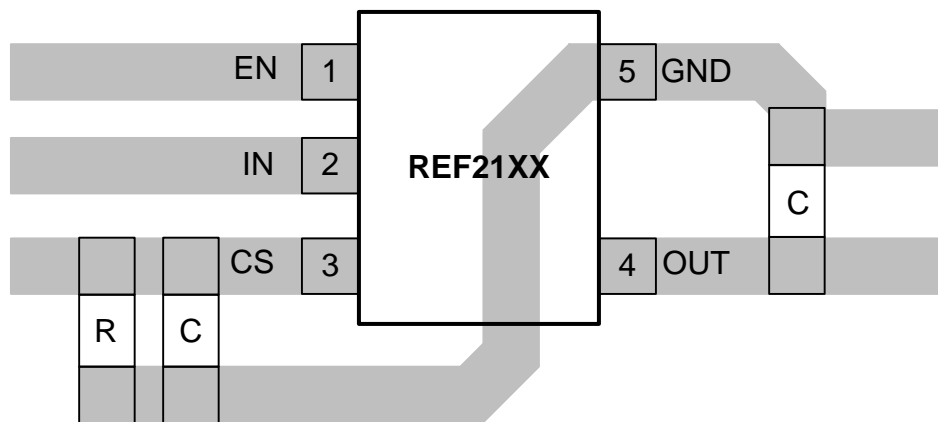


Figure 31. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档:

- 《INA21x 电压输出、低侧或高侧测量、双向、零漂移系列分流监控器》
- 《低漂移双向单电源低侧电流感应参考设计》

12.2 接收文档更新通知

要接收文档更新通知, 请导航至 TI.com 上的器件产品文件夹。单击右上角的通知我 进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

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ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据如有变更, 恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本, 请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2125IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19DD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2125IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2125IDBVR	SOT-23	DBV	5	3000	445.0	220.0	345.0

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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