SN54BCT2240 . . . J OR W PACKAGE

SCBS030E - SEPTEMBER 1988 - REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

description/ordering information

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN74BCT2241 and the 'BCT2244 devices, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (OE) inputs, and complementary OE and OE inputs. These devices feature high fan-out and improved fan-in.

The 'BCT2240 devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC}

through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The outputs, which are designed to source or sink up to 12 mA, include $33-\Omega$ series resistors to reduce overshoot and undershoot.

T _A	PACKA	GE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP – N		SN74BCT2240N	SN74BCT2240N	
0°C to 70°C		Tube	SN74BCT2240DW	DOTOGIO	
	SOIC – DW	Tape and reel	SN74BCT2240DWR	BCT2240	
	SOP – NS	Tape and reel	SN74BCT2240NSR	BCT2240	
	SSOP – DB	Tape and reel	SN74BCT2240DBR	BA240	
	CDIP – J	Tube	SNJ54BCT2240J	SNJ54BCT2240J	
–55°C to 125°C	CFP – W	Tube	SNJ54BCT2240W	SNJ54BCT2240W	
	LCCC – FK	Tube	SNJ54BCT2240FK	SNJ54BCT2240FK	

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74BCT2240DB, DW, N,OR NS PACKAGE (TOP VIEW)										
		<u> </u>								
1 <u>0</u> [$_{1}$ U	20] v _{cc}							
1A1 [2	19	20E							
2Y4 [3	18] 1Y1							
1A2 🛛	4	17] 2A4							
2Y3	5	16] 1Y2							
1A3 [6	15] 2A3							
2Y2	7	14] 1Y3							
1A4 [8	13] 2A2							
2Y1	9	12] 1Y4							
GND [10	11] 2A1							

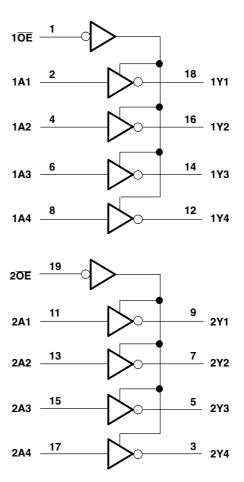
SN54BCT2240 ... FK PACKAGE (TOP VIEW)

	274 10E 20E 20E	
1A2 2Y3 1A3 2Y2 1A4	3 2 1 20 19 4 1 5 1 6 1 7 1 8 1 1 20 19 1 20 1 20 1	8 1Y1 7 2A4 6 1Y2 5 2A3 4 1Y3
	2Y1 GND 2A1 1Y4 2A2	

SCBS030E - SEPTEMBER 1988 - REVISED MARCH 2003

FUNCTION TABLE (each buffer)									
INPU	JTS	OUTPUT							
ŌĒ	Α	Y							
L	Н	L							
L	L	н							
Н	Х	Z							

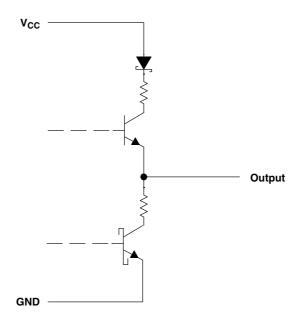
logic diagram (positive logic)





SCBS030E - SEPTEMBER 1988 - REVISED MARCH 2003

schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		
Voltage range applied to any output in the disat		
Voltage range applied to any output in the high		
Input clamp current, I _{IK}		–30 mA
Current into any output in the low state		24 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	
	DW package	58°C/W
	N package	
	NS package	60°C/W
Storage temperature range, T _{stg}		

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



SCBS030E - SEPTEMBER 1988 - REVISED MARCH 2003

recommended operating conditions (see Note 3)

		SN	I54BCT2240 SN74BCT2240			240		
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current			-12			-12	mA
I _{OL}	Low-level output current			12			12	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED		SN	54BCT22	240	SN7				
PARAMETER	TE	MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
V _{IK}	$V_{CC} = 4.5 V,$	l _l = -18 mA			-1.2			-1.2	V
N.		I _{OH} = -1 mA	2.4	3.3		2.4	3.3		v
V _{OH}	$V_{CC} = 4.5 V$	I _{OH} = -12 mA	2	3.2		2	3.2		v
N.		I _{OL} = 1 mA		0.15	0.5		0.15	0.5	v
V _{OL}	$V_{CC} = 4.5 V$	I _{OL} = 12 mA		0.35	0.8		0.35	0.8	v
lı	$V_{CC} = 5.5 V,$	V _I = 7 V			0.1			0.1	mA
I _{IH}	$V_{CC} = 5.5 V,$	V _I = 2.7 V			20			20	μA
Ι _{ΙL}	$V_{CC} = 5.5 V,$	V _I = 0.5 V			-1			-1	mA
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V			50			50	μA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.5 V			-50			-50	μA
I _{OS} ‡	V _{CC} = 5.5 V,	V _O = 0	-100		-225	-100		-225	mA
ICCH	V _{CC} = 5.5 V,	Outputs open		19	32		19	32	mA
I _{CCL}	V _{CC} = 5.5 V,	Outputs open		46	76		46	76	mA
I _{CCZ}	V _{CC} = 5.5 V,	Outputs open		6	8		6	8	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

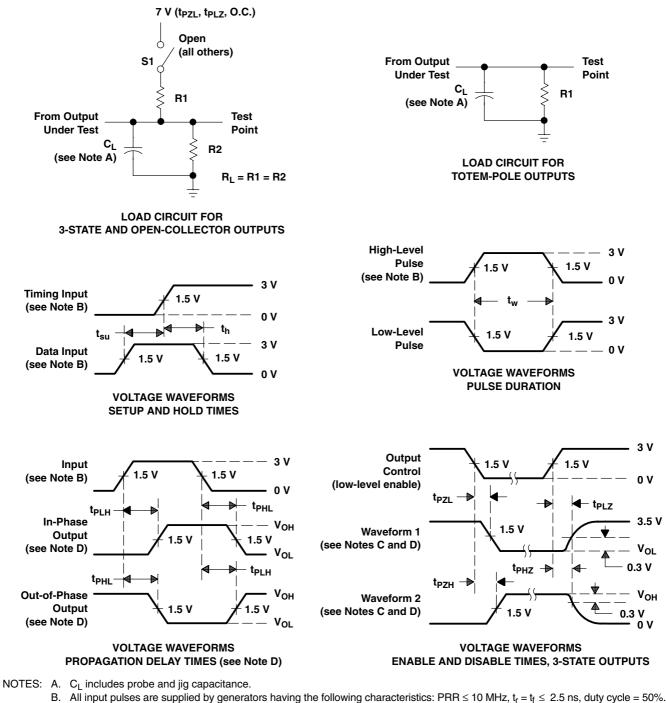
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER FROM		TO	V _{CC} = 5 V, T _A = 25°C			SN54BC	CT2240	SN74BC	UNIT	
	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}		v	0.5	3.4	4.8	0.5	6.3	0.5	5.7	
t _{PHL}	A	Ŷ	0.5	2.8	4	0.5	4.6	0.5	4.4	ns
t _{PZH}		v	2.6	6.2	8.2	2.6	10.1	2.6	9.3	
t _{PZL}	ŌĒ	Y	4.3	8.8	10.9	4.3	12.9	4.3	12.4	ns
t _{PHZ}	ŌĒ	v	2	5.3	7.1	2	9.2	2	8.7	
t _{PLZ}	OE	Y	2.2	6.7	8.5	2.2	12.2	2.2	10.6	ns



SCBS030E - SEPTEMBER 1988 - REVISED MARCH 2003

PARAMETER MEASUREMENT INFORMATION



- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MR2, t_r = t_f ≤ 2.5 ns, duty cycle = 50%
 Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.
- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9093901M2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9093901M2A SNJ54BCT 2240FK	Samples
5962-9093901MRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9093901MR A SNJ54BCT2240J	Samples
SNJ54BCT2240FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9093901M2A SNJ54BCT 2240FK	Samples
SNJ54BCT2240J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9093901MR A SNJ54BCT2240J	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	Τ (μm)	B (mm)
5962-9093901M2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54BCT2240FK	FK	LCCC	20	1	506.98	12.06	2030	NA

J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



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