- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**
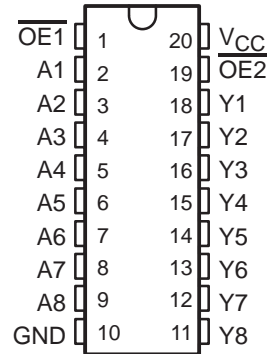
### description

The ′F541 octal buffer/line driver is ideal for driving bus lines or buffering memory address registers. The device features inputs and outputs on opposite sides of the package to facilitate printed-circuit-board layout.
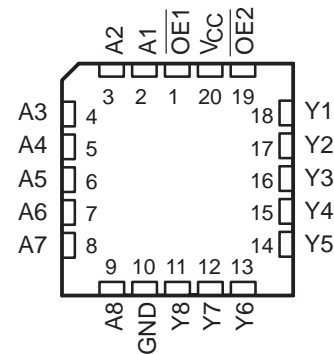
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state.

The SN54F541 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F251 is characterized for operation from 0°C to 70°C.

**SN54F541 . . . J PACKAGE**
**SN74F541 . . . DW OR N PACKAGE**
**(TOP VIEW)**

```
         _____
$\overline{OE1}$ [| 1      20 |] V_CC
   A1 [| 2      19 |] $\overline{OE2}$
   A2 [| 3      18 |] Y1
   A3 [| 4      17 |] Y2
   A4 [| 5      16 |] Y3
   A5 [| 6      15 |] Y4
   A6 [| 7      14 |] Y5
   A7 [| 8      13 |] Y6
   A8 [| 9      12 |] Y7
  GND [| 10     11 |] Y8
```

**SN54F541 . . . FK PACKAGE**
**(TOP VIEW)**

```
        A2  A1 OE1 Vcc OE2
         3   2   1  20  19
   A3 [| 4              18 |] Y1
   A4 [| 5              17 |] Y2
   A5 [| 6              16 |] Y3
   A6 [| 7              15 |] Y4
   A7 [| 8              14 |] Y5
         9  10  11  12  13
        A8 GND  Y8  Y7  Y6
```

**FUNCTION TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE1}$ | $\overline{OE2}$ | A | Y |
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

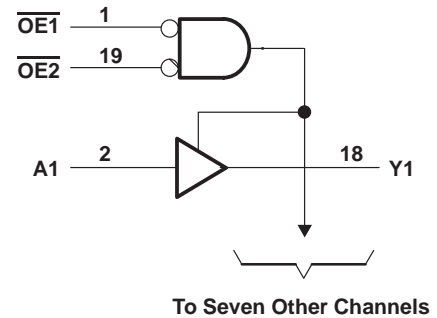Copyright © 1993, Texas Instruments Incorporated

**TEXAS INSTRUMENTS**

# SN54F541, SN74F541
# OCTAL BUFFERS/DRIVERS
# WITH 3-STATE OUTPUTS

SDFS021A – D3126, JANUARY 1989 – REVISED OCTOBER 1993

## logic symbol†



$\overline{OE1}$  1

$\overline{OE2}$  19

| & | EN |
|---|---|

A1  2 — 18  Y1
A2  3 — 17  Y2
A3  4 — 16  Y3
A4  5 — 15  Y4
A5  6 — 14  Y5
A6  7 — 13  Y6
A7  8 — 12  Y7
A8  9 — 11  Y8

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



$\overline{OE1}$  1

$\overline{OE2}$  19

A1  2 — 18  Y1

**To Seven Other Channels**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ ................................................................ −0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) ....................................................... −1.2 V to 7 V
Input current range ....................................................................... −30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state ................... −0.5 V to 5.5 V
Voltage range applied to any output in the high state ................................. −0.5 V to $V_{CC}$
Current into any output in the low state: SN54F541 ........................................... 96 mA
  SN74F541 ............................................ 128 mA
Operating free-air temperature range:  SN54F541 .................................... −55°C to 125°C
  SN74F541 .................................... 0°C to 70°C
Storage temperature range ................................................................ −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1:   The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

| | | SN54F541 | | | SN74F541 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{IK}$ | Input clamp current | | | −18 | | | −18 | mA |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | | 64 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54F541 | | | SN74F541 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | $V_{CC} = 4.5$ V, | $I_I = -18$ mA | | | -1.2 | | | -1.2 | V |
| $V_{OH}$ | $V_{CC} = 4.5$ V | $I_{OH} = -3$ mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| | | $I_{OH} = -12$ mA | 2 | 3.2 | | | | | |
| | | $I_{OH} = -15$ mA | | | | 2 | 3.1 | | |
| | $V_{CC} = 4.75$ V, | $I_{OH} = -3$ mA | | | | 2.7 | | | |
| $V_{OL}$ | $V_{CC} = 4.5$ V | $I_{OL} = 48$ mA | | 0.38 | 0.55 | | | | V |
| | | $I_{OL} = 64$ mA | | | | | 0.42 | 0.55 | |
| $I_{OZH}$ | $V_{CC} = 5.5$ V, | $V_O = 2.7$ V | | | 50 | | | 50 | μA |
| $I_{OZL}$ | $V_{CC} = 5.5$ V, | $V_O = 0.5$ V | | | -50 | | | -50 | μA |
| $I_I$ | $V_{CC} = 5.5$ V, | $V_I = 7$ V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC} = 5.5$ V, | $V_I = 2.7$ V | | | 20 | | | 20 | μA |
| $I_{IL}$ | $V_{CC} = 5.5$ V, | $V_I = 0.5$ V | | | -0.6 | | | -0.6 | mA |
| $I_{OS}$‡ | $V_{CC} = 5.5$ V, | $V_O = 0$ | -100 | | -225 | -100 | | -225 | mA |
| $I_{CC}$ | $V_{CC} = 5.5$ V | Outputs high | | 28 | 35 | | 28 | 35 | mA |
| | | Outputs low | | 62 | 75 | | 62 | 75 | |
| | | Outputs disabled | | 40 | 55 | | 40 | 55 | |

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $C_L = 50$ pF, $R_L = 500$ Ω, $T_A = 25°C$ | | | $V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_L = 500$ Ω, $T_A = $ MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 'F541 | | | SN54F541 | | SN74F541 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | Any A | Y | 1.5 | 3.3 | 5.5 | 1 | 6.5 | 1.5 | 6 | ns |
| $t_{PHL}$ | | | 1.5 | 2.7 | 5.5 | 1 | 6.5 | 1.5 | 6 | |
| $t_{PZH}$ | $\overline{OE}$ | Y | 3 | 5.8 | 8 | 1.7 | 10 | 2.5 | 9.5 | ns |
| $t_{PZL}$ | | | 3.5 | 6.1 | 8.5 | 2.2 | 10 | 3 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Y | 1.5 | 3.4 | 6 | 1 | 7 | 1.5 | 6.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 2.9 | 5.5 | 1 | 7.5 | 1.5 | 6 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2:   Load circuits and waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9175301M2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9175301M2A SNJ54F541FK | Samples |
| 5962-9175301MRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9175301MRA SNJ54F541J | Samples |
| SN74F541DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F541 | Samples |
| SN74F541DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F541 | Samples |
| SN74F541N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN74F541N | Samples |
| SN74F541NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74F541 | Samples |
| SNJ54F541FK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9175301M2A SNJ54F541FK | Samples |
| SNJ54F541J | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9175301MRA SNJ54F541J | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54F541, SN74F541 :**

- Catalog : SN74F541

- Military : SN54F541

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74F541DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74F541NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74F541DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74F541NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

## TUBE



T - Tube height

L - Tube length

W-Tube width

B - Alignment groove width

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9175301M2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SN74F541DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74F541N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54F541FK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |

FK (S—CQCC—N**)
28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.050 (1,27)

0.045 (1,14) / 0.035 (0,89)
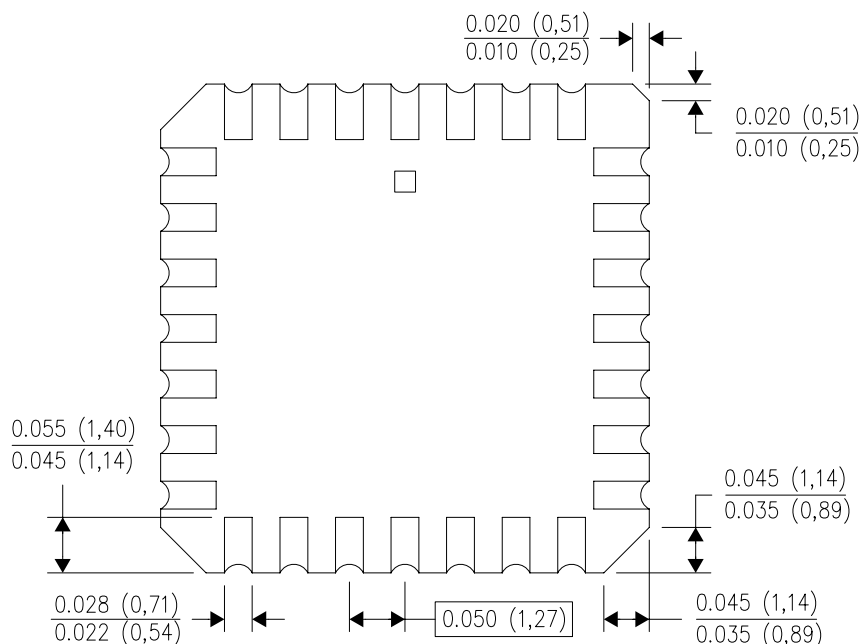
4040140/D 01/11

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  This package can be hermetically sealed with a metal lid.
        D.  Falls within JEDEC MS—004

## MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| PINS **<br>DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A    MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A    MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:   A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

| DIM PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14        8

1         7

$\frac{0.065 \ (1,65)}{0.045 \ (1,14)}$

C

0.005 (0,13) MIN

$\frac{0.060 \ (1,52)}{0.015 \ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°−15°

$\frac{0.026 \ (0,66)}{0.014 \ (0,36)}$

0.100 (2,54)

$\frac{0.014 \ (0,36)}{0.008 \ (0,20)}$

4040083/F 03/03

NOTES:    A.    All linear dimensions are in inches (millimeters).
          B.    This drawing is subject to change without notice.
          C.    This package is hermetically sealed with a ceramic lid using glass frit.
          D.    Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.    Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

## N (R−PDIP−T**)    PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A   MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A   MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | AA | BB | AC | AD |

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)  D

0.045 (1,14) / 0.030 (0,76)  D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option  D

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
        C.  Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        D.  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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SEATING PLANE

C

⌀ 0.1 C

10.63 / 9.97 TYP

PIN 1 ID AREA

A

1

18X 1.27

20

13.0 / 12.6 NOTE 3

2X 11.43

10

11

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

B

7.6 / 7.4 NOTE 4

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A    05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

1

SYMM

20X (0.6)

18X (1.27)

20

(R0.05)
TYP

SYMM

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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