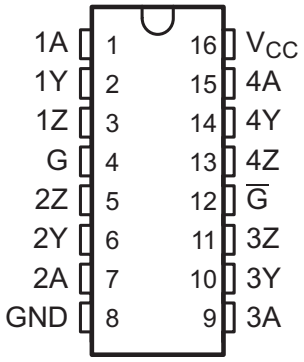
# 高速差分线路驱动器

查询样品: SN55LVDS31-SP

## 特性

- 符合 **QML-V，SMD 5962-97621**
- 符合或者超过 **ANSI TIA/EIA-644** 标准的要求
- 具有 **350mV** 的典型输出电压和 **100Ω** 负载的低压差分信号传输
- 典型输出电压上升和下降次数为 **500ps**（**400Mbps** 时）
- 典型传播延迟时间为 **1.7ns**
- 由一个单 **3.3V** 电源供电运行
- 每个驱动器在 **200MHz** 上的功率耗散典型值为 **25mW**
- 当被禁用或者 $V_{CC}$ **= 0** 时，驱动器处于高阻抗
- 总线-端子静电放电 **(ESD)** 保护超过 **8kV**
- 低压 **TTL(LVTTL)** 逻辑输入电平
- 针对有冗余需求的太空和高可靠性应用的冷备用

**J OR W PACKAGE**
**(TOP VIEW)**




## 说明

SN55LVDS31 是一款差分线路驱动器，此驱动器能够执行低压差分信号传输 (LVDS) 的电气特性。 这个信号传输技术降低了 5V 差分标准电平（例如 TIA/EIA-422B）的输出电压电平，从而减少了功耗、增加了开关速度、并可实现 3.3V 电源轨供电下的运行。 当被启用时，这个驱动器将传送一个大小为 247mV 的最小差分输出电压进入 100Ω 的负载。

此器件和信号传输技术用于接近 100Ω 的受控阻抗介质上的点到点和多支路（一个驱动器和多个接收器）的数据传输应用。此传输介质可以是印刷电路板走线、底板、或者电缆。 数据传输的最终速率和距离取决于介质的衰减特性和环境的噪声耦合。

SN55LVDS31 额定运行温度介于 -55°C 至 125°C 之间。

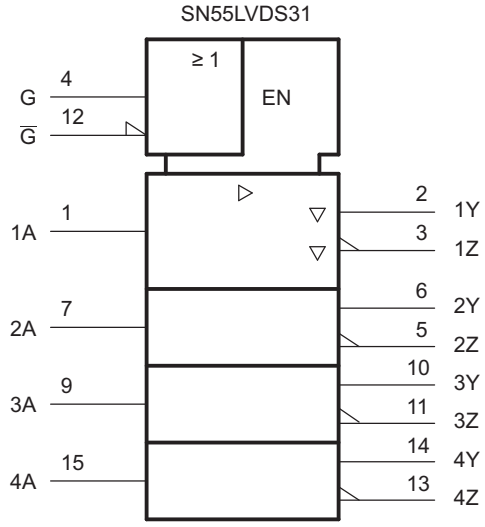
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| –55°C to 125°C | CDIP - J | 5962-9762101VEA | 5962-9762101VEA |
| | CFP - W | 5962-9762101VFA | 5962-9762101VFA |

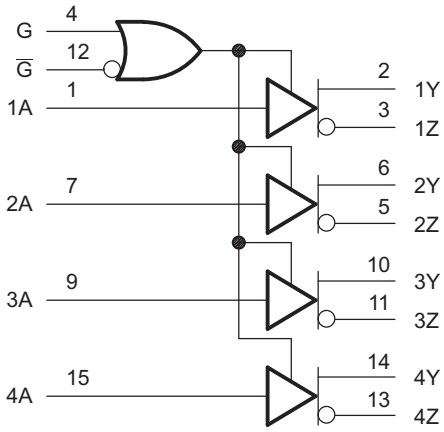
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### Logic Symbol




This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### SN55LVDS31 Logic Diagram (Positive Logic)



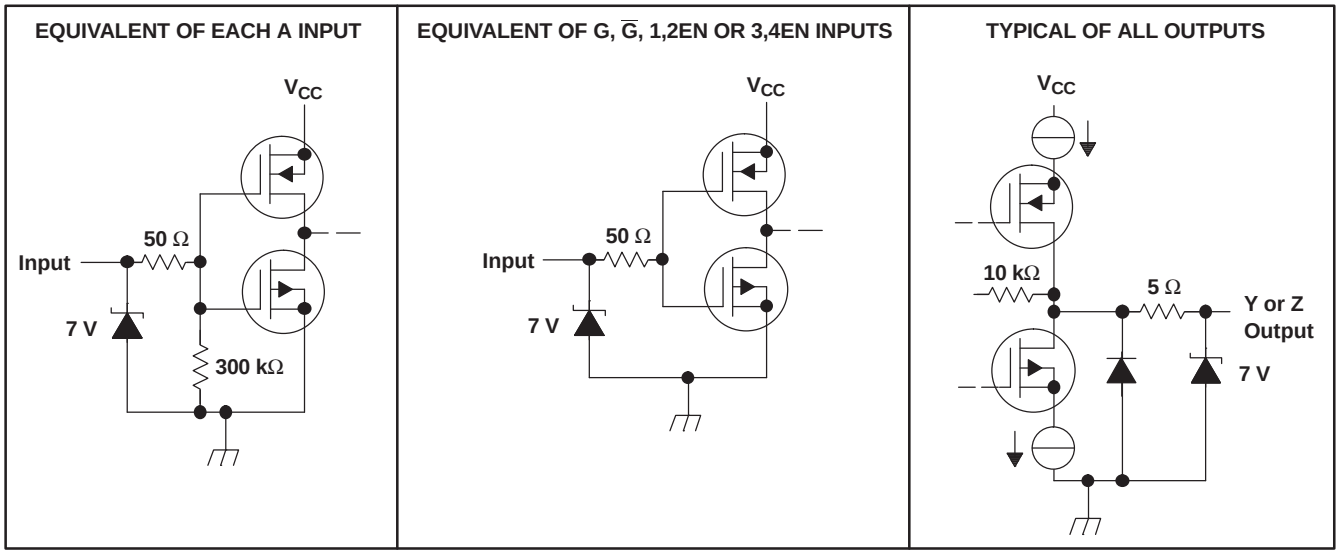
## FUNCTION TABLE

**Table 1. SN55LVDS31 (1)**

| INPUT A | ENABLES | | OUTPUTS | |
|---|---|---|---|---|
| | G | G | Y | Z |
| H | H | X | H | L |
| L | H | X | L | H |
| H | X | L | H | L |
| L | X | L | L | H |
| X | L | H | Z | Z |
| Open | H | X | L | H |
| Open | X | L | L | H |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | UNIT |
|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | –0.5 V to 4 V |
| $V_I$ | Input voltage range | –0.5 V to $V_{CC}$ + 0.5 V |
| | Continuous total power dissipation | See Dissipation Rating Table |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| $T_{stg}$ | Storage temperature range | –65°C to 150°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

## DISSIPATION RATING TABLE

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR(1) ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| J | 1375 mW | 11 mW/°C | 880 mW | 715 mW | 275 mW |
| W | 1000 mW | 8 mW/°C | 640 mW | 520 mW | 200 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $T_A$ | Operating free-air temperature | –55 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential output voltage magnitude | $R_L$ = 100 Ω, | See Figure 2 | 247 | 340 | 454 | mV |
| $\Delta V_{OD}$ | Change in differential output voltage magnitude between logic states | $R_L$ = 100 Ω, | See Figure 2 | –50 | | 50 | mV |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | See Figure 3 | | 1.125 | 1.2 | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states | See Figure 3 | | –50 | | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | See Figure 3 | | | 50 | | mV |
| $I_{CC}$ | Supply current | $V_I$ = 0.8 V or 2 V, | Enabled, No load | | 9 | 20 | mA |
| | | $V_I$ = 0.8 or 2 V, | $R_L$ = 100 Ω, Enabled | | 25 | 35 | |
| | | $V_I$ = 0 or $V_{CC}$, | Disabled | | 0.25 | 1 | |
| $I_{IH}$ | High-level input current | $V_{IH}$ = 2 | | | 4 | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0.8 V | | | 0.1 | 10 | µA |
| $I_{OS}$ | Short-circuit output current | $V_{O(Y)}$ or $V_{O(Z)}$ = 0 | | | –4 | –24 | mA |
| | | $V_{OD}$ = 0 | | | | ±12 | |
| $I_{OZ}$ | High-impedance output current | $V_O$ = 0 or 2.4 V | | | | ±1 | µA |
| $I_{O(OFF)}$ | Power-off output current | $V_{CC}$ = 0, | $V_O$ = 2.4 V | | | ±4 | µA |
| $C_i$ | Input capacitance | | | | 3 | | pF |

(1) All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3 V.

## SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $R_L$ = 100 Ω, $C_L$ = 10 pF, See Figure 2 | 0.5 | 1.4 | 4 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 1 | 1.7 | 4.5 | ns |
| $t_r$ | Differential output signal rise time (20% to 80%) | | 0.4 | 0.5 | 1 | ns |
| $t_f$ | Differential output signal fall time (80% to 20%) | | 0.4 | 0.5 | 1 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} - t_{PLH}\|$) | | | 0.3 | 0.6 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew(2) | | | 0.3 | 0.6 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | See Figure 4 | | 5.4 | 15 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | 2.5 | 15 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | | | 8.1 | 17 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | 7.3 | 15 | ns |

(1) All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3 V.
(2) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

## PARAMETER MEASUREMENT INFORMATION

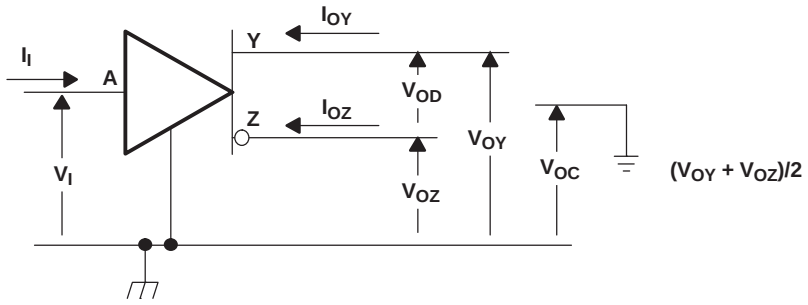
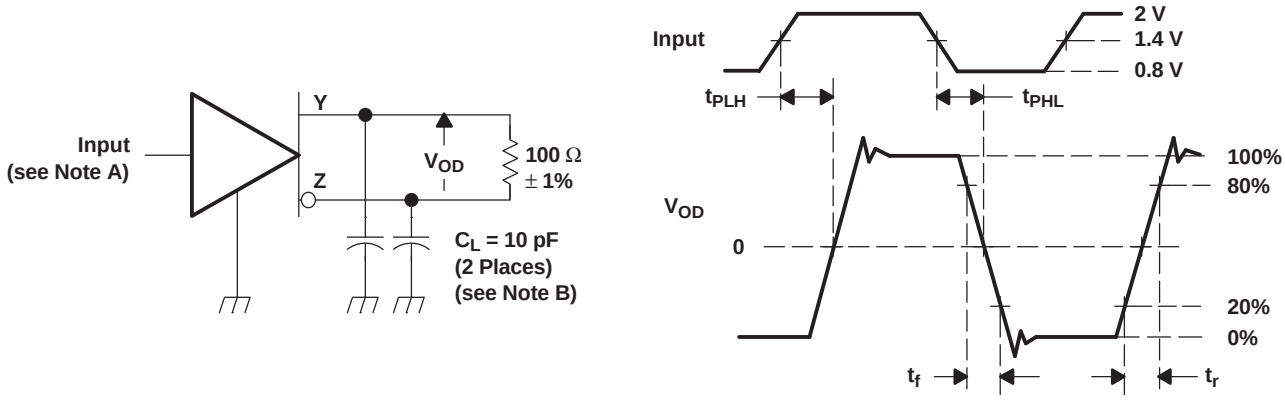


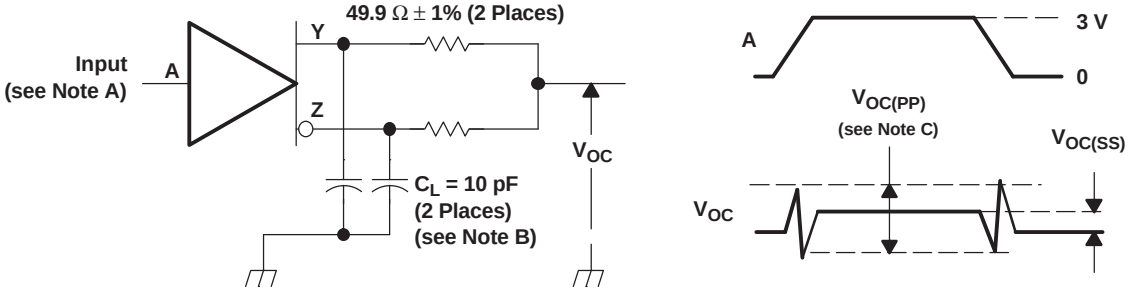

**Figure 1. Voltage and Current Definitions**




NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. $C_L$ includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

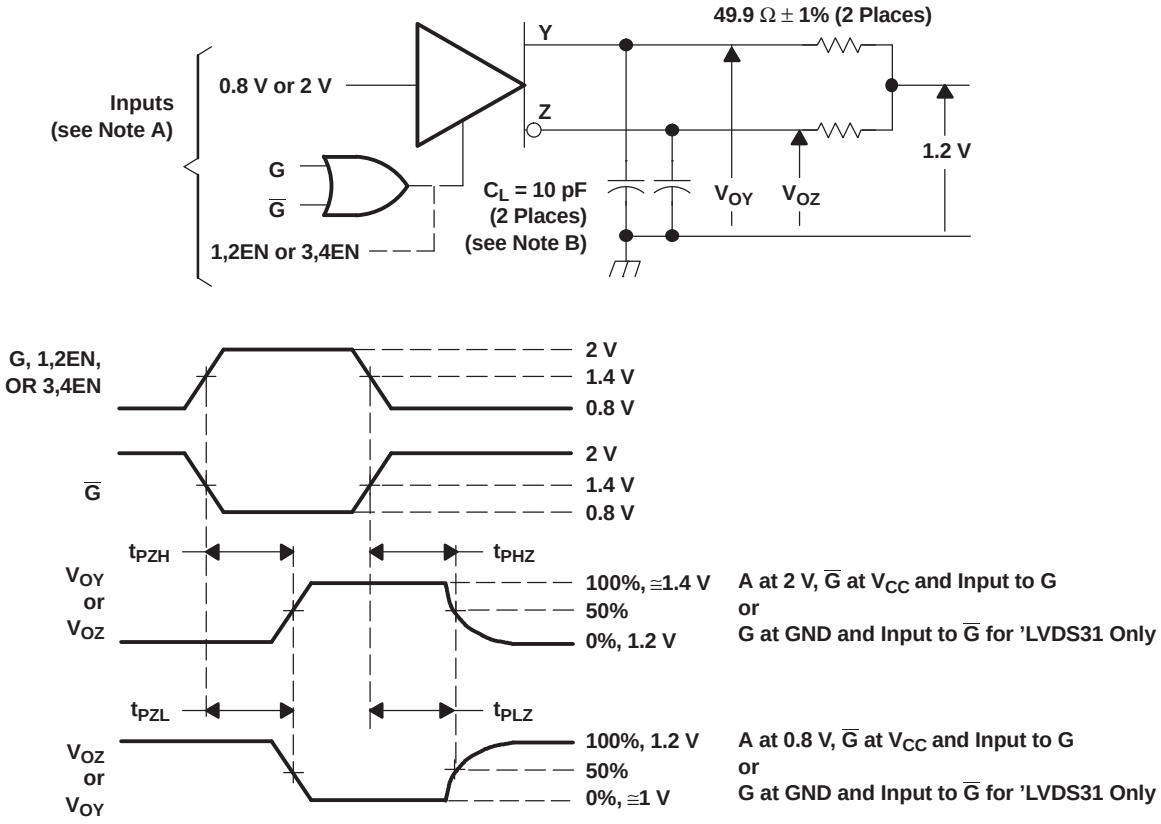
**Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**

## PARAMETER MEASUREMENT INFORMATION (continued)




NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. $C_L$ includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 300 MHz.

**Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**




NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f$ < 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.
B. $C_L$ includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

**Figure 4. Enable-/Disable-Time Circuit and Definitions**

## TYPICAL CHARACTERISTICS

**SUPPLY CURRENT vs FREQUENCY**

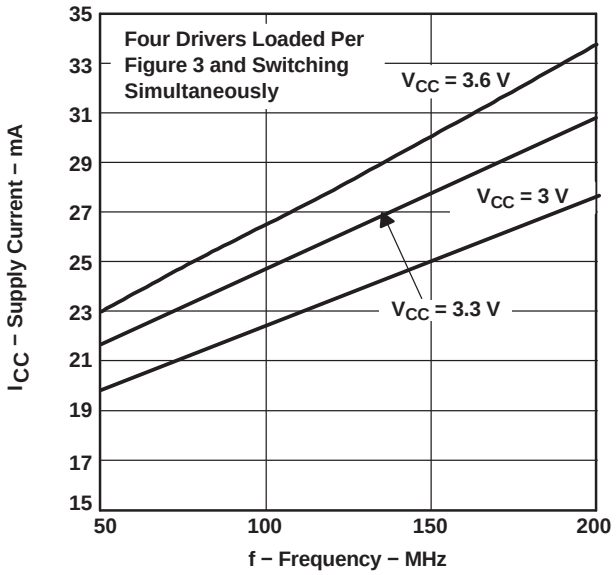



Figure 5.

**LOW-TO-HIGH PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

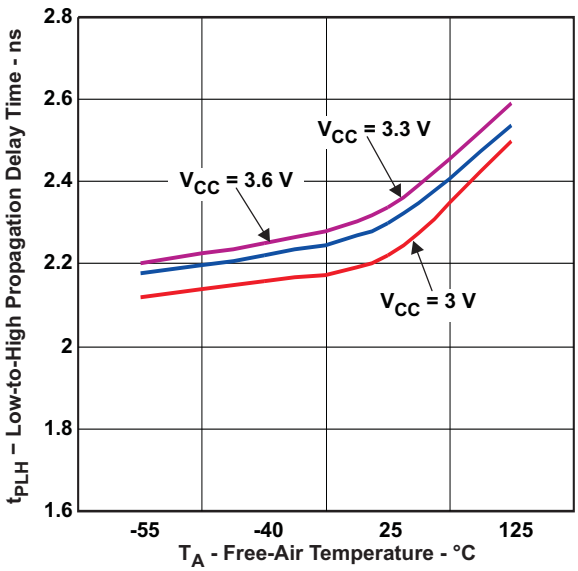



Figure 6.

**HIGH-TO-LOW PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE**

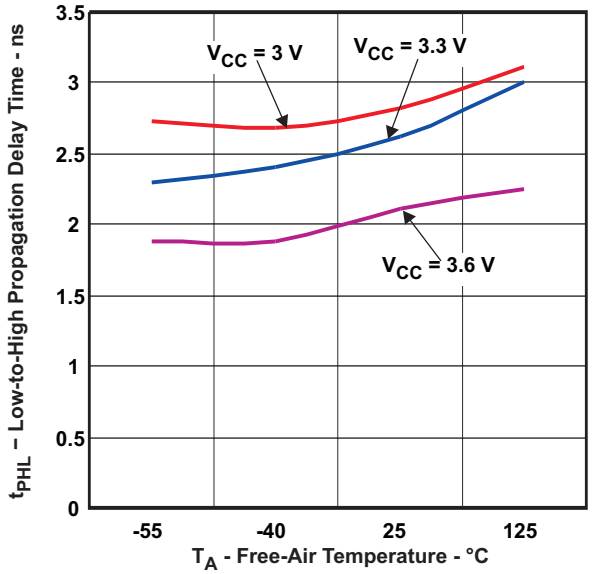
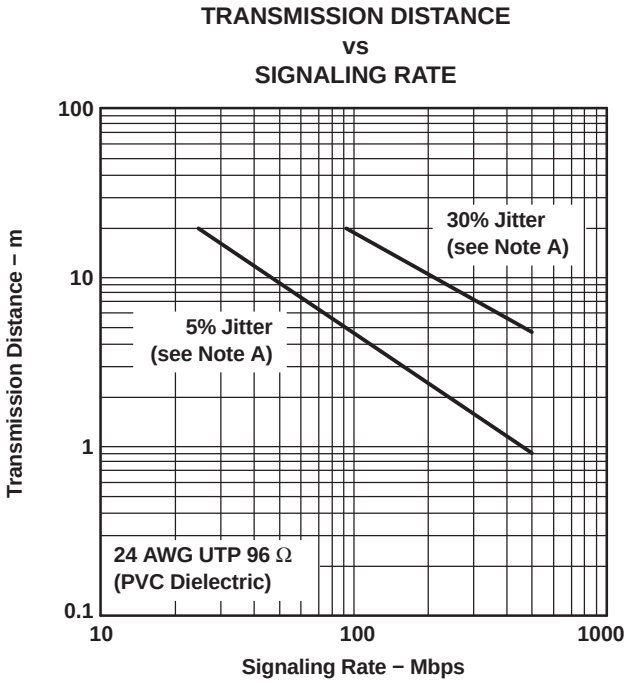



Figure 7.

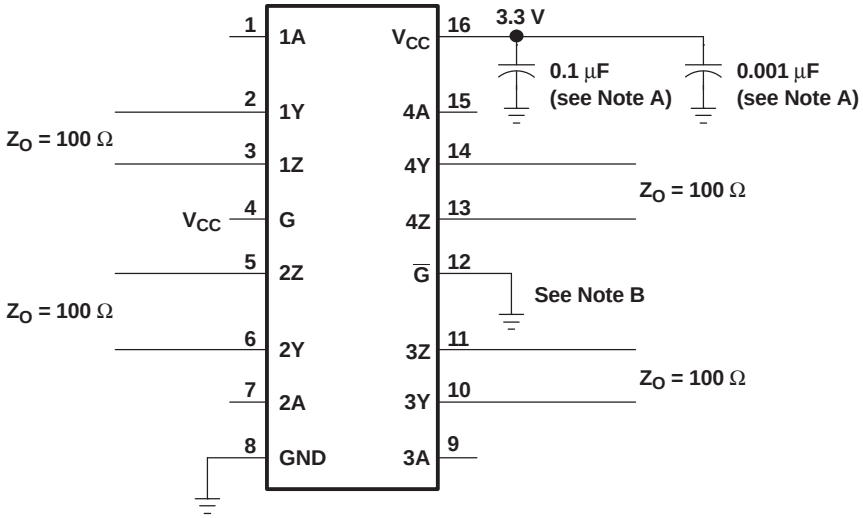
## APPLICATION INFORMATION

The SN55LVDS31 is generally used as a building block for high-speed point-to-point data transmission where ground differences are less than 1 V. The SN55LVDS31 can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.




A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

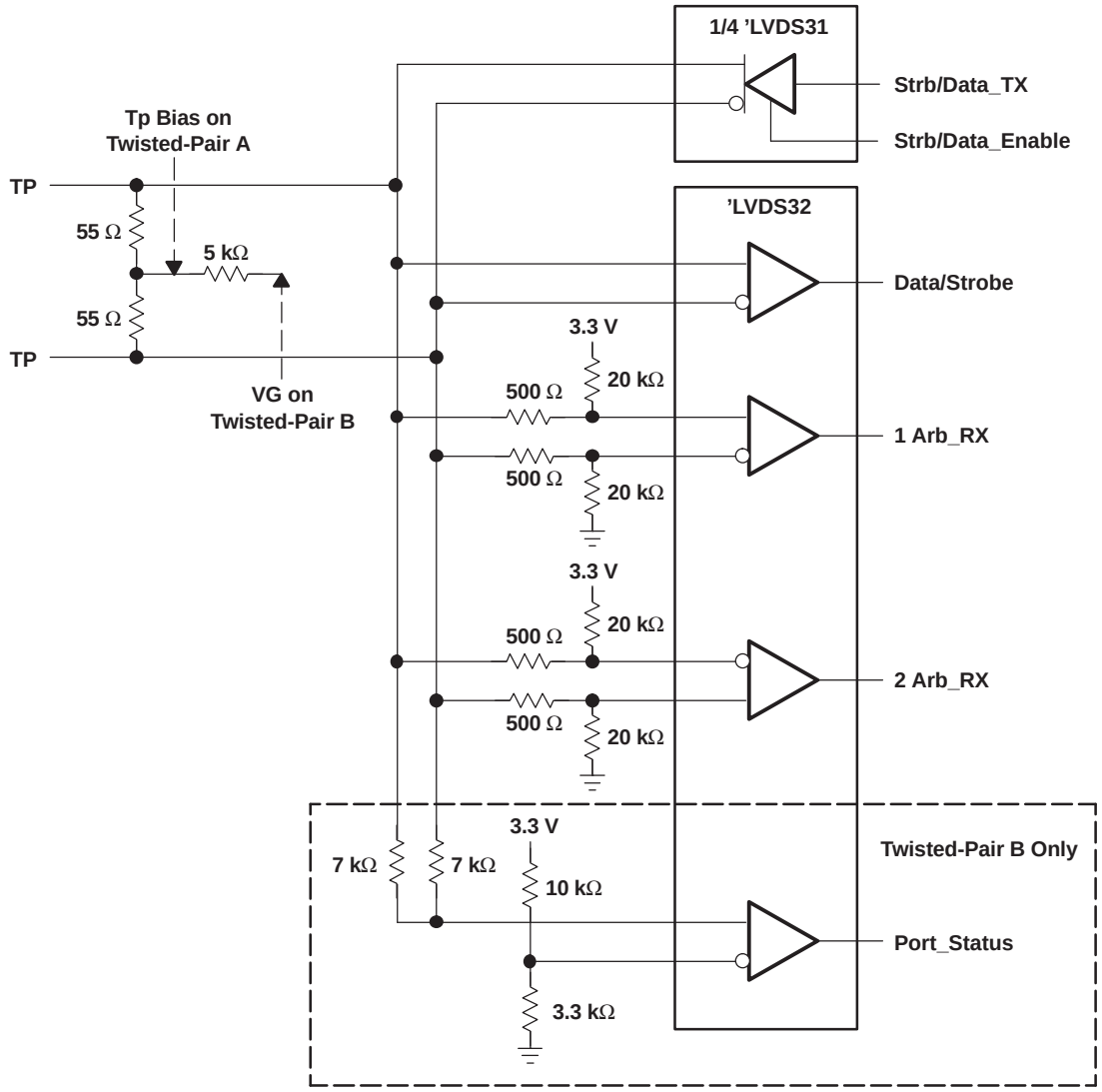
**Figure 8. Typical Transmission Distance Versus Signaling Rate**




NOTES: A. Place a 0.1-μF and a 0.001-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between $V_{CC}$ and the ground plane. The capacitors should be located as close as possible to the device terminals.

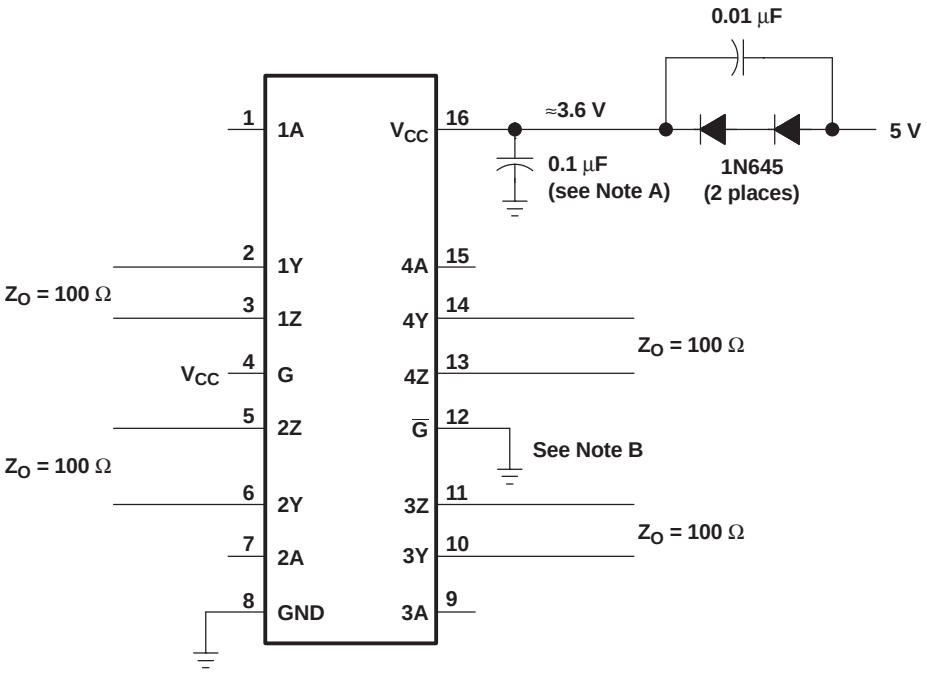
B. Unused enable inputs should be tied to $V_{CC}$ or GND, as appropriate.

**Figure 9. Typical Application Circuit Schematic**




NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
B. Decoupling capacitance is not shown, but recommended.
C. $V_{CC}$ is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

**Figure 10. 100-Mbps IEEE 1394 Transceiver**




A. Place a 0.1-µF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between $V_{CC}$ and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. Unused enable inputs should be tied to $V_{CC}$ or GND, as appropriate.

**Figure 11. Operation With 5-V Supply**

## COLD SPARING

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, $V_{CC}$ must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

## RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9762101VFA | ACTIVE | CFP | W | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9762101VFA SNV55LVDS31W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

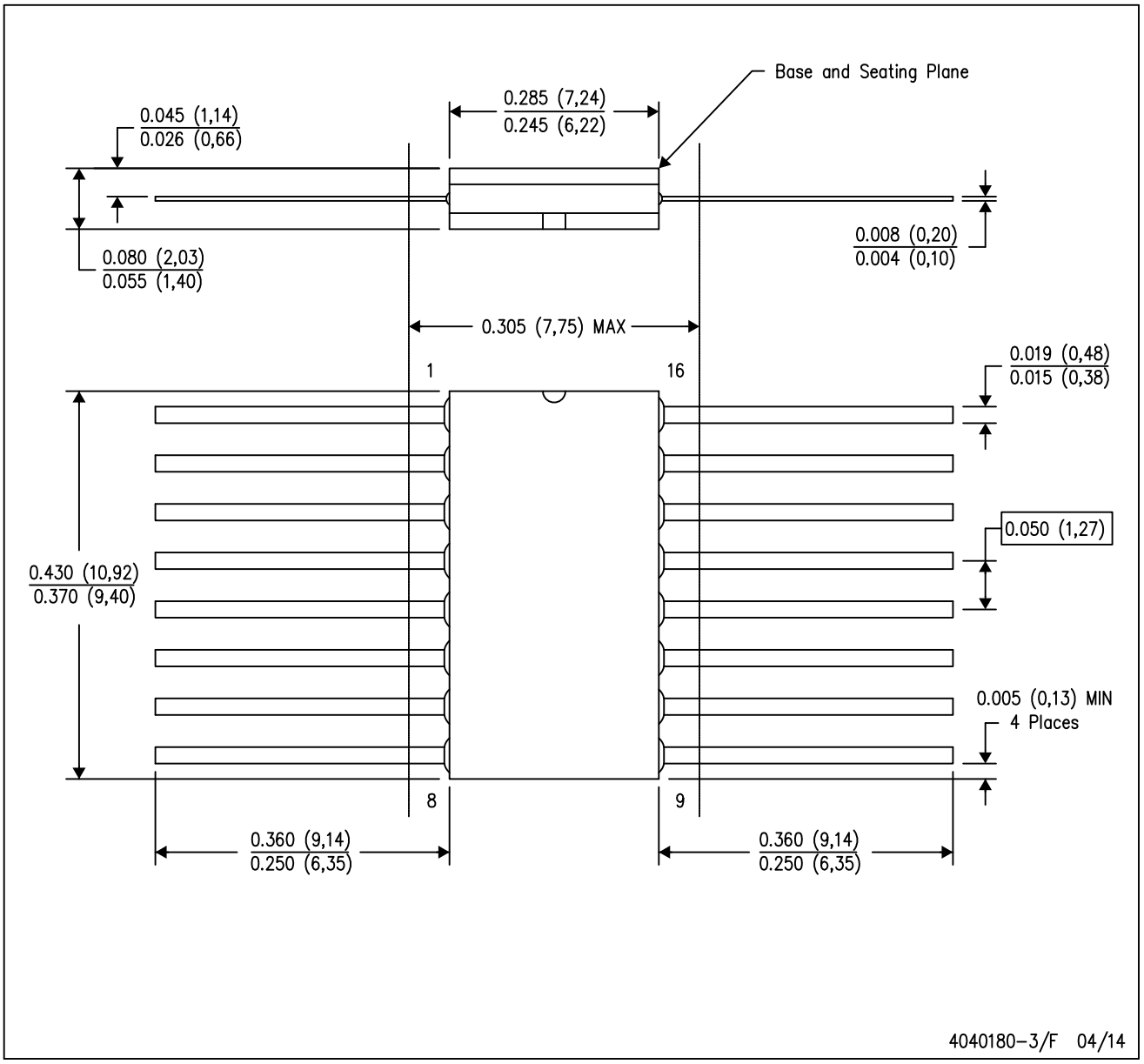
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

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