# 双路外设驱动器

查询样品: SN65472-EP

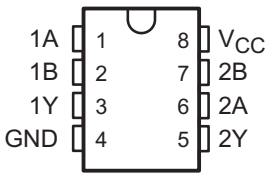
## 特性

- 特别针对高达 **300mA** 的使用
- 高压输出
- **55V** 时无输出闭锁
  （在传到 **300mA** 电流后）
- 中速切换
- 针对各种应用和逻辑功能选择的电路灵活性
- **TTL** 兼容二极管钳位输入
- 标准电源电压

## 支持工业应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持扩展（**-40°C** 至 **125°C**）温度范围 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

**D** 封装
（顶视图）




(1) 可定制工作温度范围

## 说明/订购信息

SN56472 双路外设驱动器可与系列 SN7452B 和系列 SN75462 进行功能互换，但是被设计用于要求更高击穿电压的系统。此系统以稍慢于系列 75452B 系列产品的开关速度为代价提供高于这些系列产品所能够提供的击穿电压（与 系列 SN75462 限值一样）。 典型应用包括高速逻辑缓冲器，电源驱动器，中继驱动器，灯驱动器，MOS 驱动器，线路驱动器和存储器驱动器。

SN65472 是一个双路外设 NAND 驱动器（假定为正逻辑电路），逻辑门的输出在内部被连接至 npn 输出晶体管的底部。

这个器件的运行温度范围为 -40°C 至 125°C。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

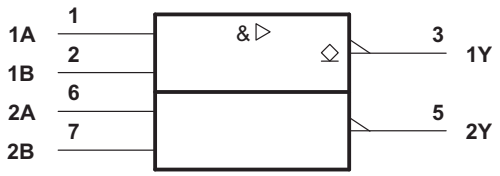
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| $T_J$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING | VID NUMBER |
|---|---|---|---|---|---|
| -40°C to 125°C | SOIC − D | Tape of 75 | SN65472DEP | 65472 | V62/13618-01XE-T |
| | | Reel of 2500 | SN65472DREP | 65472 | V62/13618-01XE |

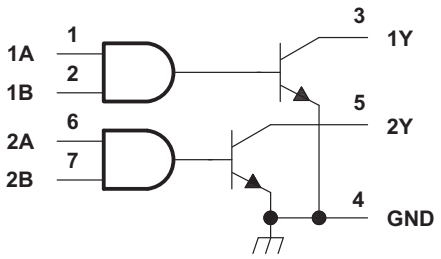
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## LOGIC SYMBOL




This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## LOGIC DIAGRAM (POSITIVE LOGIC)

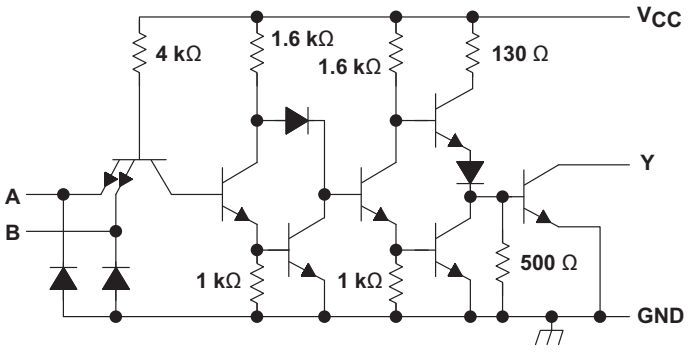



## Table 1. FUNCTION TABLE (EACH DRIVER)

| INPUTS | | Y(1) |
|---|---|---|
| A | B | |
| L | L | H (Off state) |
| L | H | H (Off state) |
| H | L | H (Off state) |
| H | H | L (On state) |

(1) positive logic: $Y = \overline{AB}$ or $\overline{A} + \overline{B}$

## SCHEMATIC (EACH DRIVER)




Resistor values shown are nominal.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range(2) | | 7 | V |
| $V_I$ | Input voltage | | 5.5 | V |
| | Inter-emitter voltage(3) | | 5.5 | V |
| $V_O$ | Off-state output voltage | | 70 | V |
| $I_O$ | Continuous collector or output current(4) | | 400 | mA |
| | Peak collector or output current ($t_w$ ≤ 10 ms, duty cycle ≤ 50%)(4) | | 500 | mA |
| $T_J$ | Absolute maximum junction temperature range | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the network GND, unless otherwise specified.
(3) This is the voltage between two emitters, A and B.
(4) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | SN65472-EP D 8 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(2) | 115.3 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance(3) | 59.7 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance(4) | 56.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter(5) | 13.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(6) | 55.6 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance(7) | N/A | |

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：ZHCA543）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，($\psi_{JT}$)，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 $\theta_{JA}$。
(6) 结至电路板的特征参数，($\psi_{JB}$)，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 $\theta_{JA}$。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2.1 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $T_A$ | Operating free-air temperature range | -40 | | 85 | °C |
| $T_J$ | Operating virtual junction temperature | -40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

These specifications apply for -40°C ≤ $T_J$ ≤ 125°C (unless otherwise noted)

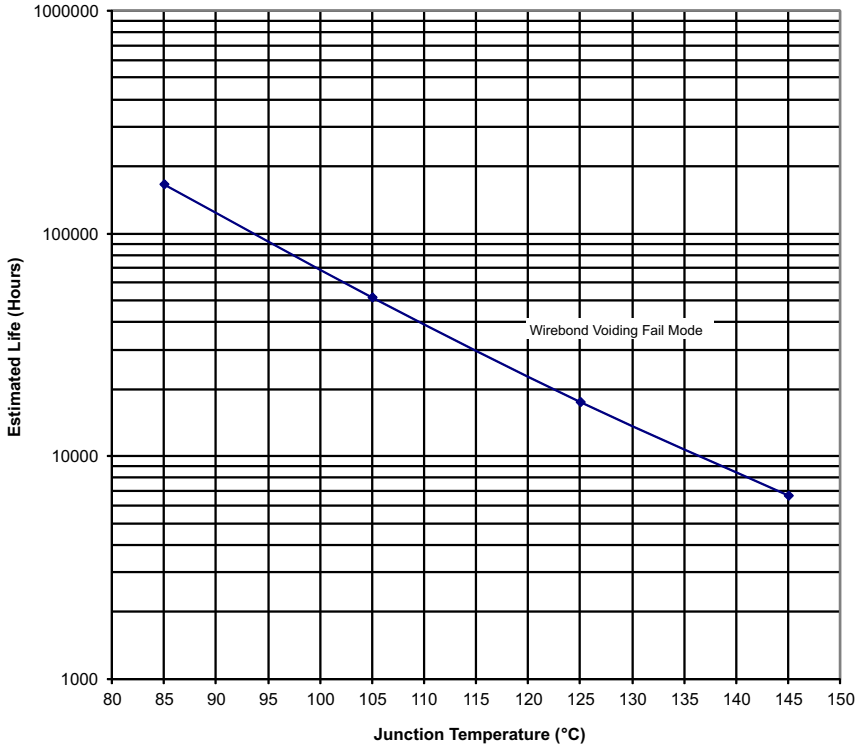
| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = 4.75 V, $I_I$ = – 12 mA | | -1.2 | -1.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.75 V, $V_{IH}$ = 2 V, $V_{OH}$ = 70 V | | | 270 | µA |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = 4.75 V, $V_{IL}$= 0.8 V, $I_{OL}$ = 100 mA | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = 4.75 V, $V_{IL}$= 0.8 V, $I_{OL}$ = 300 mA | | 0.5 | 0.75 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = 5.25 V, $V_I$ = 5.5 V | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 2.4 V | | | 44 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, $V_I$ = 0.4 V | | -1 | -1.6 | mA |
| $I_{CCH}$ | Supply current, outputs high | $V_{CC}$ = 5.25 V, $V_I$ = 5 V | | 13 | 17 | mA |
| $I_{CCL}$ | Supply current, outputs low | $V_{CC}$ = 5.25 V, $V_I$ = 0 | | 61 | 76 | mA |

(1) All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## SWITCHING CHARACTERISTICS

$V_{CC}$ = 5 V, $T_A$ = 25°C, over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $I_O$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, see Figure 2 | | 45 | 65 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $I_O$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, see Figure 2 | | 30 | 50 | ns |
| $t_{TLH}$ | Transition time, low-to-high-level output | $I_O$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, see Figure 2 | | 13 | 25 | ns |
| $t_{THL}$ | Transition time, high-to-low-level output | $I_O$ ≈ 200 mA, $C_L$ = 15 pF, $R_L$ = 50 Ω, see Figure 2 | | 10 | 20 | ns |
| $V_{OH}$ | High level output voltage after switching | $V_S$ = 55 V, $I_O$ ≈ 300 mA, see Figure 3 | $V_S$ - 18 | | | mV |

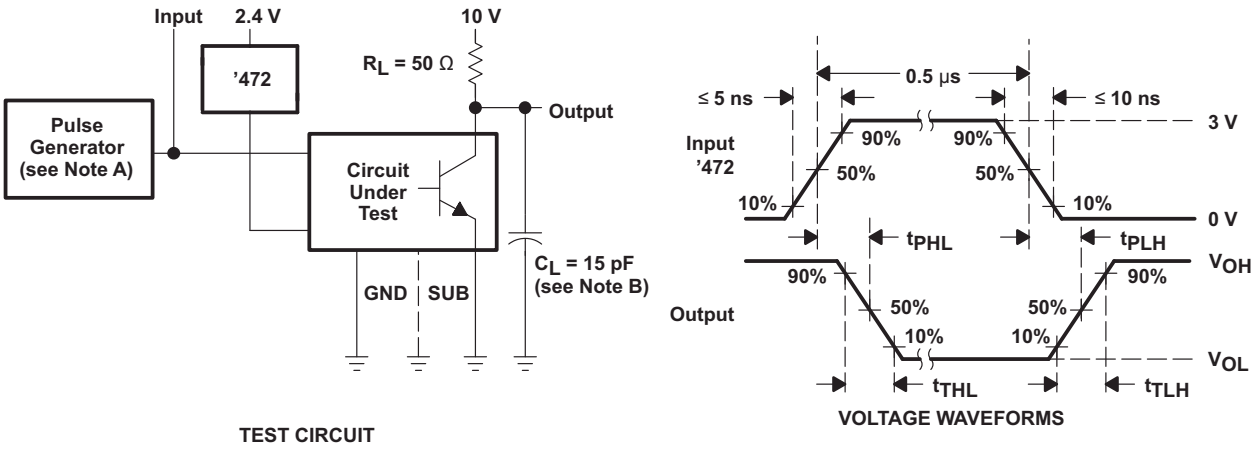



(1) See Datasheet for Absolute Maximum and minimum Recommended Operating Conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

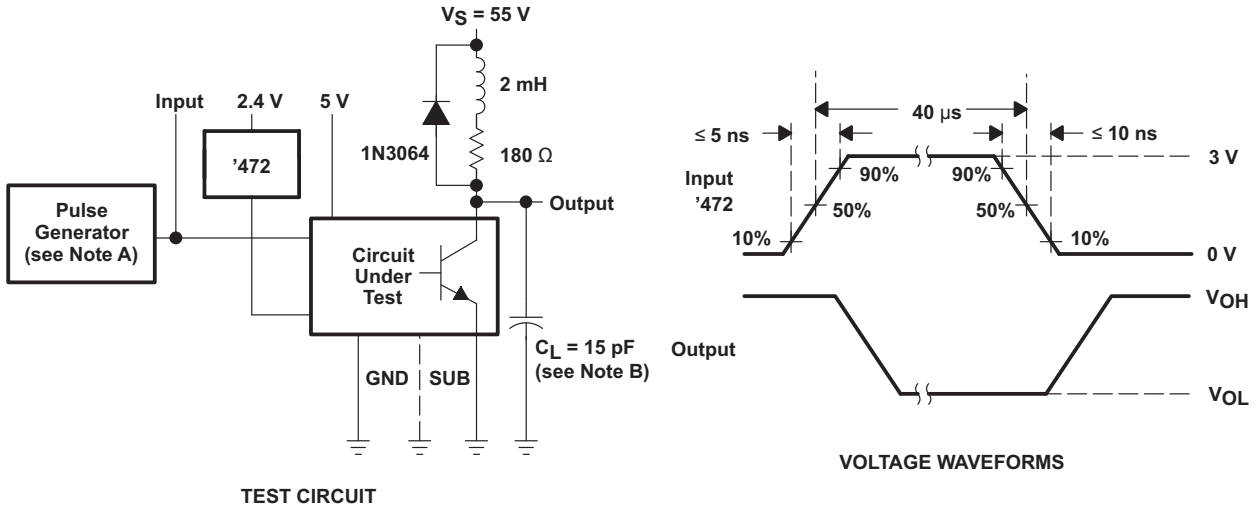
**Figure 1. SN65472-EP Wirebond Life Derating Chart**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_O$ ≈ 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 2. Switching Times**




NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, $Z_O$ ≈ 50 Ω.
B. $C_L$ includes probe and jig capacitance.

**Figure 3. Latch-Up Test**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65472DEP | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65472 | Samples |
| SN65472DREP | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65472 | Samples |
| V62/13618-01XE | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65472 | Samples |
| V62/13618-01XE-T | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65472 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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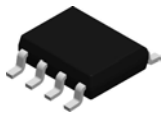
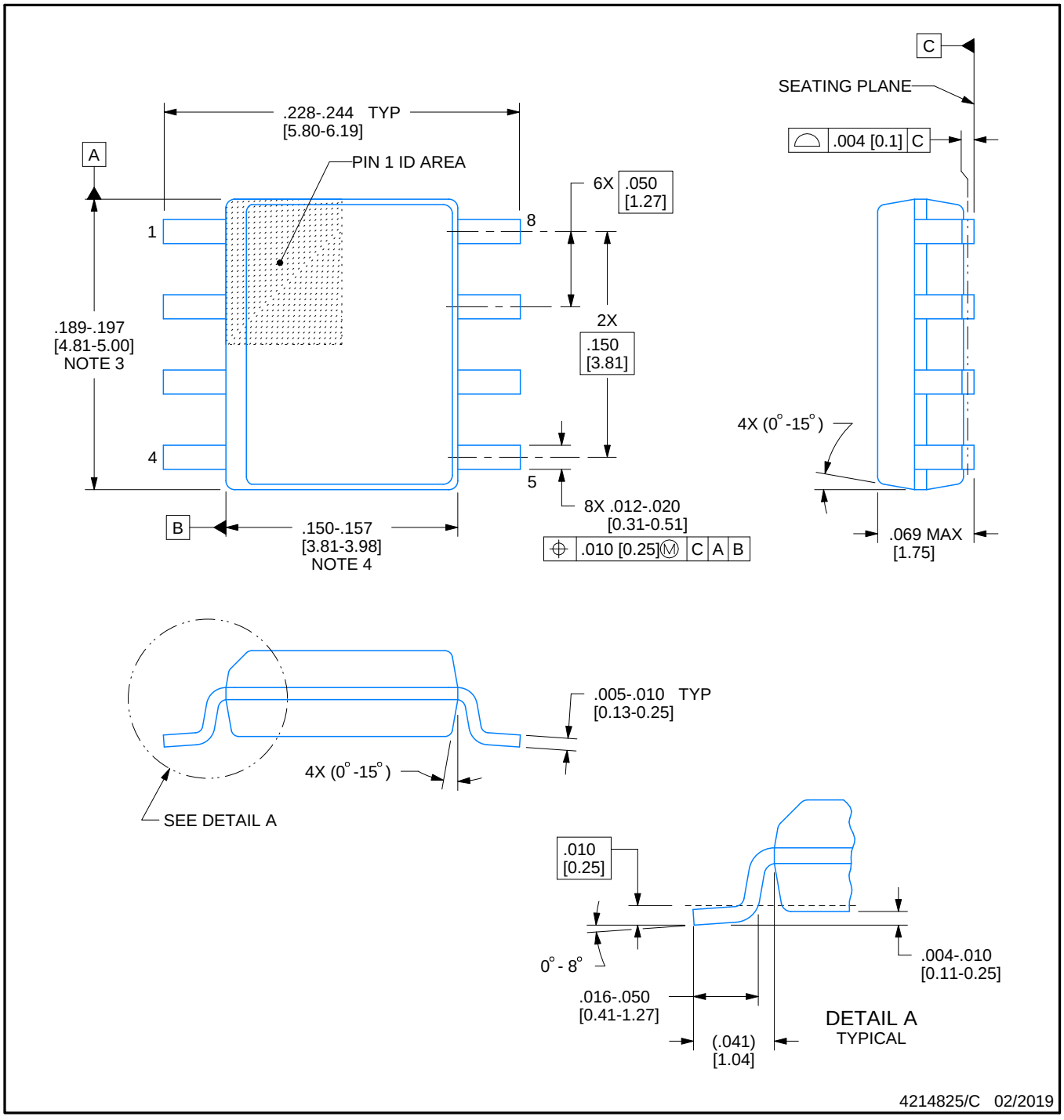


# PACKAGE OUTLINE

## D0008A

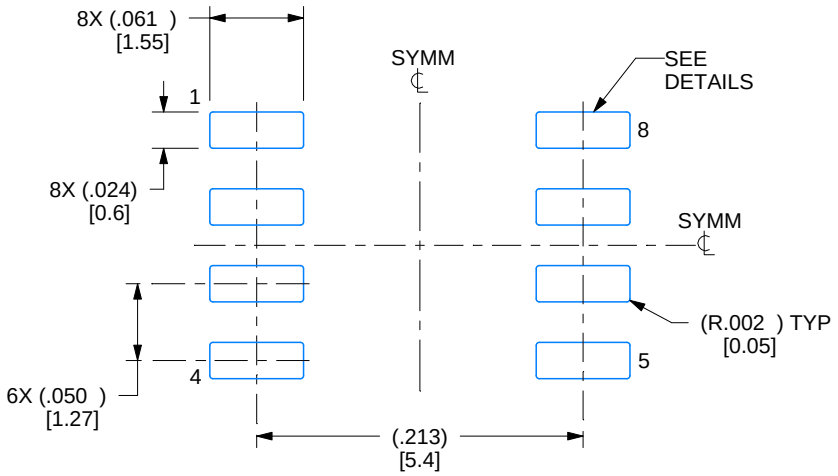
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

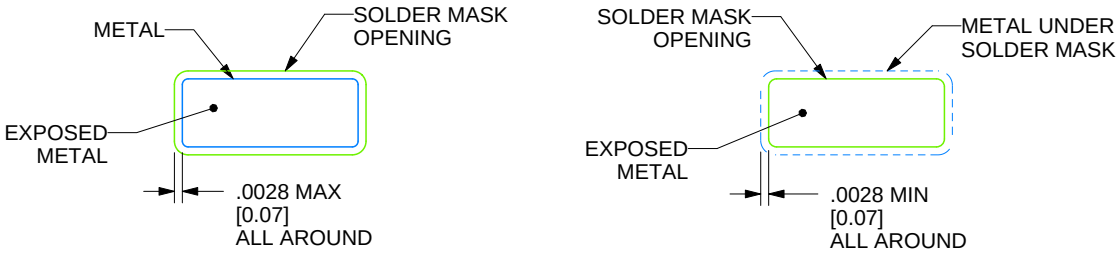



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

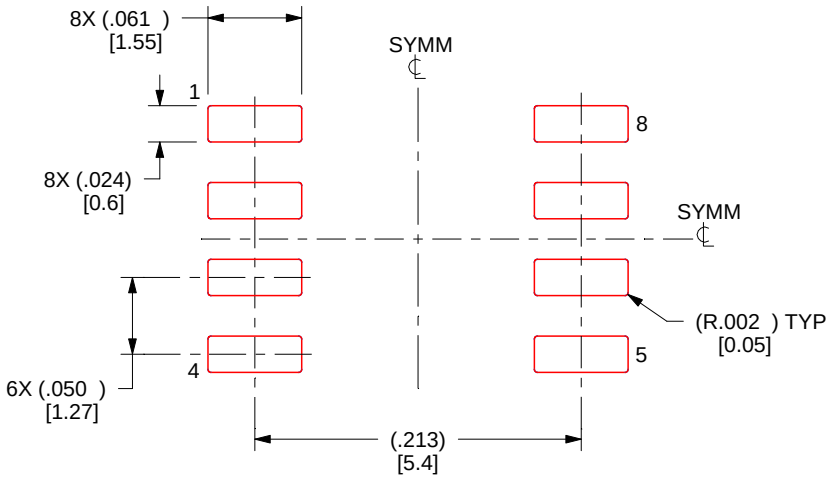
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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