

## SN65LBC173A-EP 四路 RS-485 差分线路接收器

### 1 特性

- 专为 TIA/EIA-485、TIA/EIA-422 和 ISO 8482 应用 设计
- 信号传输速率 <sup>(1)</sup>高达 50Mbps
- 在总线短路、开路和空闲总线条件下提供故障保护
- 为总线输入提供的静电放电 (ESD) 保护电压超过 6kV
- 共模总线电压输入范围: -7V 至 12V
- 传播延迟时间 < 18ns
- 低待机功耗: < 32 $\mu$ A
- 针对 AM26LS32、DS96F173、LTC488 和 SN75173 进行引脚兼容升级

### 2 应用

- 支持国防、航天和医疗 应用
  - 受控基线
  - 同一组装和测试场所
  - 同一制造场所
  - 延长的产品生命周期
  - 延长产品的变更通知周期
  - 产品可追溯性

(1) 线路的信号传输速率是指每秒钟的电压转换次数，单位为 bps（每秒比特数）。

### 3 说明

SN65LBC173A 是一款具有三态输出的四路差分接收器，专为 TIA/EIA-485 (RS-485)、TIA/EIA-422 (RS-422) 和 ISO 8482（欧盟的 RS-485）应用 而设计。

当数据速率高达甚至超过 5000bps 时，该器件针对均衡后的多点总线通信进行了优化。传输介质可采用双绞线电缆、印刷电路板走线或背板。最终数据传输速率和距离取决于介质衰减特性和环境噪声耦合。

接收器的正负共模输入电压范围较大，其 ESD 保护电压高达 6kV，适用于严苛环境中的 高速多点数据传输 应用。这些器件通过 LinBiCMOS<sup>®</sup>进行设计，兼具低功耗特性和极强稳定性。

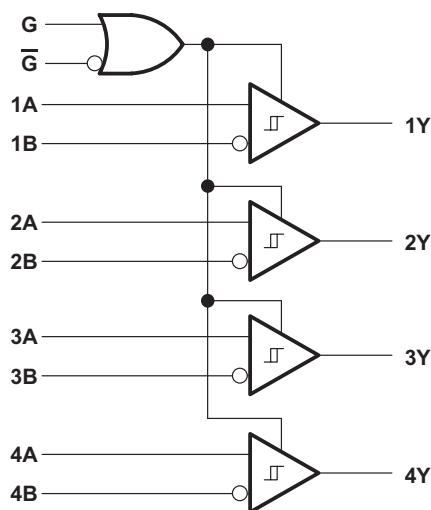
G 和  $\bar{G}$  输入为正/负逻辑提供使能控制逻辑，从而使能全部四个驱动器。禁用或关闭器件后，接收器输入针对总线呈现高阻抗状态，从而降低系统负载。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸（标称值）
SN65LBC173A-EP	SOIC (16)	9.90mm x 3.90mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

#### 逻辑图



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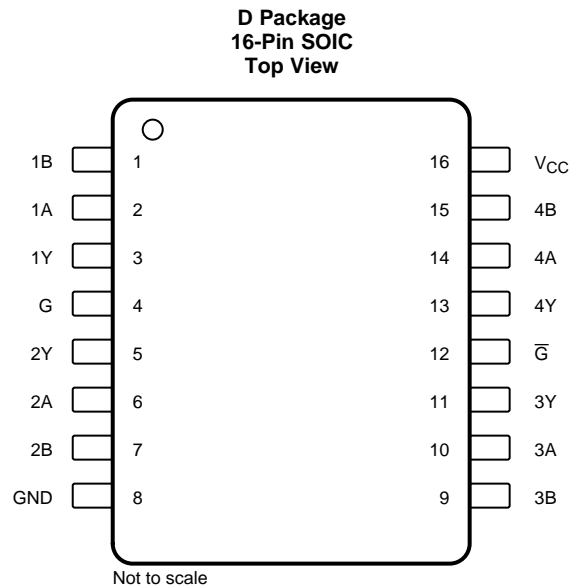
## 目录

<b>1</b>	特性 .....	1	8.3	Feature Description .....	10
<b>2</b>	应用 .....	1	8.4	Device Functional Modes .....	11
<b>3</b>	说明 .....	1	<b>9</b>	<b>Application and Implementation .....</b>	<b>12</b>
<b>4</b>	修订历史记录 .....	2	9.1	Application Information .....	12
<b>5</b>	<b>Pin Configuration and Functions .....</b>	<b>3</b>	9.2	Typical Application .....	12
<b>6</b>	<b>Specifications .....</b>	<b>4</b>	<b>10</b>	<b>Power Supply Recommendations .....</b>	<b>14</b>
6.1	Absolute Maximum Ratings .....	4	<b>11</b>	<b>Layout .....</b>	<b>14</b>
6.2	ESD Ratings .....	4	11.1	Layout Guidelines .....	14
6.3	Recommended Operating Conditions .....	4	11.2	Layout Example .....	14
6.4	Thermal Information .....	4	<b>12</b>	<b>器件和文档支持 .....</b>	<b>15</b>
6.5	Electrical Characteristics .....	5	12.1	接收文档更新通知 .....	15
6.6	Switching Characteristics .....	5	12.2	社区资源 .....	15
6.7	Typical Characteristics .....	7	12.3	商标 .....	15
<b>7</b>	<b>Parameter Measurement Information .....</b>	<b>8</b>	12.4	静电放电警告 .....	15
<b>8</b>	<b>Detailed Description .....</b>	<b>10</b>	12.5	Glossary .....	15
8.1	Overview .....	10	<b>13</b>	<b>机械、封装和可订购信息 .....</b>	<b>16</b>
8.2	Functional Block Diagram .....	10			

## 4 修订历史记录

日期	修订版本	注释
2016 年 11 月	*	最初发布版本。

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS-485 differential input (noninverting).
1B	1	I	RS-485 differential input (inverting).
1Y	3	O	Logic level output.
2A	6	I	RS-485 differential input (noninverting).
2B	7	I	RS-485 differential input (inverting).
2Y	5	O	Logic level output.
3A	10	I	RS-485 differential input (noninverting).
3B	9	I	RS-485 differential input (inverting).
3Y	11	O	Logic level output.
4A	14	I	RS-485 differential input (noninverting).
4B	15	I	RS-485 differential input (inverting).
4Y	13	O	Logic level output.
$\bar{G}$	12	I	Active-low select.
G	4	I	Active-high select.
GND	8	—	Ground.
V <sub>CC</sub>	16	—	Power supply.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{CC}$ <sup>(2)</sup>	-0.3	6	V
Voltage at any bus input (DC)	-10	15	V
Voltage at any bus input (transient pulse through 100 $\Omega$ , see <a href="#">图 10</a> )	-30	30	V
Input voltage at G and $\bar{G}$ , $V_I$	-0.5	$V_{CC} + 0.5$	V
Receiver output current, $I_O$	-10	10	mA
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to GND.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	A and B to GND	$\pm 6000$	V
		All pins	$\pm 5000$	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	All pins	$\pm 2000$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
	Voltage at any bus terminal	A, B		12	V
$V_{IH}$	High-level input voltage	G, $\bar{G}$		$V_{CC}$	V
$V_{IL}$	Low-level input voltage	G, $\bar{G}$		0.8	V
	Output current	Y		8	mA
$T_J$	Junction temperature	-55		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65LBC173A-EP		
		D (SOIC)		
		16 PINS		
$\theta_{JA}$	Junction-to-ambient thermal resistance	78		°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance	39.5		°C/W
$\theta_{JB}$	Junction-to-board thermal resistance	35.4		°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	8.5		°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	35.1		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IT+</sub>	Positive-going differential input voltage threshold	-7 V ≤ V <sub>CM</sub> ≤ 12 V (V <sub>CM</sub> = (V <sub>A</sub> + V <sub>B</sub> ) / 2)			-80	-10	mV
V <sub>IT-</sub>	Negative-going differential input voltage threshold				-200	-120	mV
V <sub>HYS</sub>	Hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )				40		mV
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18 mA		-1.5	-0.8		V
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV, I <sub>OH</sub> = -8 mA	See 图 6	2.7	4.8		V
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -200 mV, I <sub>OL</sub> = 8 mA			0.2	0.4	V
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>		-1		1	μA
I <sub>I</sub>	Line input current	Other input at 0 V, V <sub>CC</sub> = 0 V or 5 V	V <sub>I</sub> = 12 V			0.9	mA
			V <sub>I</sub> = -7 V	-0.7			
I <sub>IH</sub>	High-level input current	Enable inputs G, $\overline{G}$				110	μA
I <sub>IL</sub>	Low-level input current						
R <sub>I</sub>	Input resistance	A, B inputs		12			kΩ
I <sub>CC</sub>	Supply current	V <sub>ID</sub> = 5 V	G at 0 V, $\overline{G}$ at V <sub>CC</sub>			32	μA
		No load	G at V <sub>CC</sub> , $\overline{G}$ at 0 V		11	16	mA

(1) All typical values are at V<sub>CC</sub> = 5 V and 25°C.

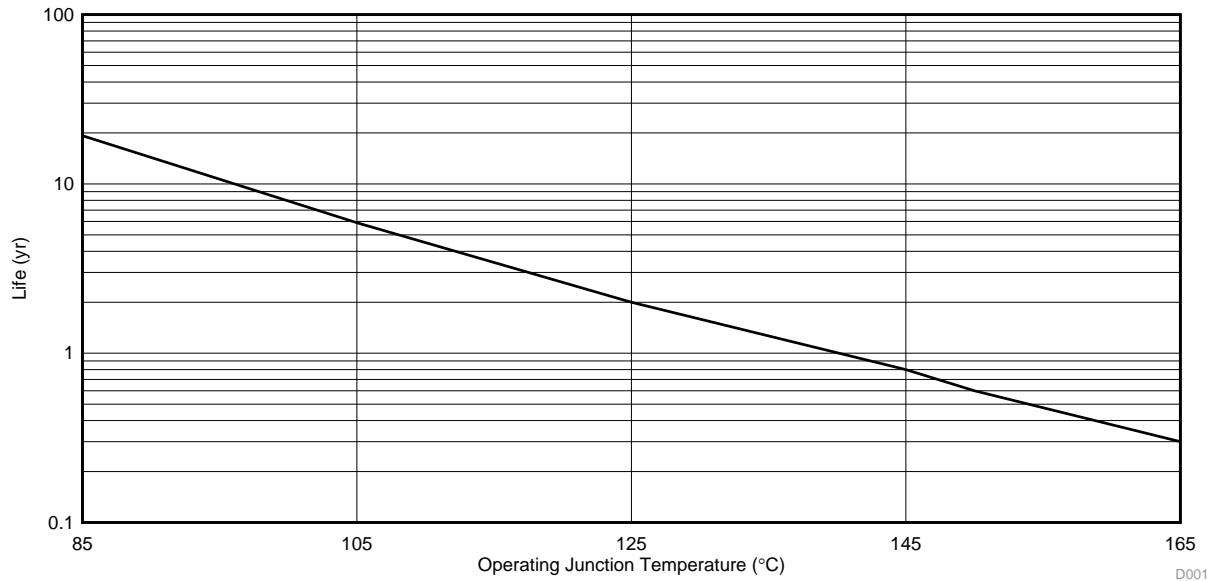
## 6.6 Switching Characteristics

over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>r</sub>	Differential output voltage rise time		2	7	ns	
t <sub>f</sub>	Differential output voltage fall time		2	7	ns	
t <sub>PLH</sub>	Propagation delay time, low-to-high level output	V <sub>ID</sub> = -3 V to 3 V, See 图 7	8	12	18	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low level output		8	12	18	ns
t <sub>PZH</sub>	Propagation delay time, high-impedance-to-high-level output		27	39	ns	
t <sub>PHZ</sub>	Propagation delay time, high-level-output-to-high impedance	See 图 8	7	24	ns	
t <sub>PZL</sub>	Propagation delay time, high-impedance-to-low-level output		29	39	ns	
t <sub>PLZ</sub>	Propagation delay time, low-level-output-to-high impedance	See 图 9	12	18	ns	
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PLH</sub> - t <sub>PHL</sub>  )		0.2	2	ns	
t <sub>sk(o)</sub>	Output skew <sup>(1)</sup>			3	ns	
t <sub>sk(pp)</sub>	Part-to-part skew <sup>(2)</sup>			3	ns	

(1) Output skew (t<sub>sk(o)</sub>) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

(2) Part-to-part skew (t<sub>sk(pp)</sub>) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.



- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

**图 1. SN65LBC173A-EP Wirebond Life Derating Chart**

### 6.7 Typical Characteristics

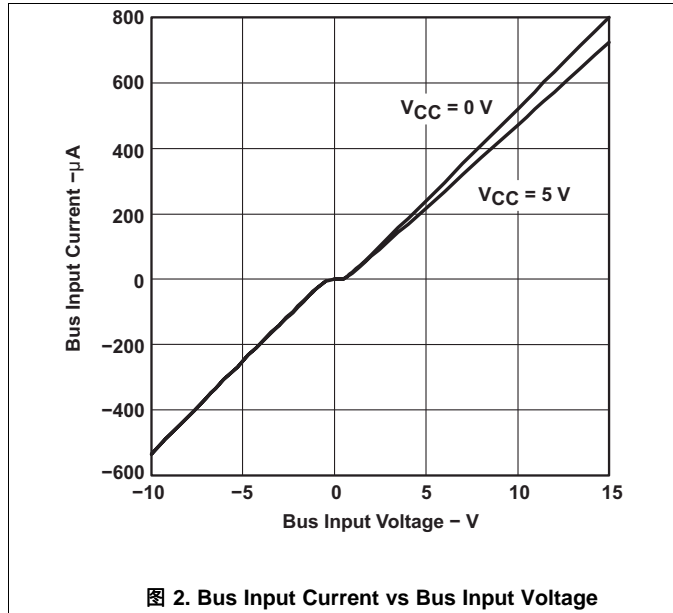


图 2. Bus Input Current vs Bus Input Voltage

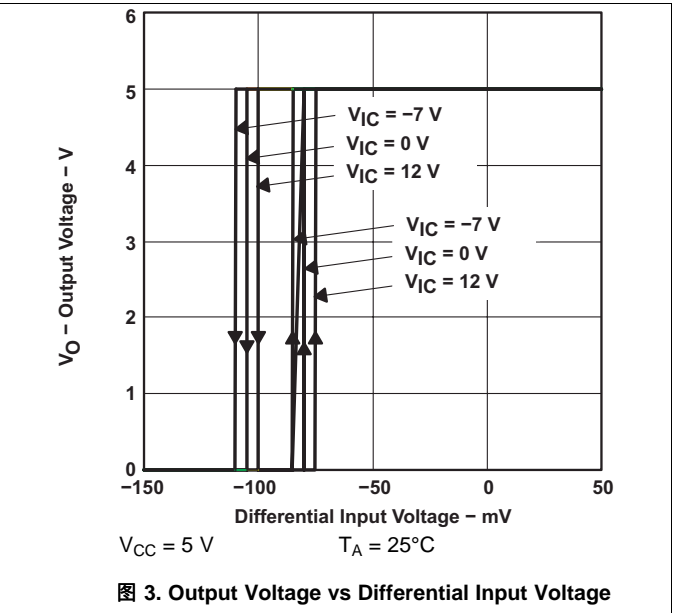


图 3. Output Voltage vs Differential Input Voltage

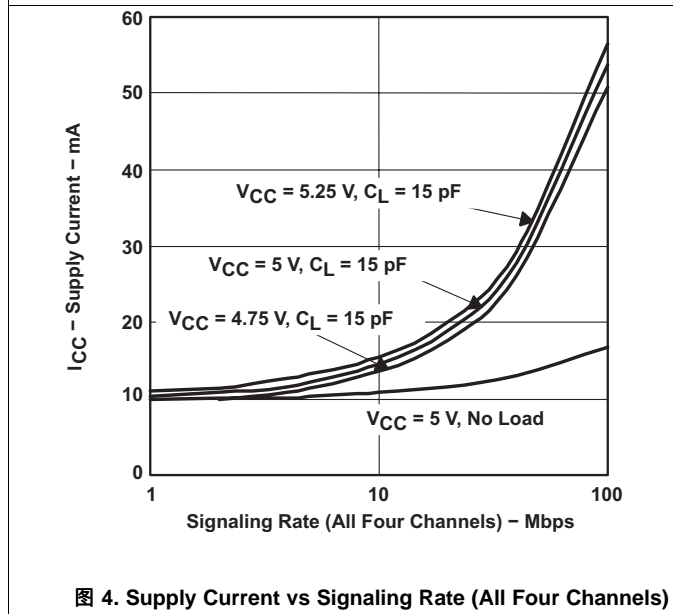


图 4. Supply Current vs Signaling Rate (All Four Channels)

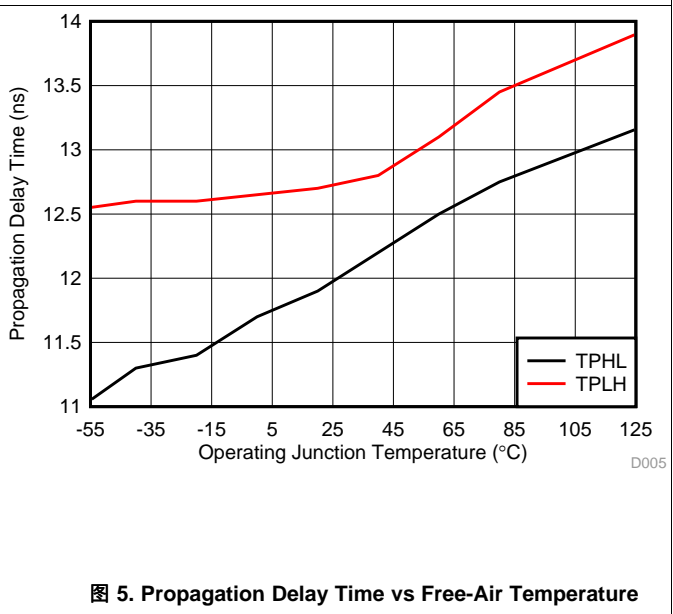


图 5. Propagation Delay Time vs Free-Air Temperature

## 7 Parameter Measurement Information

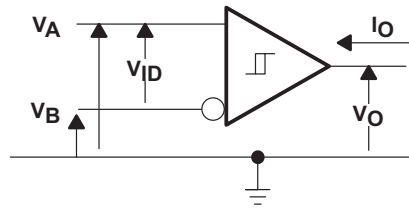
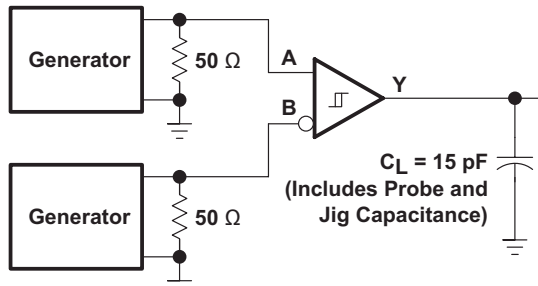


图 6. Voltage and Current Definitions



Generators: PRR = 1 MHz, 50% Duty Cycle,  
 $t_r < 6$  ns,  $Z_o = 50 \Omega$

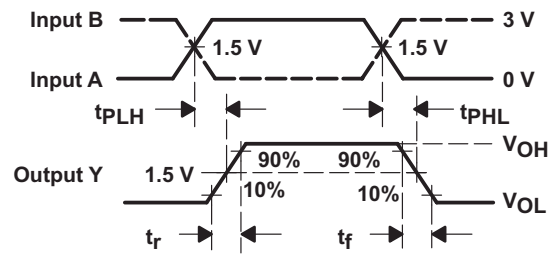
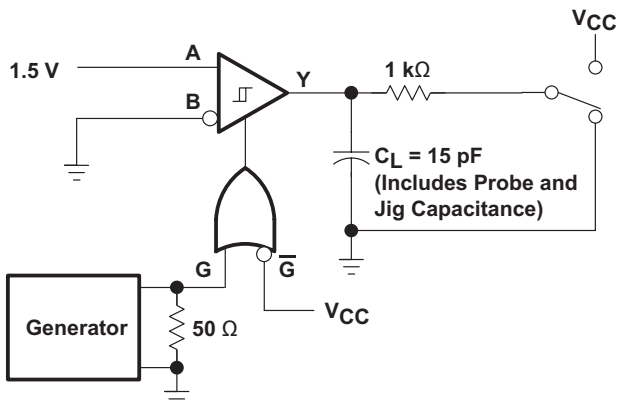


图 7. Switching Test Circuit and Waveforms



Generators: PRR = 1 MHz, 50% Duty Cycle,  
 $t_r < 6$  ns,  $Z_o = 50 \Omega$

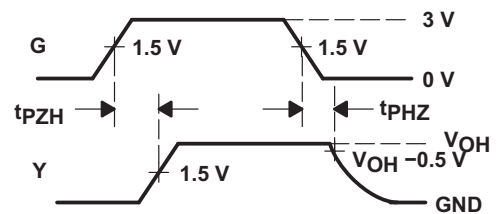


图 8. Test Circuit Waveforms,  $t_{PZH}$  and  $t_{PHZ}$



Parameter Measurement Information (接下页)

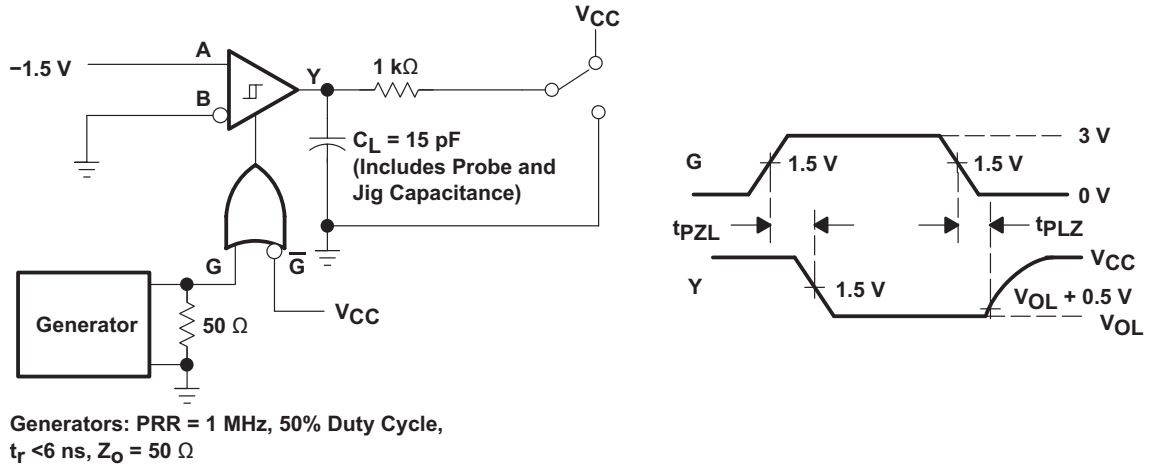


图 9. Test Circuit Waveforms,  $t_{pZL}$  and  $t_{PLZ}$

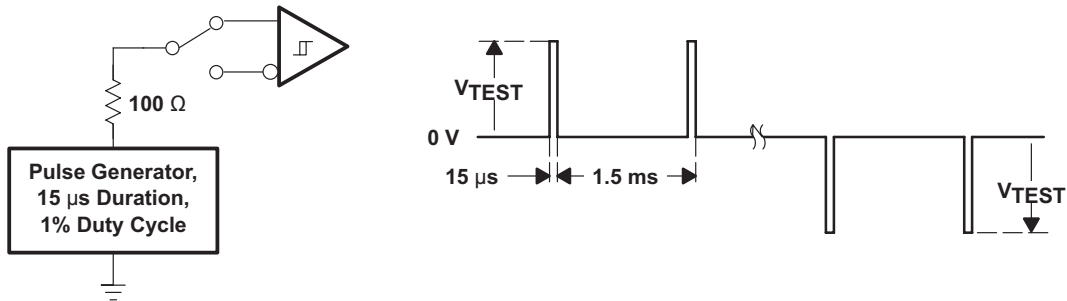


图 10. Test Circuit and Waveform, Transient Over-Voltage Test

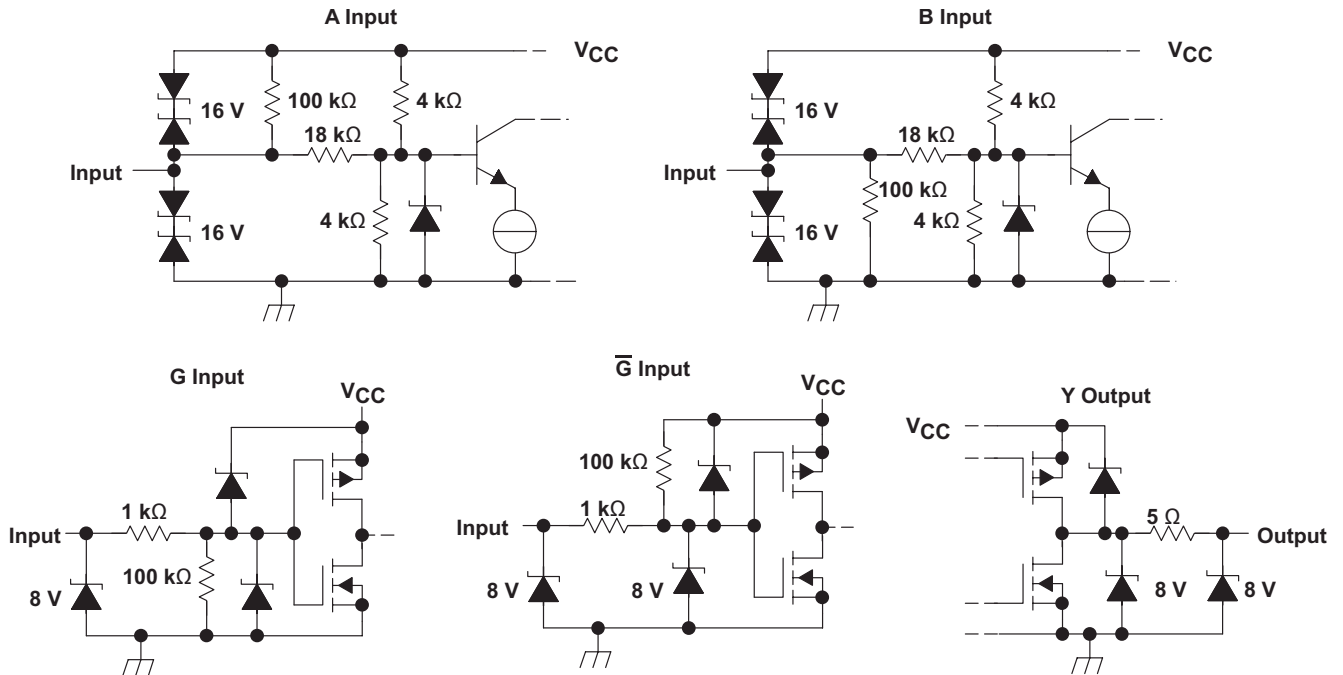


图 11. Equivalent Input and Output Schematic Diagrams

## 8 Detailed Description

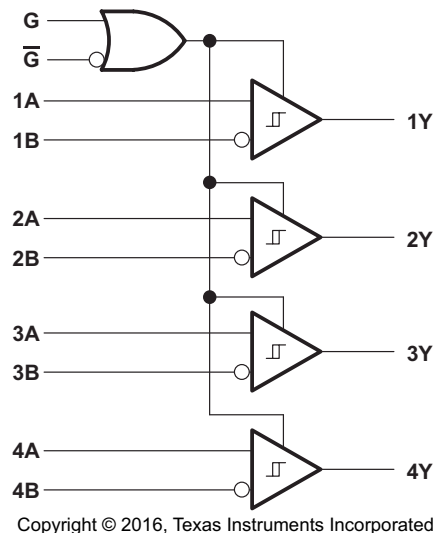
### 8.1 Overview

The SN65LBC173A is a quadruple differential line receiver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications. This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS®, facilitating low-power consumption and robustness.

The  $G$  and  $\bar{G}$  inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The device can be configured using the  $G$  and  $\bar{G}$  logic inputs to select receiver output. The high voltage or logic 1 on the  $G$  pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the  $\bar{G}$  enables active low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

## 8.4 Device Functional Modes

The receivers implemented in these RS-485 device can be configured using the G and  $\overline{G}$  logic pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

表 1. Function Table<sup>(1)</sup>

INPUT A - B ( $V_{ID}$ )	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \leq -0.2 \text{ V}$	H	X	L
	X	L	
$-0.2 \text{ V} < V_{ID} < -0.01 \text{ V}$	H	X	?
	X	L	
$-0.01 \text{ V} \leq V_{ID}$	H	X	H
	X	L	
X	L	H	Z
	OPEN	OPEN	
Short circuit	H	X	H
	X	L	
Open circuit	H	X	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

## 9 Application and Implementation

### 注

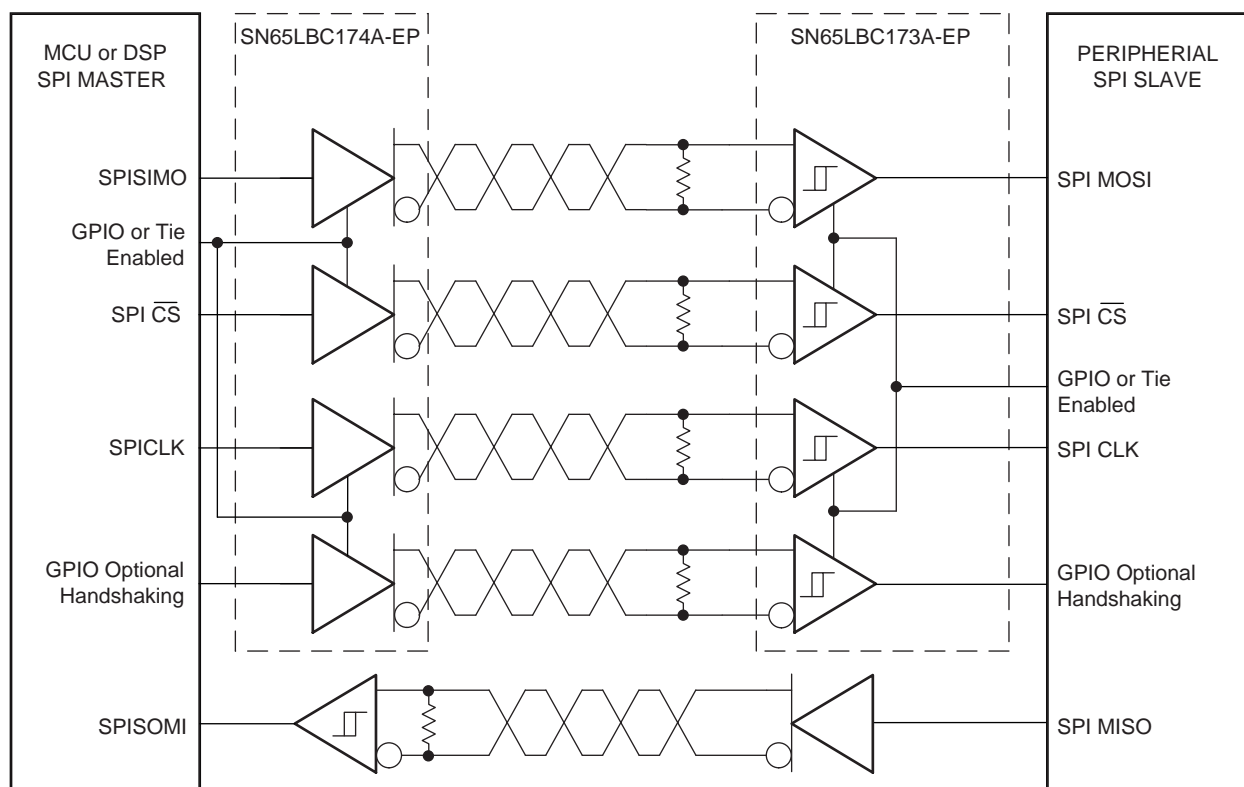
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Extending SPI operation over RS-485 link.

### 9.2 Typical Application

The following block diagram shows an MCU host connected via RS-485 to a SPI slave device. This device can be an ADC, DAC, MCU, or other SPI slave peripheral.



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图 12. DSP-to-DSP Link via Serial Peripheral Interface

#### 9.2.1 Design Requirements

This application can be implemented using standard SPI protocol on DSP or MCU devices. The interface is independent of the specific frame or data requirements of the host or slave device. An additional but not required handshake bit is provided that can be used for customer purposes.

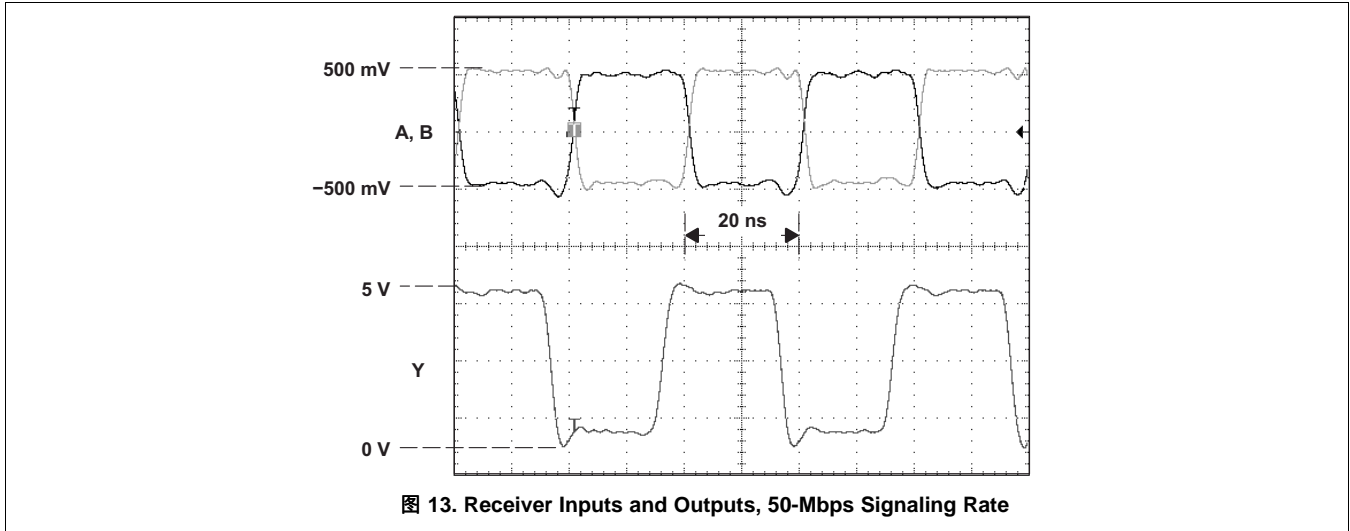
#### 9.2.2 Detailed Design Procedure

The interface design requirements are fairly straight forward in this single source/destination scenario. Trace lengths and cable lengths need to be matched to maximize SPI timing. If there is a benefit to put the interface to sleep, GPIOs can be used to control the enable signals of the transmitter and receiver. If GPIOs are not available, or constant uptime needed, both the enables on transmit and receive can be hard tied enabled.

### Typical Application (接下页)

The link shown can operate at up to 50 Mbps, well within the capability of most SPI links.

#### 9.2.3 Application Curves



## 10 Power Supply Recommendations

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.
- Place termination resistor as close as possible to the input pins (if end point node).
- Keep trace lengths from input pins to buss as short as possible to reduce stub lengths and reflections on any nodes that are not end points of bus.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

### 11.2 Layout Example

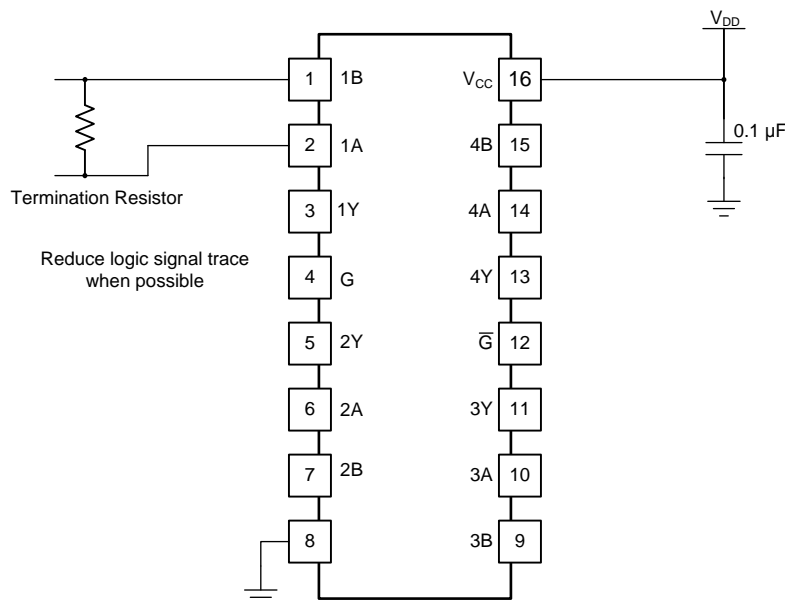


图 14. Layout with PCB Recommendations

## 12 器件和文档支持

### 12.1 接收文档更新通知

如需接收文档更新通知，请访问 [www.ti.com.cn](http://www.ti.com.cn) 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 商标

E2E is a trademark of Texas Instruments.

LinBiCMOS is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

### 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC173AMDREP	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP	<a href="#">Samples</a>
V62/13623-02XE	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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