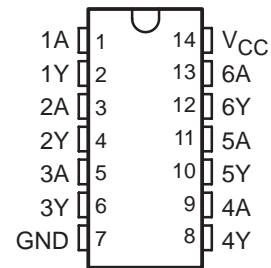


SN74HCT14-Q1 HEX SCHMITT-TRIGGER INVERTER

SCLS588A – JULY 2004 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible

D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74HCT14 device contains six independent inverters. The device performs the Boolean function $Y = \bar{A}$ in positive logic.

ORDERING INFORMATION†

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN74HCT14QDRQ1	HCT14Q
	TSSOP – PW	Reel of 2000	SN74HCT14QPWRQ1	HCT14Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN74HCT14-Q1

HEX SCHMITT-TRIGGER INVERTER

SCLS588A – JULY 2004 – REVISED APRIL 2008

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_I Input voltage	0	V_{CC}	V
V_O Output voltage	0	V_{CC}	V
T_A Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{T+} Positive-going threshold		4.5 V	1.2	1.5	1.9	1.2	1.9	V
		5.5 V	1.4	1.7	2.1	1.4	2.1	
V_{T-} Negative-going threshold		4.5 V	0.5	0.9	1.2	0.5	1.2	V
		5.5 V	0.6	1	1.4	0.6	1.4	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)		4.5 V	0.4	0.6	1.4	0.4	1.4	V
		5.5 V	0.4	0.65	1.5	0.4	1.5	
V_{OH}	$I_{OH} = -20 \mu\text{A}$	4.5 V	4.4	4.49		4.4		V
	$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		
V_{OL}	$I_{OL} = 20 \mu\text{A}$	4.5 V		0.001	0.1		0.1	V
	$I_{OL} = 4 \text{ mA}$	4.5 V		0.17	0.26		0.4	
I_I	$V_I = V_{CC}$ or GND	5.5 V				± 0.1	± 1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40	μA
ΔI_{CC}^\ddagger	One input at 0.5 V or 2.4 V, Other inputs at GND or V_{CC}	5.5 V		0.2	2.4		3	mA
C_i	$V_I = V_{CC}$ or GND	5 V		3	10		10	pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .



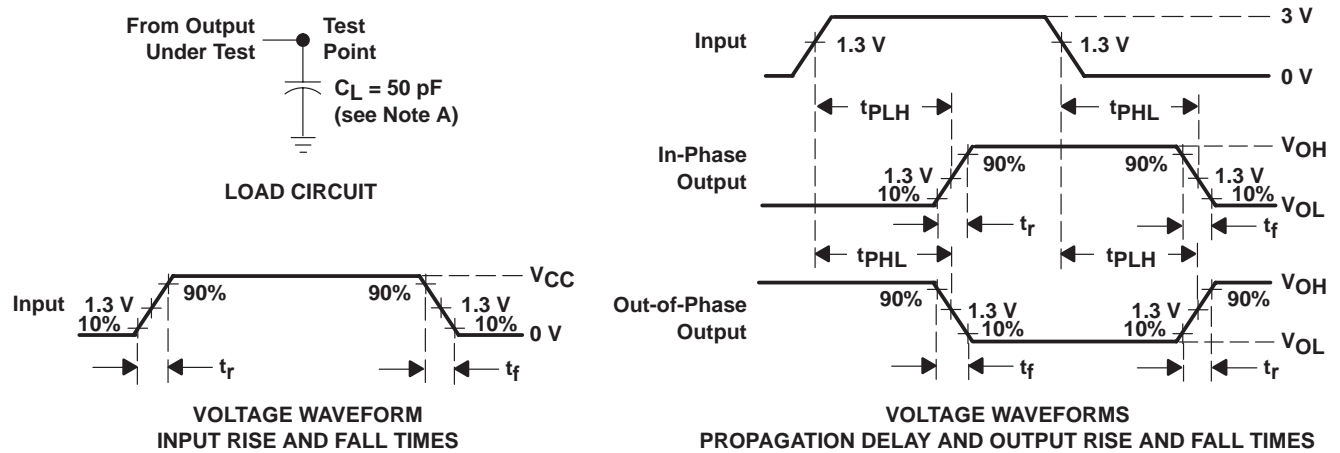
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	A	Y	4.5 V		20	32		48	ns
			5.5 V		18	30		45	
t_t		Y	4.5 V		7	15		22	ns
			5.5 V		6	14		20	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	10	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

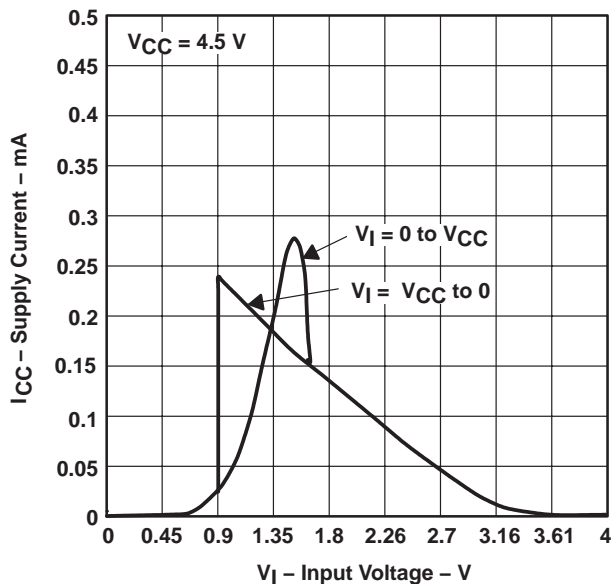
Figure 1. Load Circuit and Voltage Waveforms

SN74HCT14-Q1 HEX SCHMITT-TRIGGER INVERTER

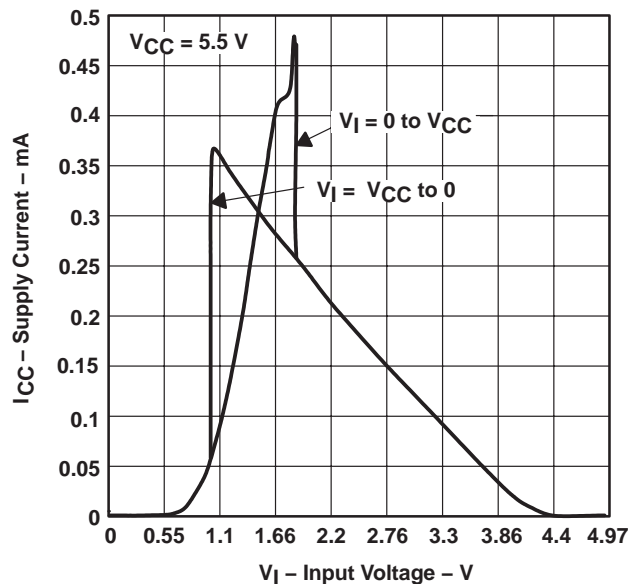
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TYPICAL CHARACTERISTICS

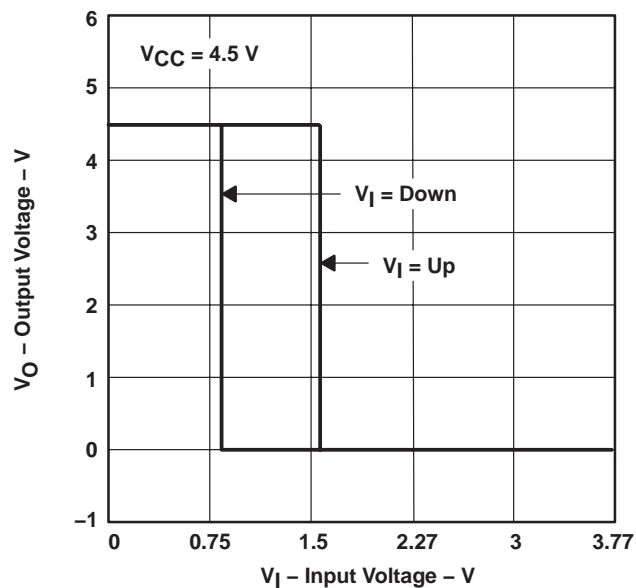
SUPPLY CURRENT
vs
INPUT VOLTAGE



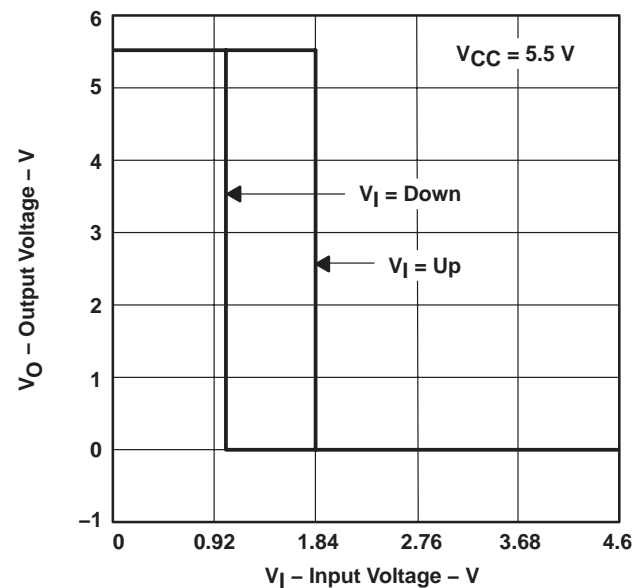
SUPPLY CURRENT
vs
INPUT VOLTAGE



OUTPUT VOLTAGE
vs
INPUT VOLTAGE



OUTPUT VOLTAGE
vs
INPUT VOLTAGE



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT14QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT14Q	Samples
SN74HCT14QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	HCT14Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74HCT14-Q1 :

- Catalog: [SN74HCT14](#)
- Military: [SN54HCT14](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT14QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT14QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

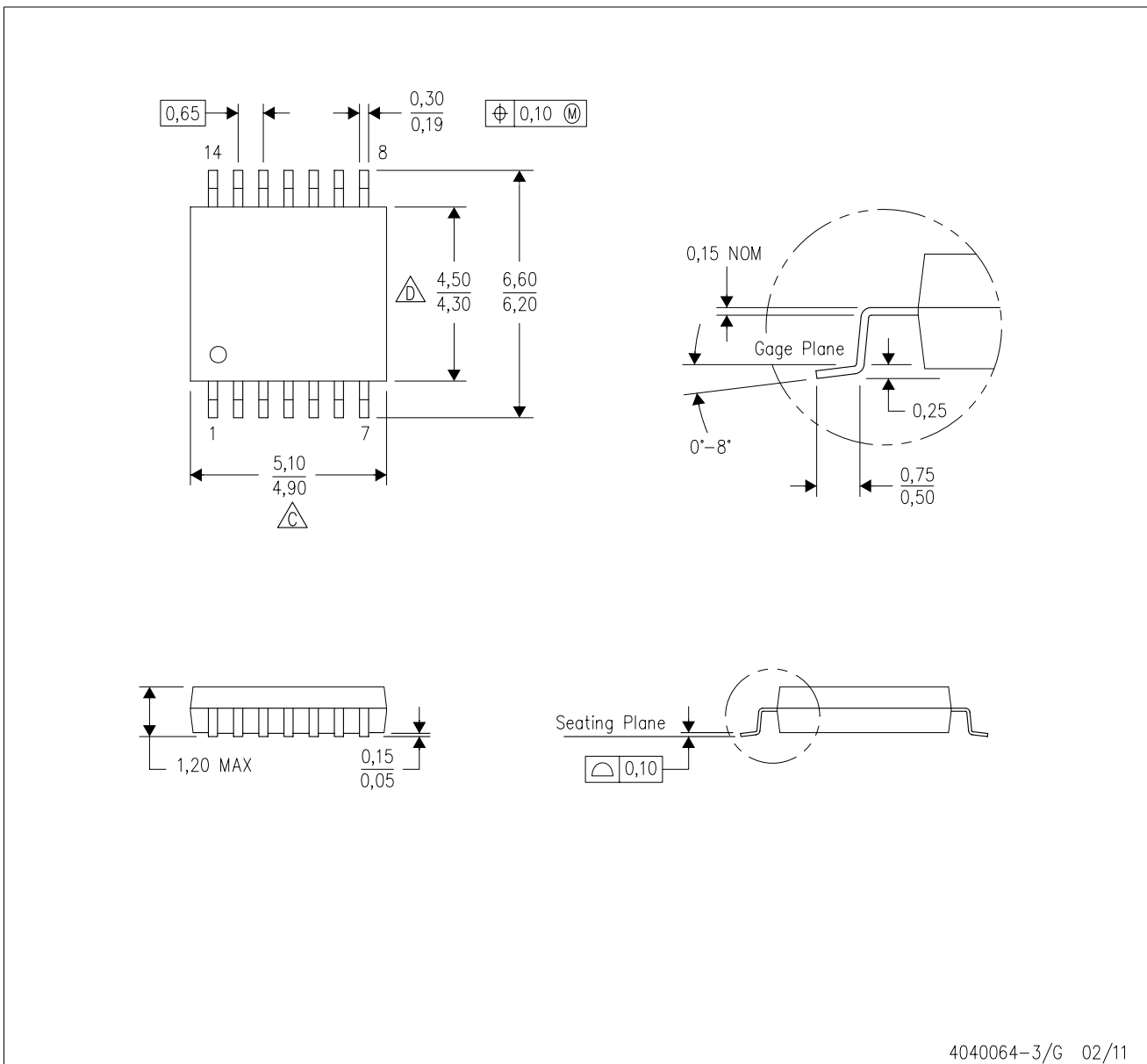

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT14QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT14QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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