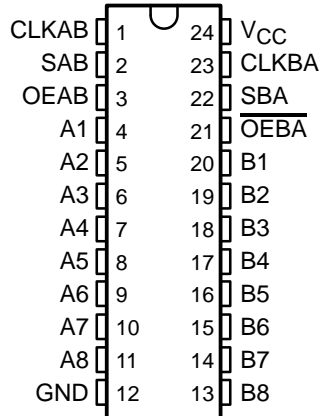


# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

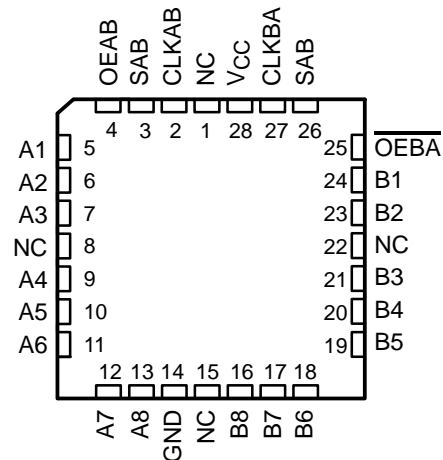
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- Operating Voltage Range of 4.5 V to 5.5 V
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- High-Current 3-State Outputs Can Drive Up To 15 LSTTL Loads

SN54HCT652 . . . JT OR W PACKAGE  
SN74HCT652 . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54HCT652 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'HCT652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and  $\overline{OEBA}$ ) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select real-time or stored data transfer. A low input level selects real-time data; a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with these devices.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – NT	Tube	SN74HCT652NT	HCT652
	SOIC – DW	Tube	SN74HCT652DW	
		Tape and reel	SN74HCT652DWR	
-55°C to 125°C	CDIP – JT	Tube	SNJ54HCT652JT	SNJ54HCT652JT
	CFP – W	Tube	SNJ54HCT652W	SNJ54HCT652W
	LCCC – FK	Tube	SNJ54HCT652FK	SNJ54HCT652FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## description/ordering information (continued)

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) terminals, regardless of the select- or output-control terminals. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{OEBA}$ . In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

To ensure the high-impedance state during power up or power down,  $\overline{OEBA}$  should be tied to  $V_{CC}$  through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

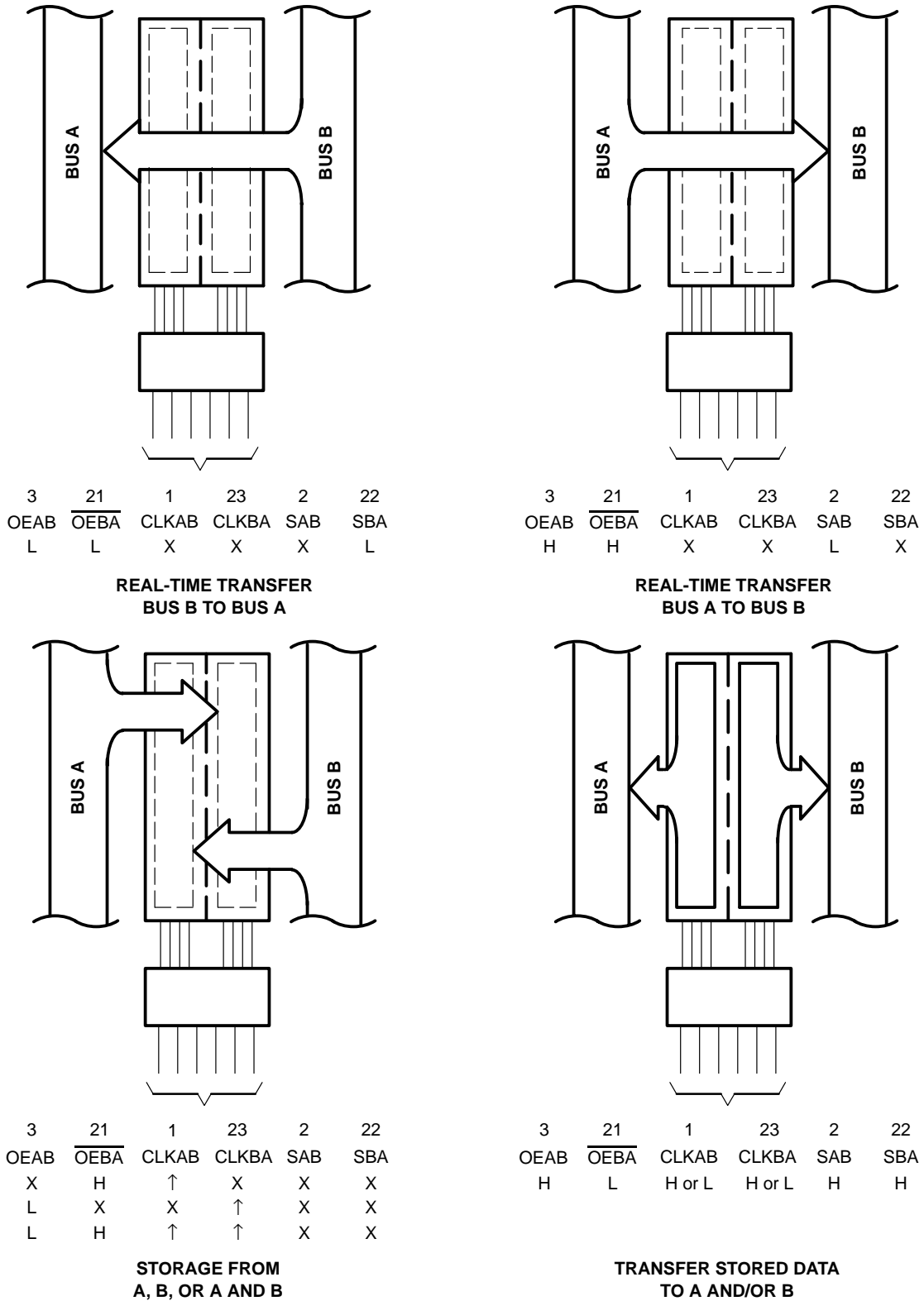
† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or  $\overline{OEBA}$ . Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered to load both registers.

# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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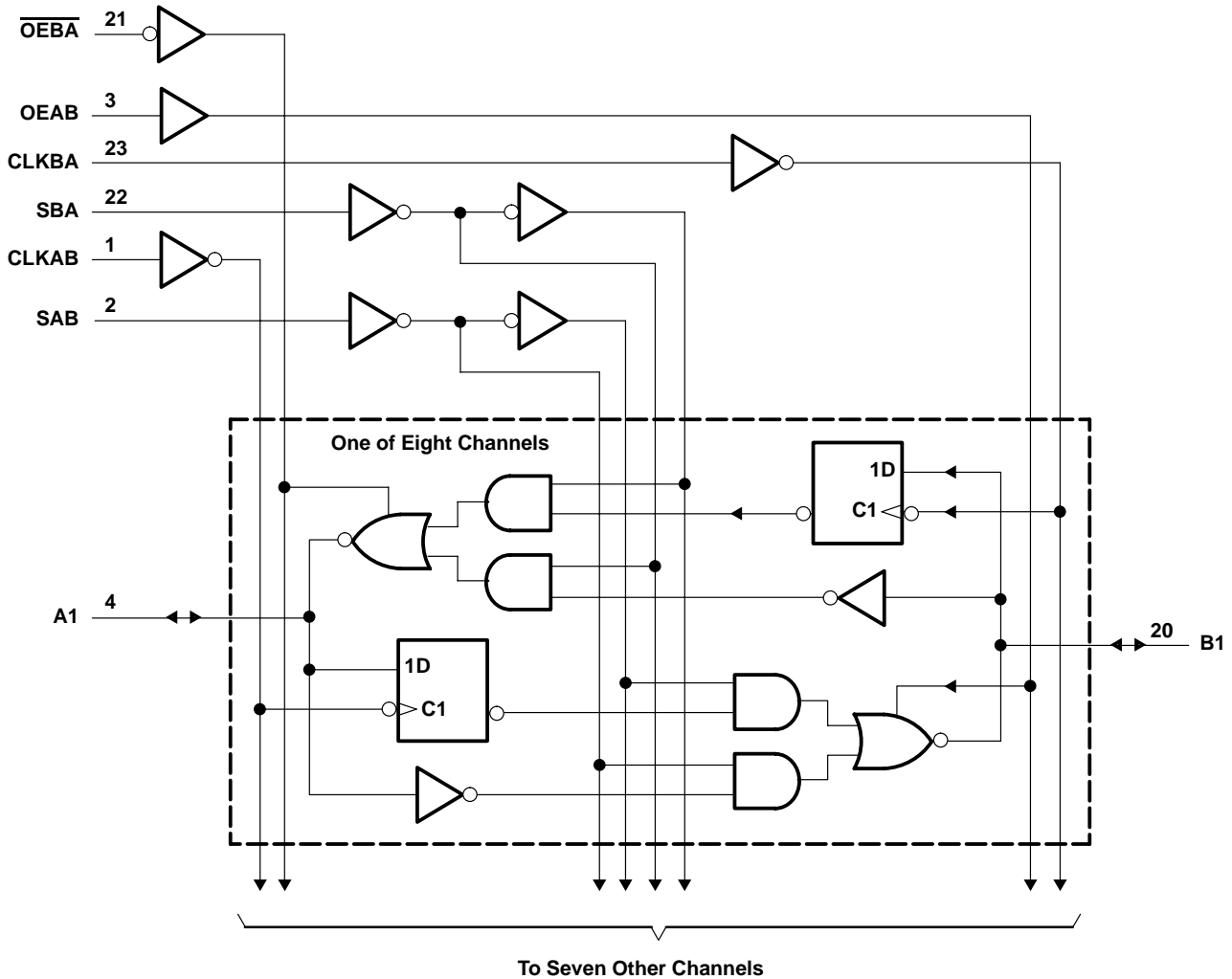
Pin numbers shown are for the DW, JT, NT, and W packages.

Figure 1. Bus-Management Functions

# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package .....	46°C/W
(see Note 3): NT package .....	67°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-3.



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# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 4)

		SN54HCT652			SN74HCT652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		2	2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V			0.8			V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
t <sub>f</sub>	Input transition (rise and fall) time	500			500			ns
T <sub>A</sub>	Operating free-air temperature	-55	125		-40	85		°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT652		SN74HCT652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA I <sub>OH</sub> = -6 mA	4.5 V	4.4	4.499	4.4	4.4		V	
			3.98	4.3	3.7	3.84			
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA I <sub>OL</sub> = 6 mA	4.5 V	0.001 0.1		0.1		0.1		V
			0.17 0.26		0.4		0.33		
I <sub>I</sub>	Control inputs V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V	±0.1	±100	±1000		±1000		nA
I <sub>OZ</sub>	A or B V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , Data = V <sub>CC</sub> or 0	5.5 V	±0.01	±0.5	±10		±5		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	5.5 V	8		160		80		μA
ΔI <sub>CC</sub> †	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5 V	1.4	2.4	3		2.9		mA
C <sub>i</sub>	Control inputs	4.5 V to 5.5 V	3	10	10		10		pF

† This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT652		SN74HCT652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	4.5 V	25		17		20		MHz
	5.5 V	28		19		22		
t <sub>w</sub>	4.5 V	20	30	25		ns		
	5.5 V	18	27	23				
t <sub>su</sub>	4.5 V	15	23	19		ns		
	5.5 V	14	21	17				
t <sub>h</sub>	4.5 V	5	5	5		ns		
	5.5 V	5	5	5				

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# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT652		SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			4.5 V	25	35		17		20	MHz	
			5.5 V	28	40		19		22		
$t_{\text{pd}}$	CLKBA or CLKAB	A or B	4.5 V		18	36		54		45	ns
			5.5 V		16	32		49		41	
	A or B	B or A	4.5 V		14	27		41		34	
			5.5 V		12	24		37		31	
	SBA or SAB†	A or B	4.5 V		20	38		57		48	
			5.5 V		17	34		51		43	
$t_{\text{en}}$	$\overline{\text{OEBA}}$ or OEAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
$t_{\text{dis}}$	$\overline{\text{OEBA}}$ or OEAB	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
$t_t$		Any	4.5 V		9	12		18		15	ns
			5.5 V		7	11		16		14	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HCT652		SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{\text{pd}}$	CLKBA or CLKAB	A or B	4.5 V		24	53		80		66	ns
			5.5 V		22	47		72		60	
	A or B	B or A	4.5 V		22	44		70		55	
			5.5 V		20	39		60		50	
	SBA or SAB†	A or B	4.5 V		26	55		83		69	
			5.5 V		24	49		74		62	
$t_{\text{en}}$	$\overline{\text{OEBA}}$ or OEAB	A or B	4.5 V		33	66		100		82	ns
			5.5 V		30	59		90		74	
$t_t$		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

† These parameters are measured with the internal output state of the storage register opposite that of the bus input.

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$ Power dissipation capacitance	No load	50	pF

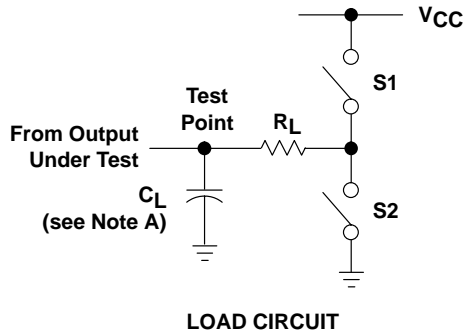
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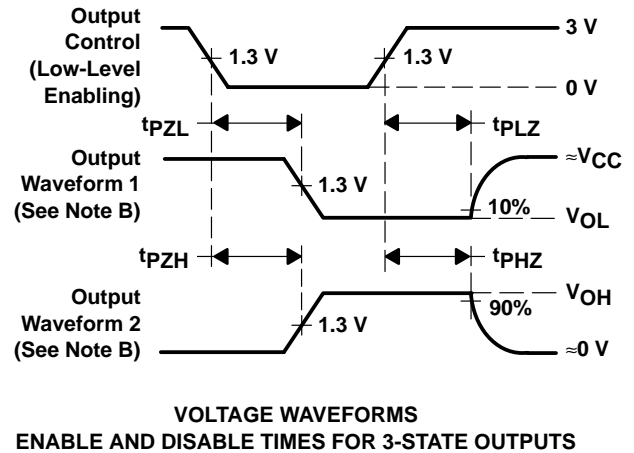
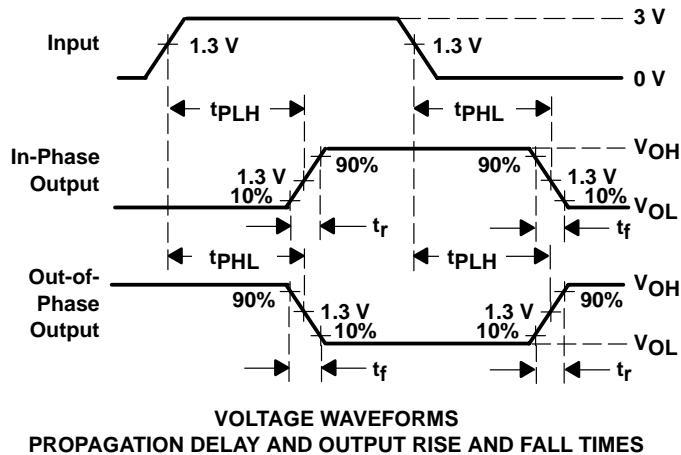
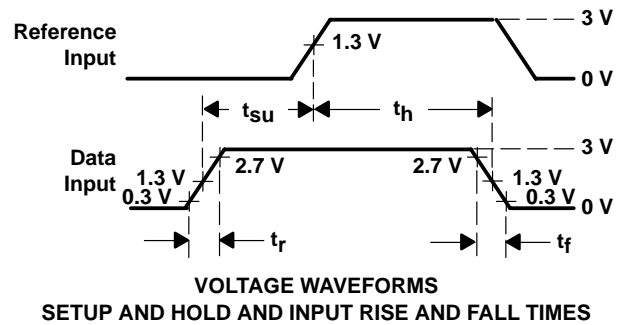
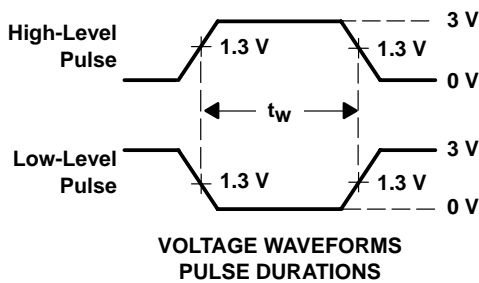
# SN54HCT652, SN74HCT652 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



PARAMETER		$R_L$	$C_L$	S1	S2
$t_{en}$	$t_{PZH}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
	$t_{PZL}$			Closed	Open
$t_{dis}$	$t_{PHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{PLZ}$			Closed	Open
$t_{pd}$ or $t_t$		—	50 pF or 150 pF	Open	Open



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT652DW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT652	<a href="#">Samples</a>
SN74HCT652DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT652	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT652DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT652DWR	SOIC	DW	24	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74HCT652DW	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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