

## SN74LV541A-Q1 具有三态输出的汽车类八路缓冲器/驱动器

### 1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：
    - 40°C 至 +125°C,  $T_A$
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 采用具有可润湿侧翼的 QFN (WRKS) 封装
- 2 V 至 5.5 V  $V_{CC}$  运行
- 最长  $t_{pd}$  : 6ns (5V 时)
- 所有端口上均支持以混合模式电压运行
- $I_{off}$  支持局部断电模式运行
- 闩锁性能超过 250mA, 符合 JESD 17 规范

### 2 应用

- 启用或禁用数字信号
- 消除缓慢或嘈杂输入信号
- 在控制器复位期间保持信号
- 对开关进行去抖

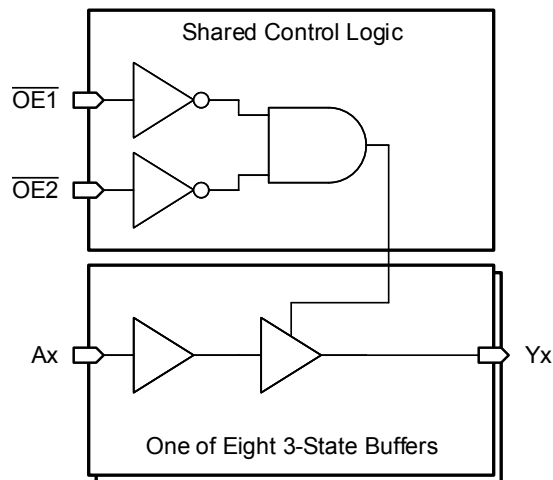
### 3 说明

SN74LV541A-Q1 器件是一款八路缓冲器/驱动器, 可在 2V 至 5.5V  $V_{CC}$  电压下运行。低电平有效输出能够使引脚 ( $\overline{OE1}$  和  $\overline{OE2}$ ) 控制所有八个通道, 并配置为使输出都必须为低电平才能有效。

#### 封装信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
SN74LV541A-Q1	WRKS (WQFN、20)	4.50mm x 2.50mm
	DGS (SOT、20)	5.10mm x 3.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



逻辑图 (正逻辑)



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## 4 Revision History

DATE	REVISION	NOTES
August 2022	*	Initial Release

## 5 Pin Configuration and Functions

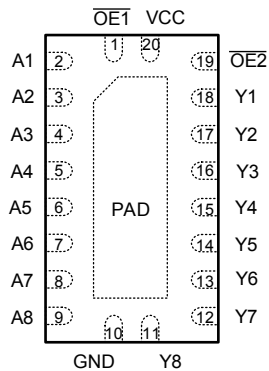


图 5-1. WRKS Package,  
20-Pin WQFN  
(Top View)

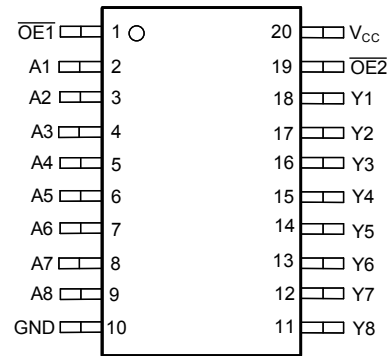


图 5-2. DGS Package,  
20-Pin SOT  
(Top View)

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
OE1	1	I	Output enable input 1, active low
A1	2	I	Input for channel 1
A2	3	I	Input for channel 2
A3	4	I	Input for channel 3
A4	5	I	Input for channel 4
A5	6	I	Input for channel 5
A6	7	I	Input for channel 6
A7	8	I	Input for channel 7
A8	9	I	Input for channel 8
GND	10	G	Ground
Y8	11	O	Output for channel 8
Y7	12	O	Output for channel 7
Y6	13	O	Output for channel 6
Y5	14	O	Output for channel 5
Y4	15	O	Output for channel 4
Y3	16	O	Output for channel 3
Y2	17	O	Output for channel 2
Y1	18	O	Output for channel 1
OE2	19	I	Output enable input 2, active low
V <sub>CC</sub>	20	P	Positive supply
Thermal Pad <sup>(2)</sup>		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) WRKS package only

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	- 0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	- 0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	- 0.5	7	V
V <sub>O</sub>	Output voltage <sup>(2)</sup> <sup>(3)</sup>	- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		- 20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		- 50 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup>	±4000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±2000

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 2.3 V to 5.5 V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 2.3 V to 5.5 V		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		-2	
		V <sub>CC</sub> = 3 V to 3.6 V		-8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		-16	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2	
		V <sub>CC</sub> = 3 V to 3.6 V		8	
		V <sub>CC</sub> = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V		200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V		100	
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LV541A-Q1		UNIT
		WRKS (WQFN)	DGS (SOT)	
		20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	86	125.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	82.6	80.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.9	63.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	9.5	8.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	54.9	79.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	32.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted).

PARAMETER			V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = - 50 mA	2 V to 5.5 V	V <sub>CC</sub> - 0.1			V
		I <sub>OH</sub> = - 2 mA	2.3 V	2			
		I <sub>OH</sub> = - 8 mA	3 V	2.48			
		I <sub>OH</sub> = - 16 mA	4.5 V	3.8			
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 50 mA	2 V to 5.5 V			0.1	V
		I <sub>OL</sub> = 2 mA	2.3 V			0.4	
		I <sub>OL</sub> = 8 mA	3 V			0.44	
		I <sub>OL</sub> = 16 mA	4.5 V			0.55	
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±1	μA
I <sub>OZ</sub>	Off-state (high- impedance state) output current	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±5	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20	μA
I <sub>off</sub>	Input/Output Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V			5	μA
C <sub>i</sub>	Input Capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		2		pF

## 6.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ± 0.2 V

over operating free-air temperature range (unless otherwise noted), (see [Fig 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			- 40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		6.7		1		13.5	ns
t <sub>en</sub>	OE	Y			8.5		1		19.5	
t <sub>dis</sub>	OE	Y			8.4		1		15	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		8.7		1		18.5	ns
t <sub>en</sub>	OE	Y			10.5		1		24	
t <sub>dis</sub>	OE	Y			12.3		1		20	
t <sub>sk(o)</sub>							2		2	

## 6.7 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over operating free-air temperature range (unless otherwise noted), (see [Fig 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			- 40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF		4.8	7	1		8.5	ns
t <sub>en</sub>	OE	Y			6.1	10.5	1		12.5	
t <sub>dis</sub>	OE	Y			5.8	11	1		12	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF		6.1	10.5	1		12	ns
t <sub>en</sub>	OE	Y			7.4	14	1		16	
t <sub>dis</sub>	OE	Y			8.8	15.4	1		17.5	
t <sub>sk(o)</sub>							1.5		1.5	

## 6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over operating free-air temperature range (unless otherwise noted), (see 图 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	25°C			-40°C to 125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{pd}$	A	Y	$C_L = 15\text{ pF}$		3.5	5	1		6	ns
$t_{en}$	OE	Y	$C_L = 15\text{ pF}$		4.3	7.2	1		8.5	
$t_{dis}$	OE	Y	$C_L = 15\text{ pF}$		3.9	7.5	1		8	
$t_{pd}$	A	Y	$C_L = 50\text{ pF}$		4.3	7	1		8	ns
$t_{en}$	OE	Y	$C_L = 50\text{ pF}$		5.3	9.2	1		10.5	
$t_{dis}$	OE	Y	$C_L = 50\text{ pF}$		5.6	8.8	1		10	
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1			1	

## 6.9 Noise Characteristics<sup>(1)</sup>

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	DESCRIPTION	SN74LV541A-Q1			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.4	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

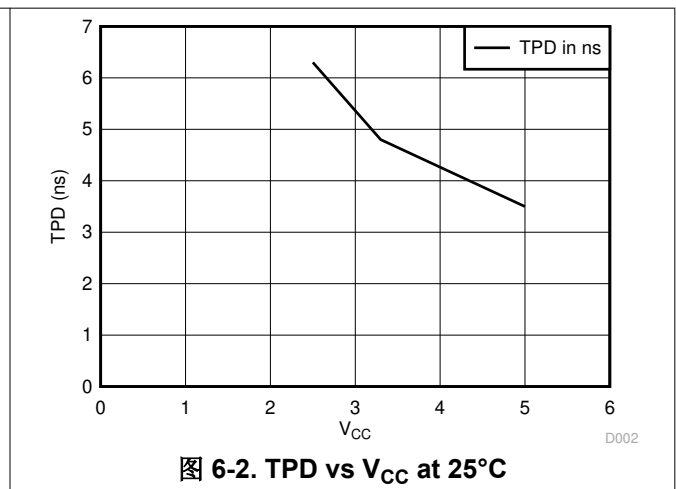
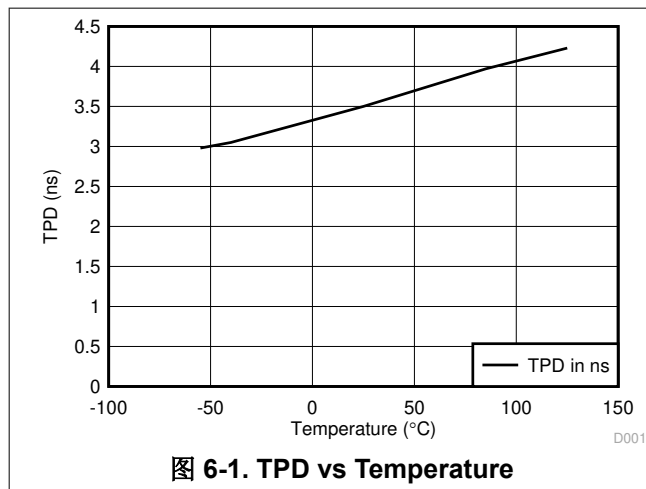
(1) Characteristics are for surface-mount packages only.

## 6.10 Operating Characteristics

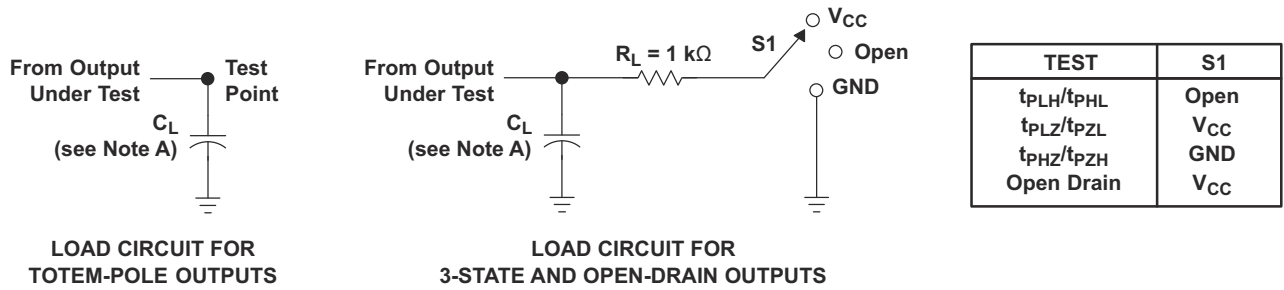
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ $f = 10\text{ MHz}$	3.3 V	16.3	pF
		5 V	17.8	

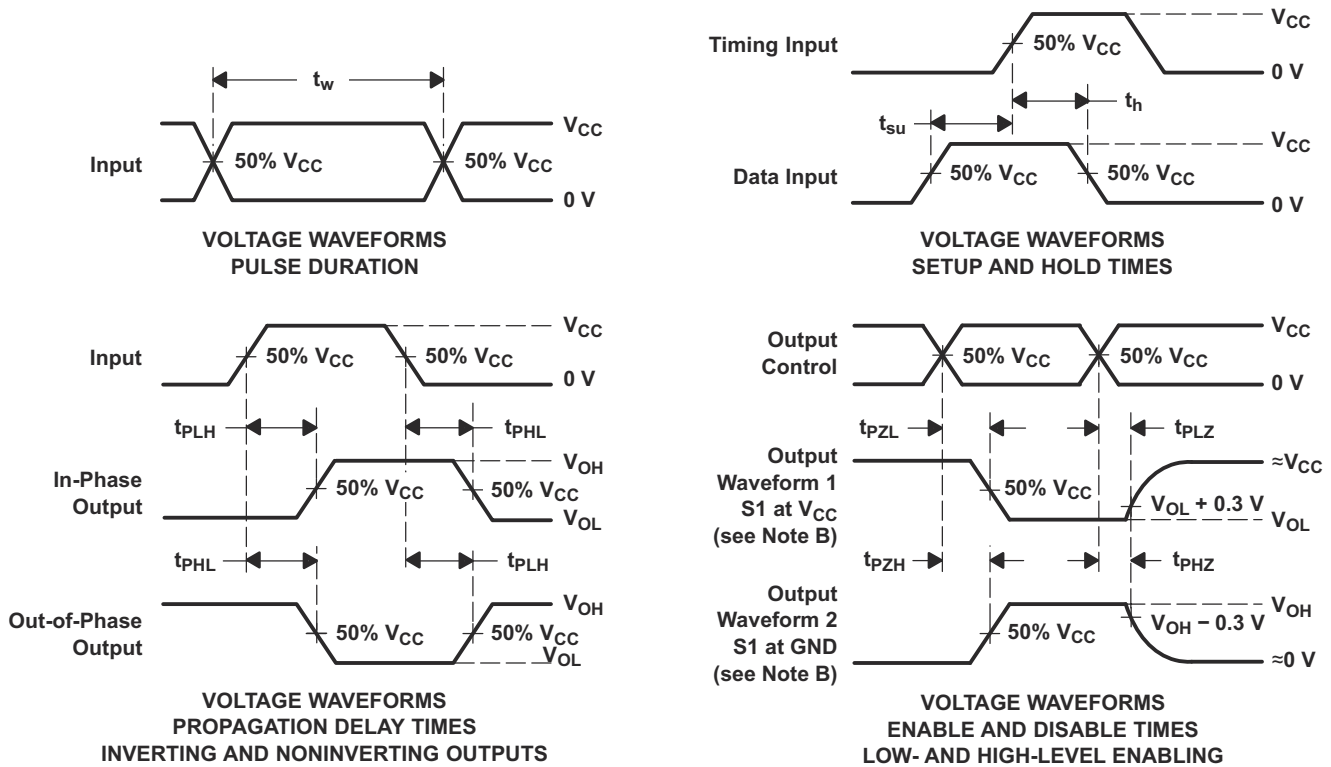
## 6.11 Typical Characteristics



## 7 Parameter Measurement Information



ADVANCE INFORMATION



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \ \Omega$ ,  $t_r \leq 3 \text{ ns}$ , and  $t_f \leq 3 \text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms



## 8 Detailed Description

### 8.1 Overview

The SN74LV541A-Q1 device is an octal buffer/driver designed for 2 V to 5.5 V  $V_{CC}$  operation.

The active low output enable pins ( $\overline{OE1}$  and  $\overline{OE2}$ ) control all eight channels, and are configured so that both must be low for the outputs to be active. When the outputs are enabled, the outputs are actively driving low or high. When the outputs are disabled, the outputs are set into the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### 8.2 Functional Block Diagram

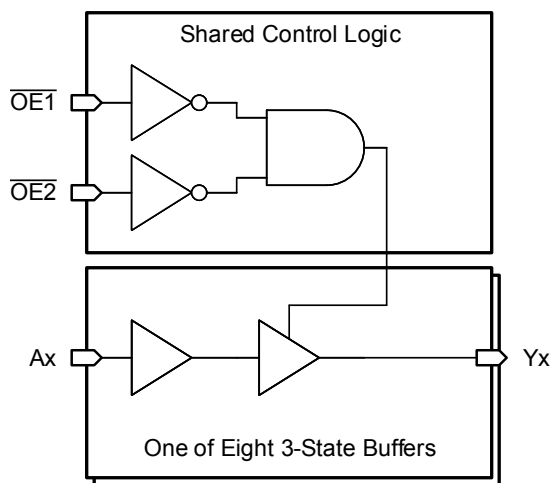


图 8-1. Logic Diagram (Positive Logic)

### 8.3 Feature Description

#### 8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-k $\Omega$  resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

#### 8.3.2 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

### 8.3.3 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

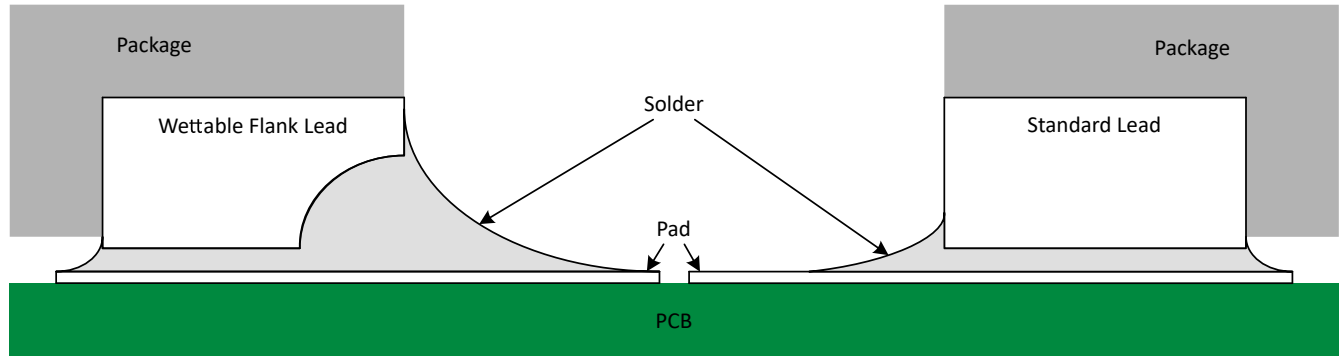


图 8-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in 图 8-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. Please see the mechanical drawing for additional details.

### 8.3.4 Clamp Diode Structure

图 8-3 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

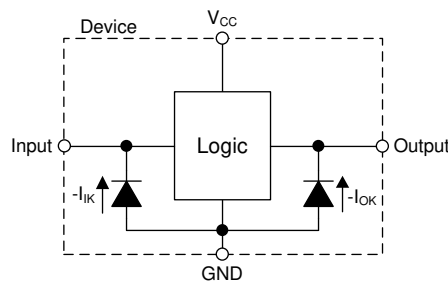


图 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

## 8.4 Device Functional Modes

表 8-1. Function Table

INPUTS <sup>(1)</sup>			OUTPUT <sup>(2)</sup>
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

(1) L = input low, H = input high, X = do not care

(2) L = output low, H = output high, Z = high impedance

**ADVANCE INFORMATION**

## 9 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LV541A-Q1 can be used to drive signals over relatively long traces or transmission lines. In order to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The figure in the *Application Curve* section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

### 9.2 Typical Application

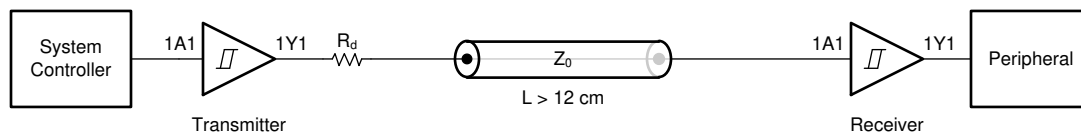


图 9-1. Input Expansion with Shift Registers

#### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV541A-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV541A-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV541A-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV541A-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

**CAUTION**

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

**9.2.2 Input Considerations**

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV541A-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k $\Omega$  resistor value is often used due to these factors.

The SN74LV541A-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

**9.2.3 Output Considerations**

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

### 9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50$  pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV541A-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)}) \Omega$ . This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

### 9.2.5 Application Curves

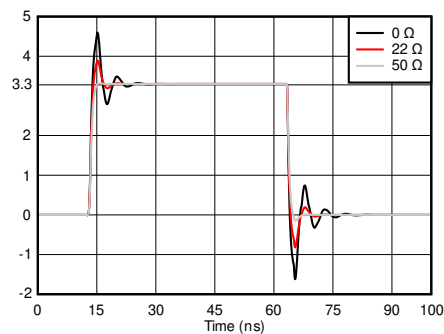


图 9-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor ( $R_d$ ) Values

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* section. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- $\mu$ F capacitor; if there are multiple  $V_{CC}$  terminals, then TI recommends a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

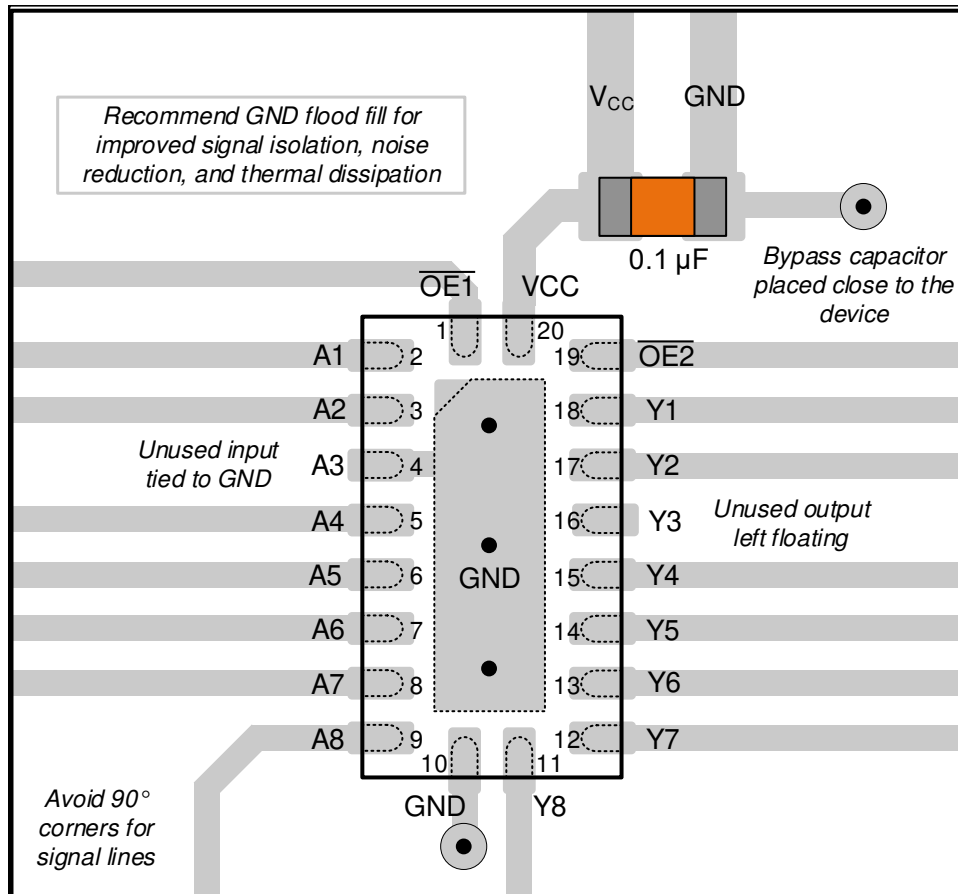


图 11-1. Layout Example for the SN74LV541A-Q1 in the WRKS Package

## 12 Device and Documentation Support

### 12.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Power-Up Behavior of Clocked Devices](#)
- Texas Instruments, [Introduction to Logic](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](#). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



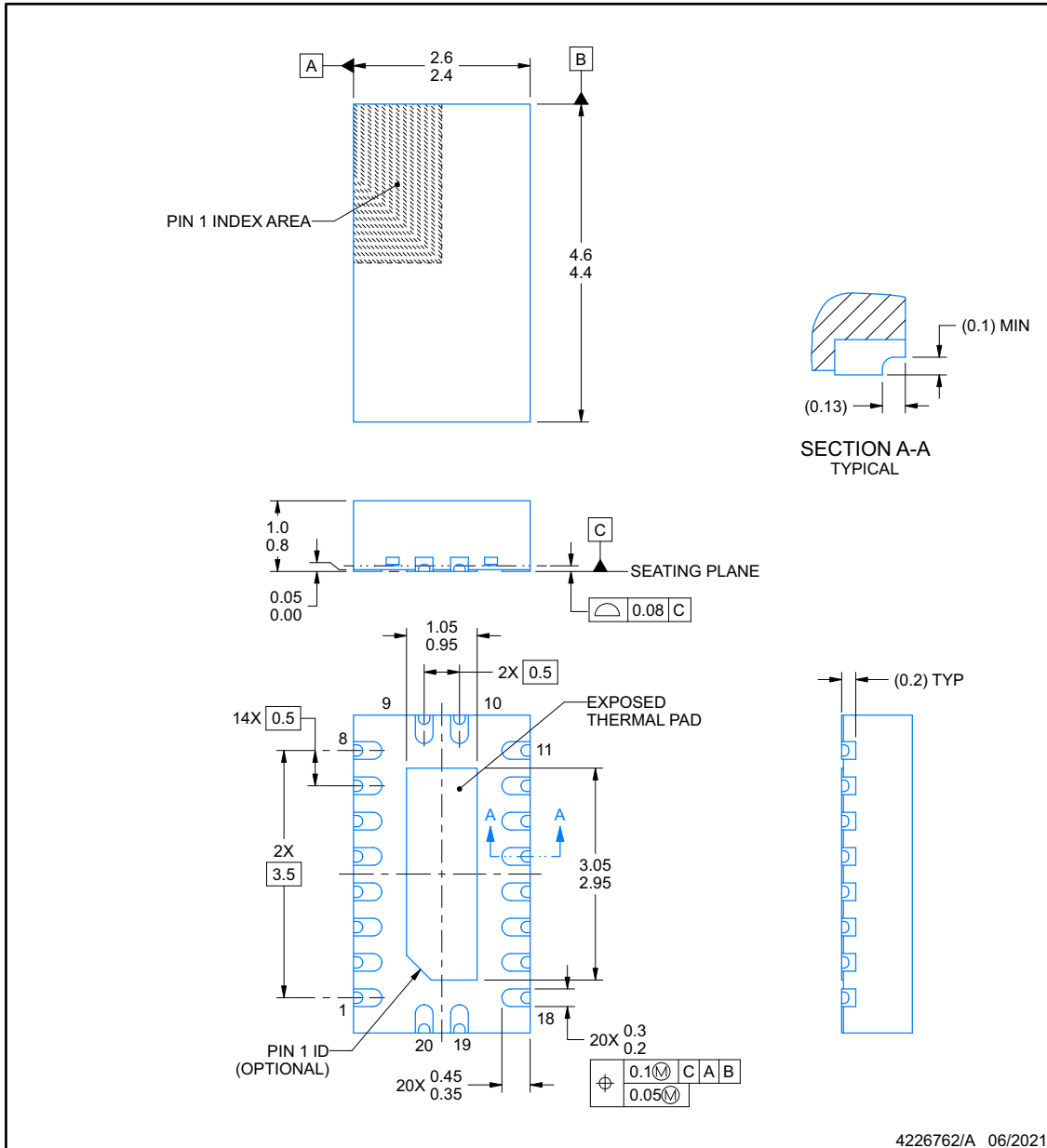


**RKS0020B**

**PACKAGE OUTLINE**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**ADVANCE INFORMATION**

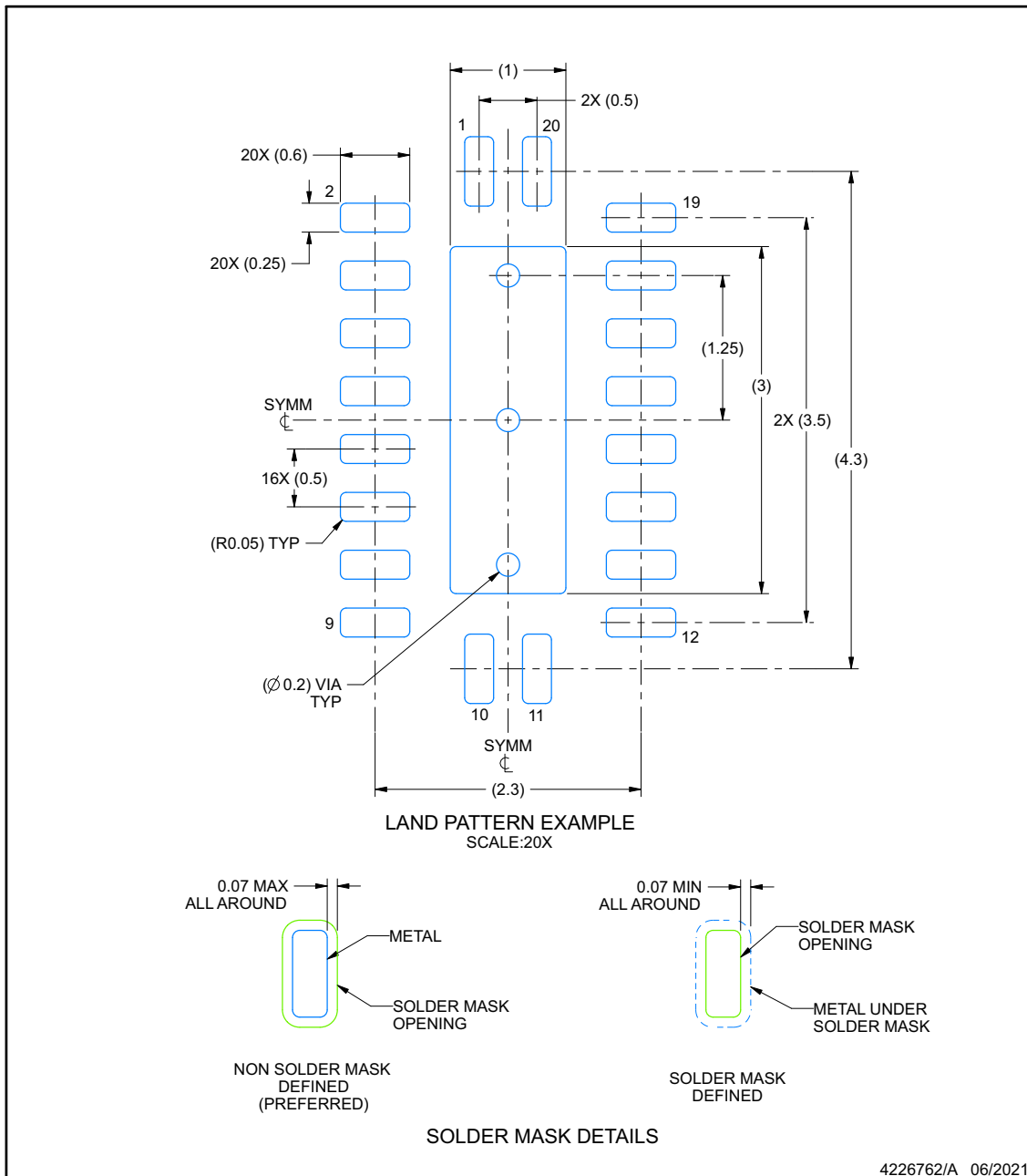
## EXAMPLE BOARD LAYOUT

**RKS0020B**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

**ADVANCE INFORMATION**



NOTES: (continued)

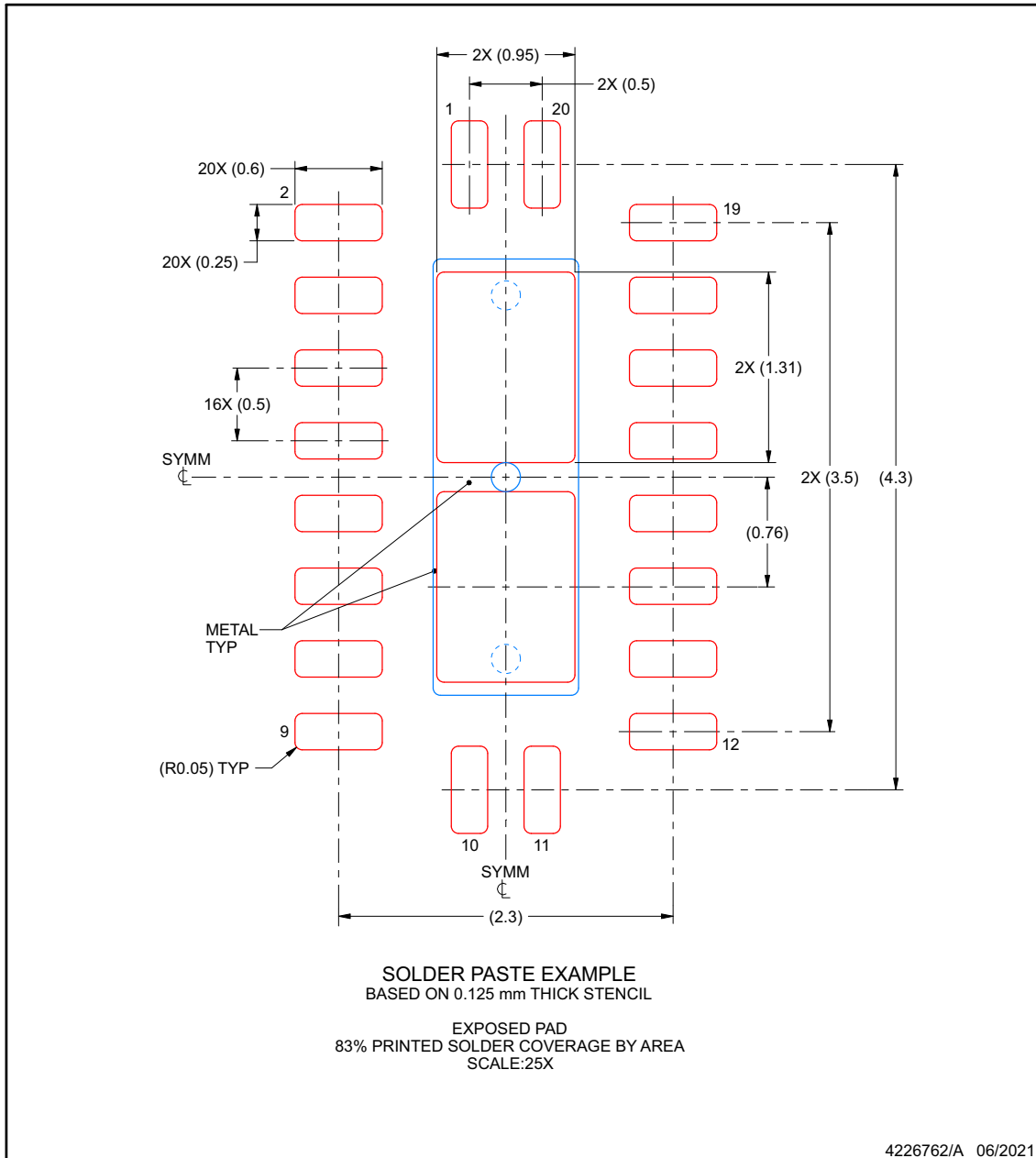
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

## EXAMPLE STENCIL DESIGN

**RKS0020B**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

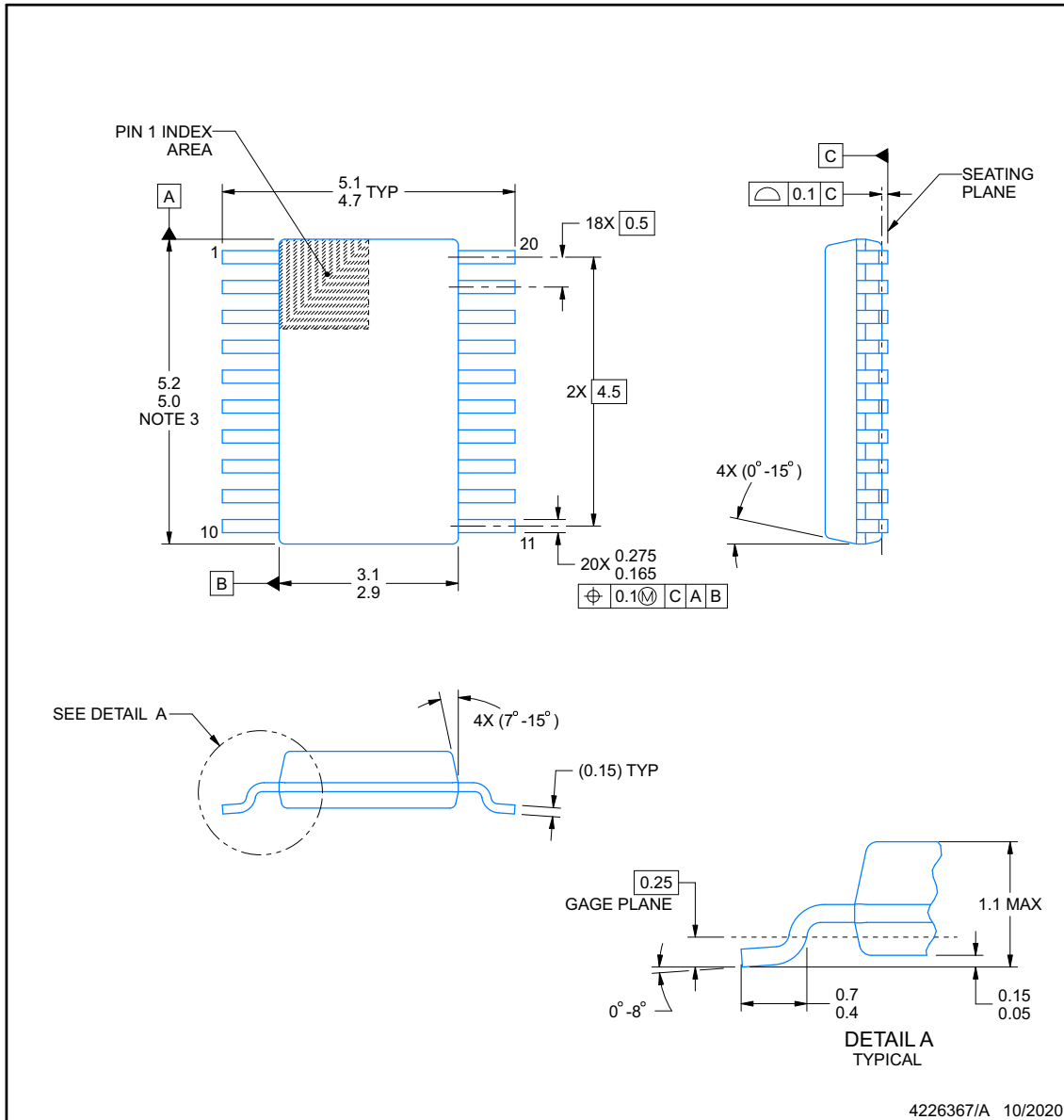
**ADVANCE INFORMATION**

**DGS0020A**



**PACKAGE OUTLINE**  
**VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

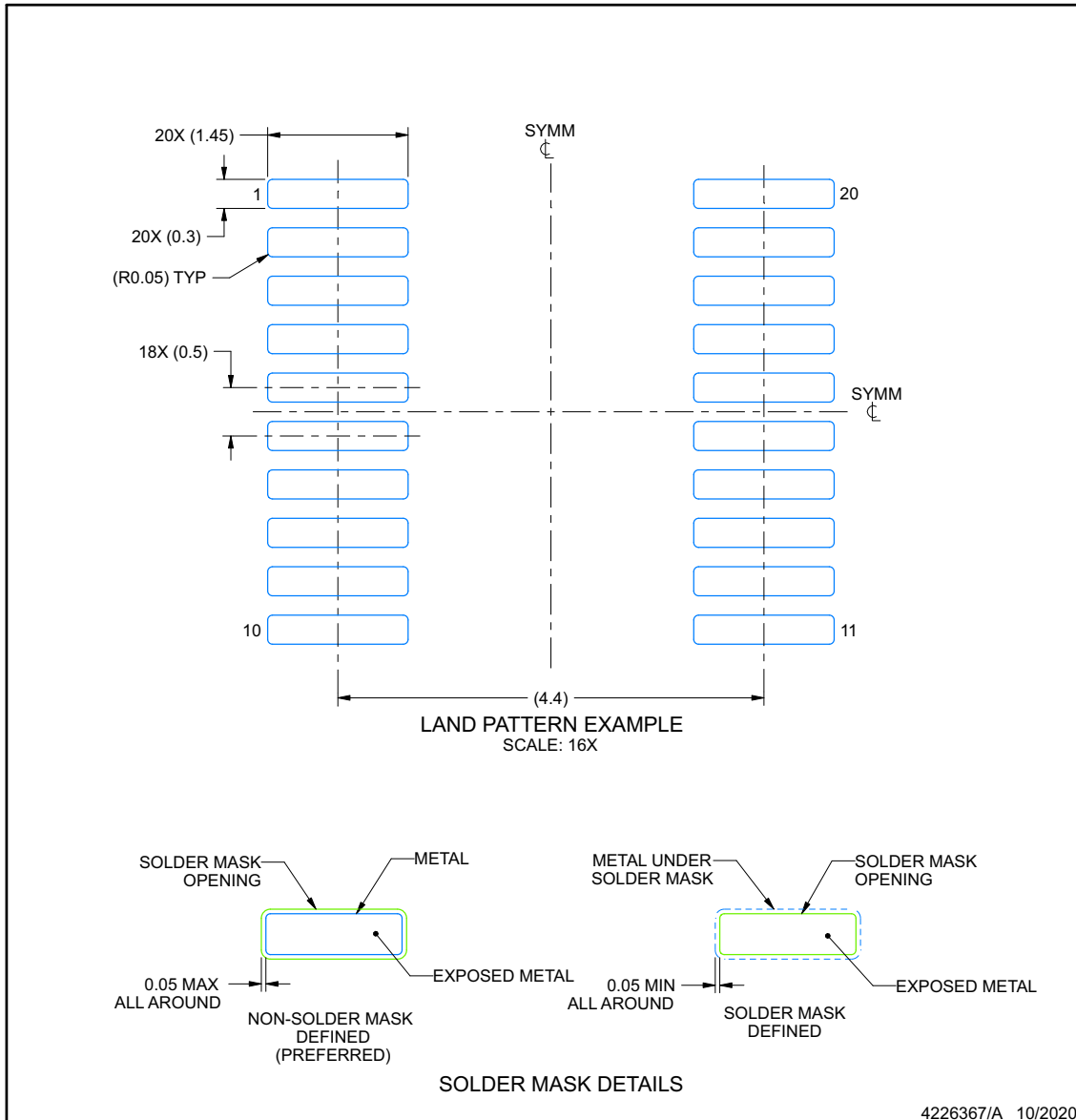
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

## EXAMPLE BOARD LAYOUT

**DGS0020A**

**VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

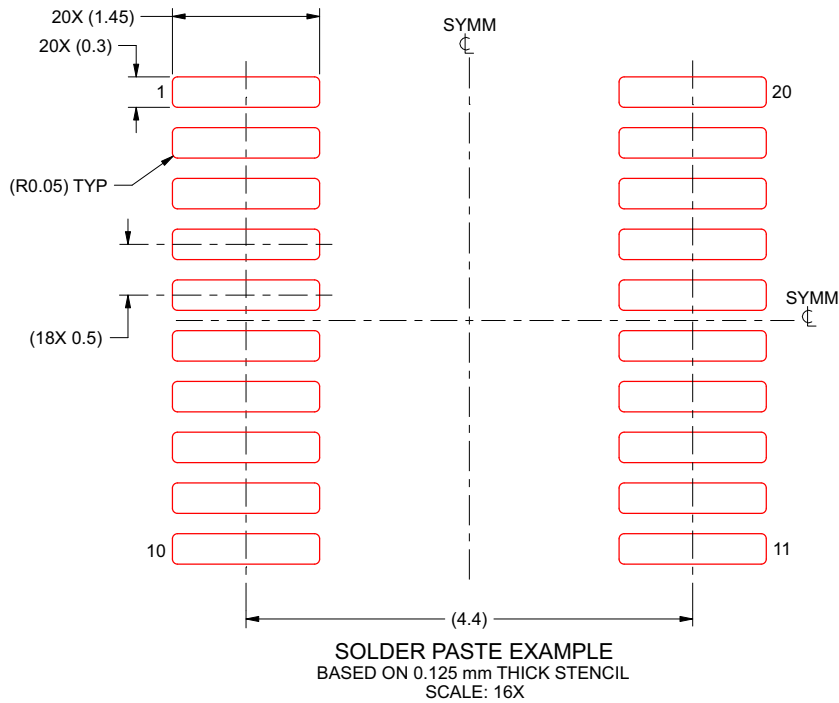
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



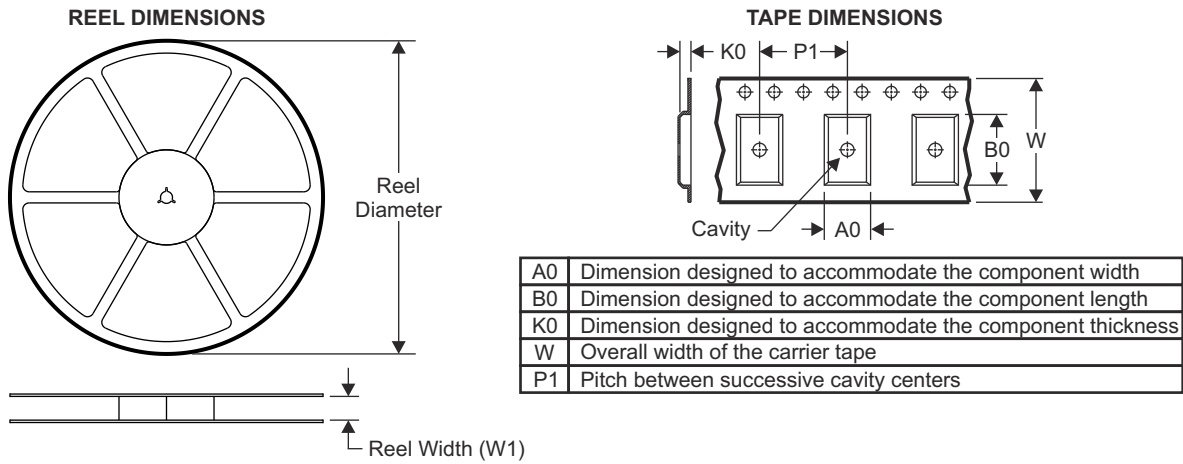
4226367/A 10/2020

NOTES: (continued)

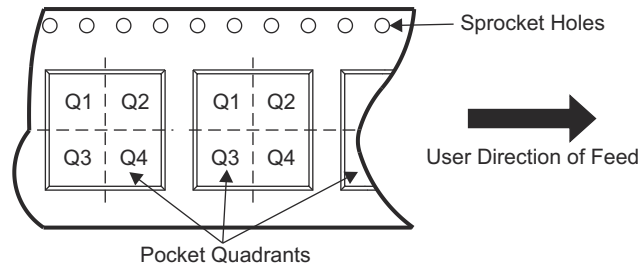
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

### 13.1 Tape and Reel Information



#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



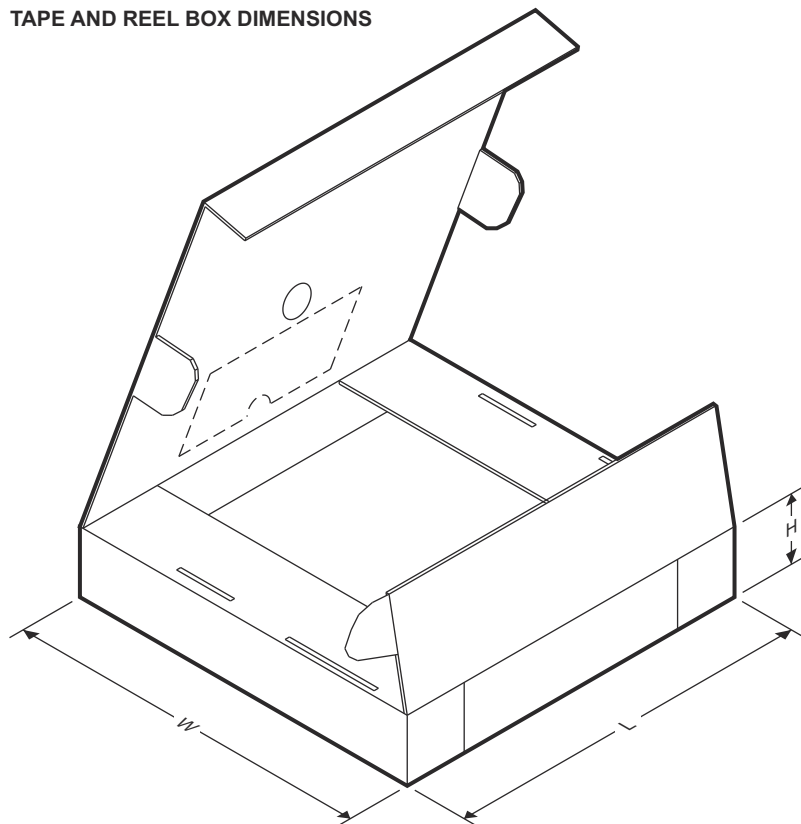
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV541AQWRKSR Q1	WQFN	RKS	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV541AQDGSRQ 1	SOT	DGS	20	2000	330	16.4	5.40	5.40	1.45	8	16	Q1

**ADVANCE INFORMATION**

**SN74LV541A-Q1**

ZHCSQX0 - AUGUST 2022

**TAPE AND REEL BOX DIMENSIONS**



**ADVANCE INFORMATION**

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV541AQWRKSRQ1	WQFN	RKS	20	3000	210.0	185.0	35.0
SN74LV541AQDGSRQ1	SOT	DGS	20	2000	356.0	356.0	35.0



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCLV541AQDGSRQ1	ACTIVE	VSSOP	DGS	20	5000	TBD	Call TI	Call TI	-40 to 125		Samples
PCLV541AQWRKSRQ1	ACTIVE	VQFN	RKS	20	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LV541A-Q1 :**

- Catalog : [SN74LV541A](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## GENERIC PACKAGE VIEW

**RKS 20**

**VQFN - 1 mm max height**

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226872/A

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