- **Meet or Exceed the Requirements of ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noise Environments**
- **Driver Positive- and Negative-Current Limiting**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs**
- **Receiver Common-Mode Input Voltage Range of –12 V to 12 V**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Hysteresis . . . 50 mV Typ**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver 3-State Outputs (SN751177 Only)**
- **Operate From Single 5-V Supply**

SN751177 . . . N OR NS† PACKAGE
(TOP VIEW)

1B	1	16	V_{CC}
1A	2	15	1D
1R	3	14	1Y
$\overline{RE}$	4	13	1Z
2R	5	12	DE
2A	6	11	2Z
2B	7	10	2Y
GND	8	9	2D

SN751178 . . . N OR NS† PACKAGE
(TOP VIEW)

1B	1	16	V_{CC}
1A	2	15	1D
1R	3	14	1Y
1DE	4	13	1Z
2R	5	12	2DE
2A	6	11	2Z
2B	7	10	2Y
GND	8	9	2D

† The NS package is only available taped and reeled.
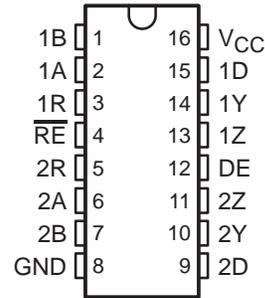
description

The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 Mbit/s. They are designed to improve the performance of full-duplex data communications over long bus lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.10 and V.11.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal-shutdown protection from line-fault conditions on the transmission bus line.
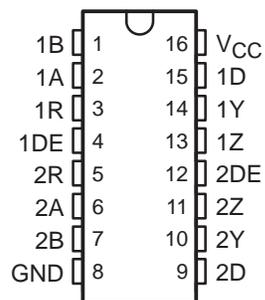
The receiver features high input impedance of at least 12 kΩ, an input sensitivity of ±200 mV over a common-mode input voltage range of –12 V to 12 V, and typical input hysteresis of 50 mV. Fail-safe design ensures that if the receiver inputs are open, the receiver outputs always will be high.

The SN751177 and SN751178 are characterized for operation from –20°C to 85°C.

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![TEXAS INSTRUMENTS]

Function Tables

SN751177, SN751178
(each driver)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN751177
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{\text{RE}}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

SN751178
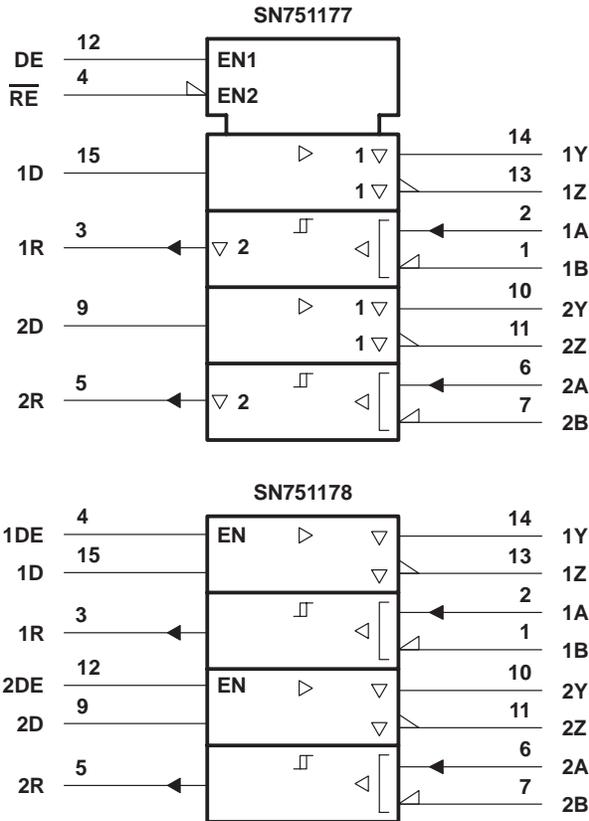**(each receiver)**

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L

H = high level, L = low level,
? = indeterminate

![Texas Instruments logo]

logic symbols†

SN751177

SN751178

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN751177

SN751178

schematics of inputs

EQUIVALENT OF DRIVER OR ENABLE INPUT	EQUIVALENT OF RECEIVER INPUT

Driver Input: $R_{(eq)}$ = 6 kΩ NOM
Enable Input: $R_{(eq)}$ = 4 kΩ NOM
$R_{(eq)}$ = Equivalent Resistor
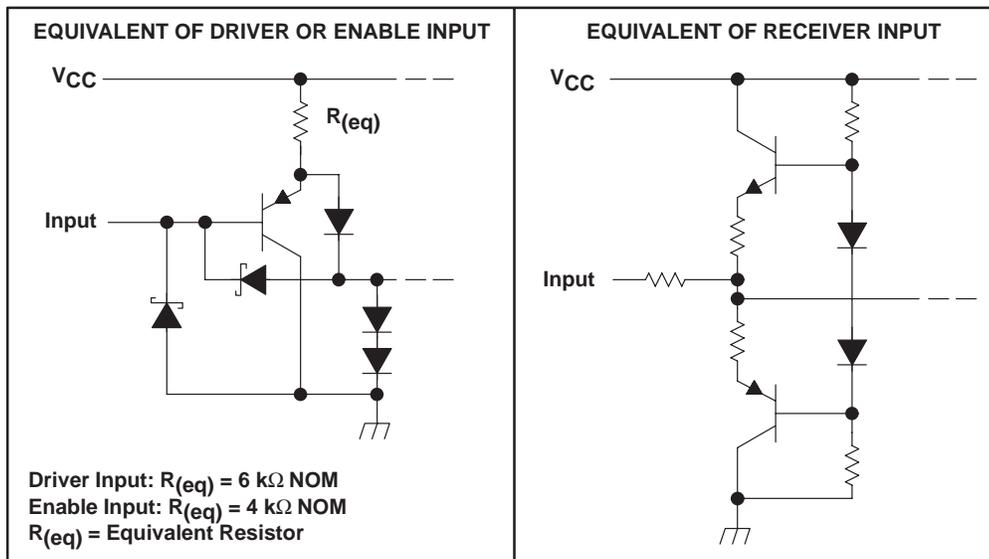
All resistor values are nominal.

SN751177, SN751178
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

schematics of outputs

| TYPICAL OF ALL DRIVER OUTPUTS | TYPICAL OF ALL RECEIVER OUTPUTS |
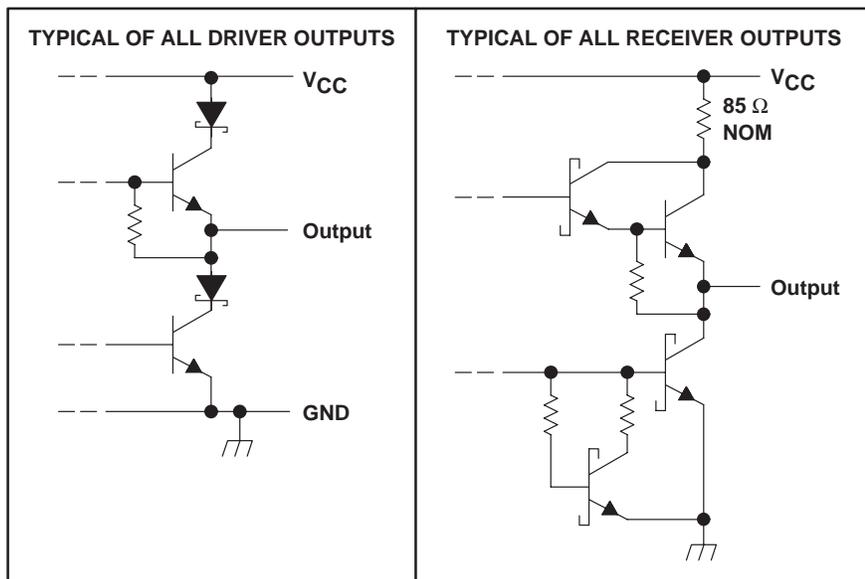
All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage, V_I (DE, $\overline{RE}$, and D inputs) . . . . 7 V
Receiver input voltage range, V_I (A or B inputs) . . . . −25 V to 25 V
Receiver differential input voltage range, V_{ID} (see Note 2) . . . . −25 V to 25 V
Driver output voltage range, V_O . . . . −10 V to 15 V
Receiver low-level output current, I_{OL} . . . . 50 mA
Package thermal impedance, θ_{JA} (see Note 3): N package . . . . 78°C/W
NS package . . . . 111°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace
length of zero.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, and D inputs	2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}	Driver	-7†		12	V
High-level output current, I_{OH}				-60	mA
Low-level output current, I_{OL}				60	mA
Common-mode input voltage, V_{IC}	Receiver			±12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}				-400	µA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		-20		85	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

DRIVER SECTIONS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{IH} = 2$ V, $\quad$ $V_{IL} = 0.8$ V, $\quad$ $I_{OH} = -33$ mA			3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V, $\quad$ $V_{IL} = 0.8$ V, $\quad$ $I_{OH} = 33$ mA			1.1		V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$		1.5		6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100$ Ω, $\quad$ See Figure 1		2 or $\frac{1}{2}$ V_{OD1}‡			V
		$R_L = 54$ Ω, $\quad$ See Figure 1		1.5		5	
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta|V_{OD}|$	Change in magnitude of differential output voltage (see Note 5)	$R_L = 54$ Ω or 100 Ω, $\quad\quad$ See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage			−1§		3	V
$\Delta|V_{OC}|$	Change in magnitude of common-mode output voltage (see Note 5)					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$, $\quad$ $V_O = -7$ V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	µA
I_{IH}	High-level input current	$V_{IH} = 2.7$ V				20	µA
I_{IL}	Low-level input current	$V_{IL} = 0.4$ V				−100	µA
I_{OS}	Short-circuit output current (see Note 6)	$V_O = -7$ V				−250	mA
		$V_O = V_{CC}$				250	
		$V_O = 12$ V				250	
I_{CC}	Supply current	No load	Outputs enabled		80	110	mA
			Outputs disabled		50	80	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°$C.
‡ The minimum V_{OD2} with a 100-Ω load is either $\frac{1}{2}$ V_{OD1} or 2 V, whichever is greater.
§ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
NOTES: 4. See TIA/EIA-485-A Figure 3.5, Test Termination Measurement 2
5. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics at $V_{CC} = 5$ V, $C_L = 50$ pF, $T_A = 25°$C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54$ Ω, $\quad$ See Figure 3			20	25	ns
$t_{t(OD)}$	Differential output transition time				27	35	ns
t_{PLH}	Propagation delay time, low- to high-level output	$R_L = 27$ Ω, $\quad$ See Figure 4			20	25	ns
t_{PHL}	Propagation delay time, high- to low-level output				20	25	ns
t_{PZH}	Output enable time to high level	$R_L = 110$ Ω, $\quad$ See Figure 5			80	120	ns
t_{PZL}	Output enable time to low level	$R_L = 110$ Ω, $\quad$ See Figure 6			40	60	ns
t_{PHZ}	Output disable time from high level	$R_L = 110$ Ω, $\quad$ See Figure 5			90	120	ns
t_{PLZ}	Output disable time from low level	$R_L = 110$ Ω, $\quad$ See Figure 6			30	45	ns

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SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
$|V_{OD1}|$	V_O	V_O
$|V_{OD2}|$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$|V_{OD3}|$		V_t (Test Termination Measurement 2)
$\Delta|V_{OD}|$	$||V_t| - |\overline{V}_t||$	$||V_t| - |\overline{V}_t||$
V_{OC}	$|V_{OS}|$	$|V_{OS}|$
$\Delta|V_{OC}|$	$|V_{OS} - \overline{V}_{OS}|$	$|V_{OS} - \overline{V}_{OS}|$
I_{OS}	$|I_{sal}|, |I_{sb}|$	
I_O	$|I_{xal}|, |I_{xb}|$	I_{ia}, I_{ib}

RECEIVER SECTIONS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		$V_O = 2.7$ V,	$I_O = -0.4$ mA			0.2	V
V_{IT-}	Negative-going input threshold voltage		$V_O = 0.5$ V,	$I_O = 16$ mA	-0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IK}	Enable clamp voltage	SN751177	$I_I = -18$ mA				-1.5	V
V_{OH}	High-level output voltage		$V_{ID} = 200$ mV,	$I_{OH} = -400\ \mu$A	2.7			V
V_{OL}	Low-level output voltage		$V_{ID} = -200$ mV	$I_{OL} = 8$ mA			0.45	V
				$I_{OL} = 16$ mA			0.5	
I_{OZ}	High-impedance-state output current	SN751177	$V_O = 0.4$ V to 2.4 V				±20	μA
I_I	Line input current (see Note 7)		Other input at 0 V	$V_I = 12$ V			1	mA
				$V_I = -7$ V			-0.8	
I_{IH}	High-level enable input current	SN751177	$V_{IH} = 2.7$ V				20	μA
I_{IL}	Low-level enable input current	SN751177	$V_{IL} = 0.4$ V				-100	μA
I_{OS}	Short-circuit output current (see Note 6)				-15		-85	μA
I_{CC}	Supply current		No load,	Outputs enabled		80	110	mA
r_i	Input resistance				12			kΩ

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°$C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.
NOTES: 6.   Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
         7.   Refer to ANSI Standards TIA/EIA-422-B, TIA/EIA-423-A, and TIA/EIA-485-A for exact conditions.

SN751177, SN751178
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

switching characteristics at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 7			20	35	ns
t_{PHL}	Propagation delay time, high- to low-level output				22	35	ns
t_{PZH}	Output enable time to high level	SN751177	See Figure 8		17	25	ns
t_{PZL}	Output enable time to low level				20	27	ns
t_{PHZ}	Output disable time from high level				25	40	ns
t_{PLZ}	Output disable time from low level				30	40	ns

PARAMETER MEASUREMENT INFORMATION
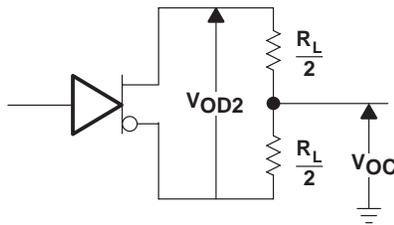
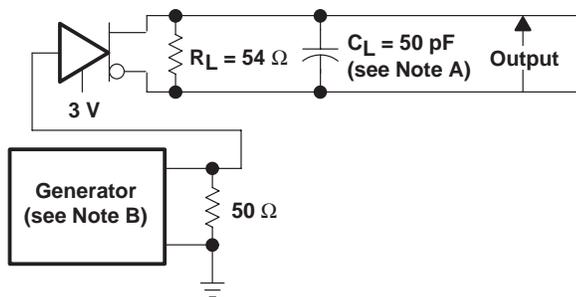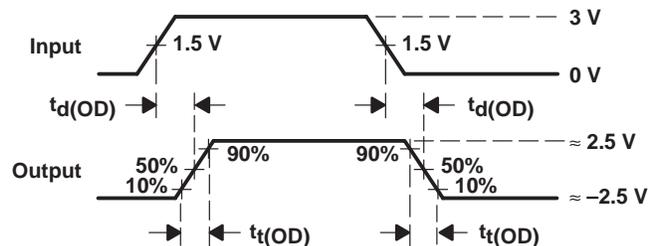Figure 1. Driver Test Circuit, V_{OD} and V_{OC}
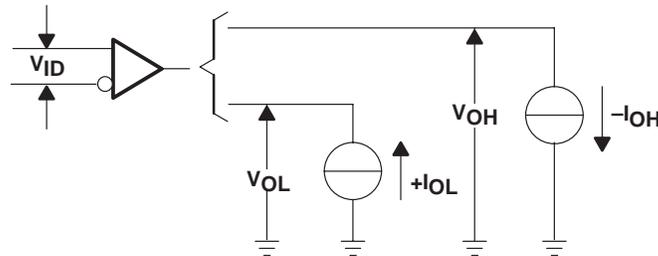
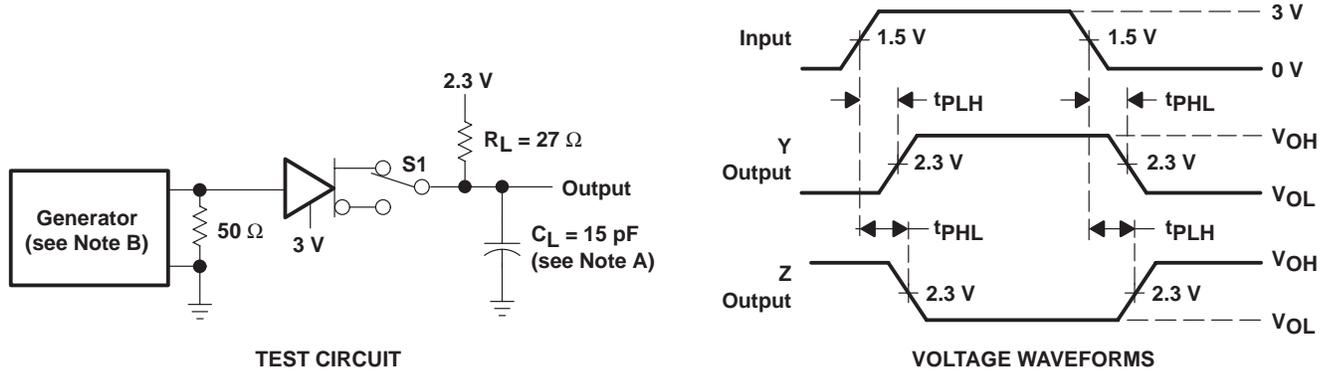Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.

Figure 3. Driver Differential Output-Delay and Transition-Time Test Circuit and Voltage Waveforms

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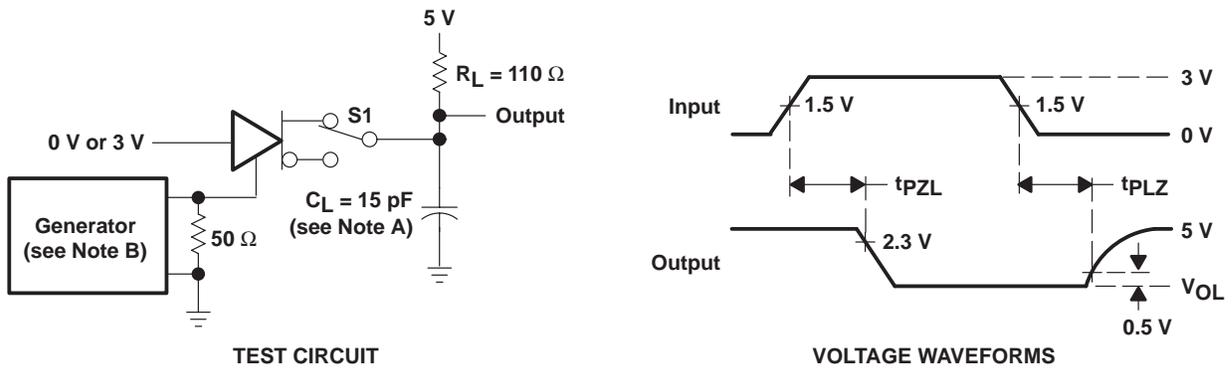## PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.

Figure 4. Driver Propagation-Time Test Circuit and Voltage Waveforms
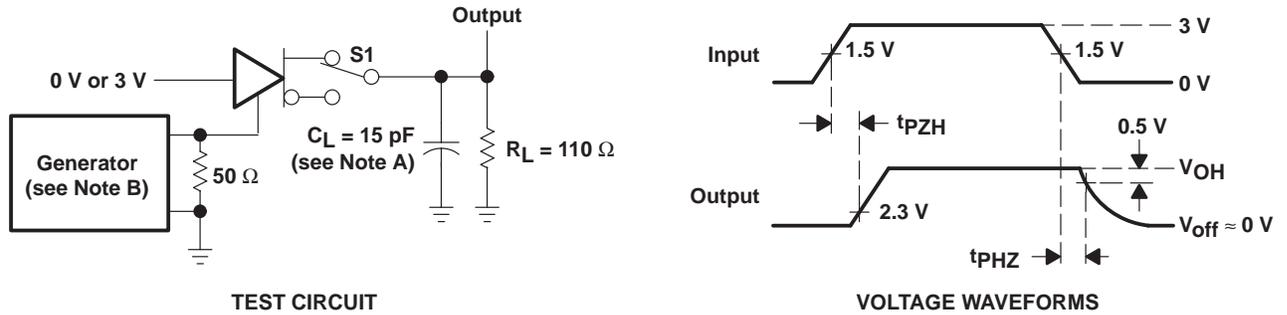
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.

Figure 5. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms
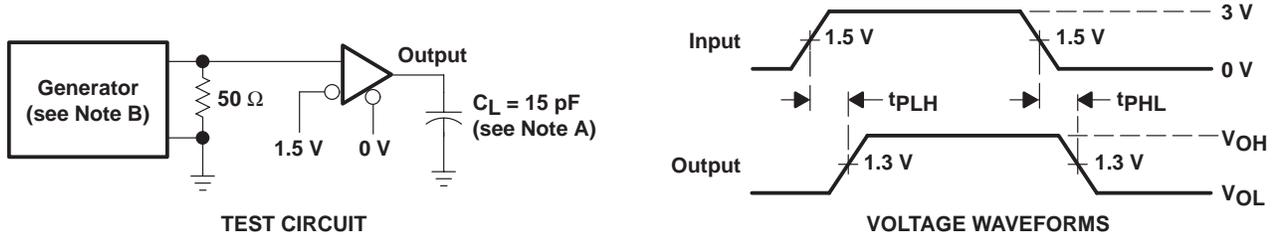

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.

Figure 6. Driver Enable- and Disable-Time Test Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, Z_O = 50 Ω, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns.

Figure 7. Receiver Propagation-Time Test Circuit and Voltage Waveforms
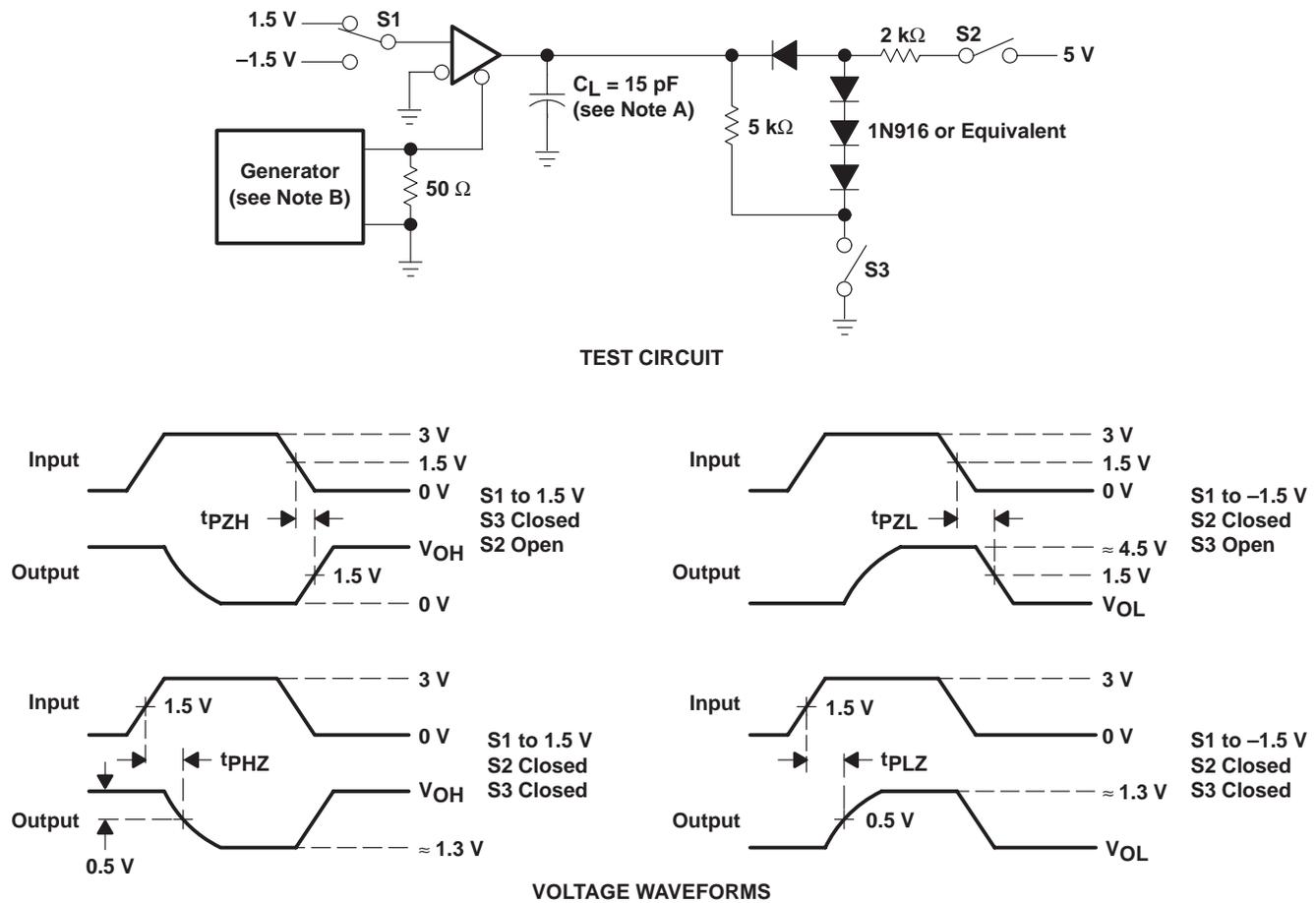
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, Z_O = 50 Ω, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns.

Figure 8. Receiver Output Enable- and Disable-Time Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN751177N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 85	SN751177N	Samples
SN751177NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751177	Samples
SN751177NSRE4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751177	Samples
SN751178N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-20 to 85	SN751178N	Samples
SN751178NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN751178	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
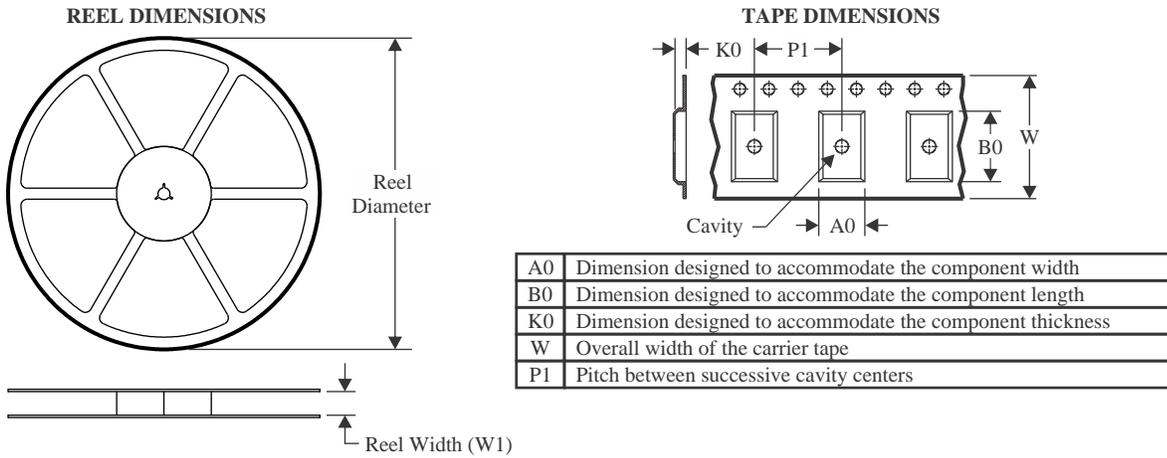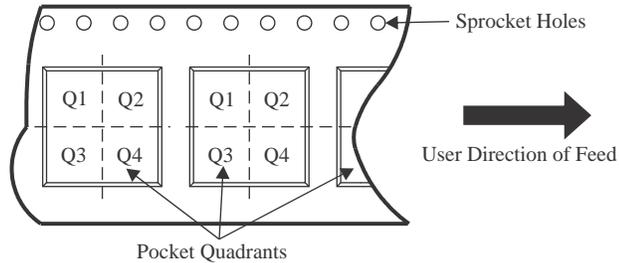
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN751177NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN751178NSR	SO	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN751177NSR	SO	NS	16	2000	356.0	356.0	35.0
SN751178NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
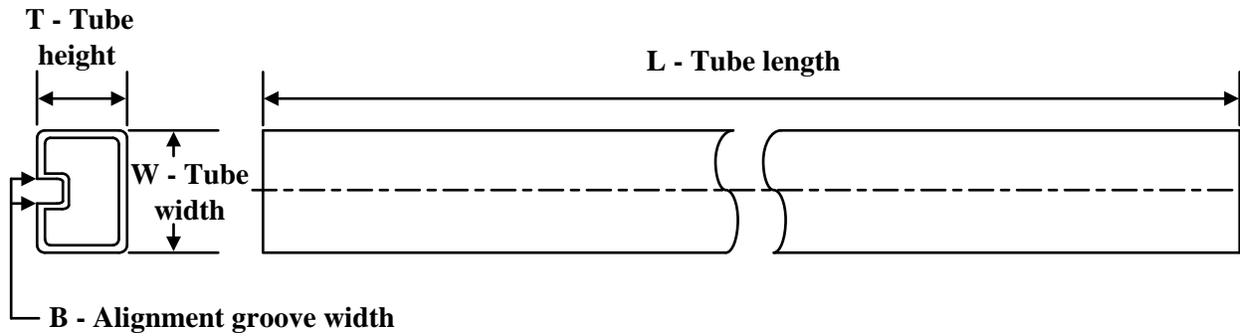
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN751177N	N	PDIP	16	25	506	13.97	11230	4.32
SN751177N	N	PDIP	16	25	506	13.97	11230	4.32
SN751178N	N	PDIP	16	25	506	13.97	11230	4.32
SN751178N	N	PDIP	16	25	506	13.97	11230	4.32

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03
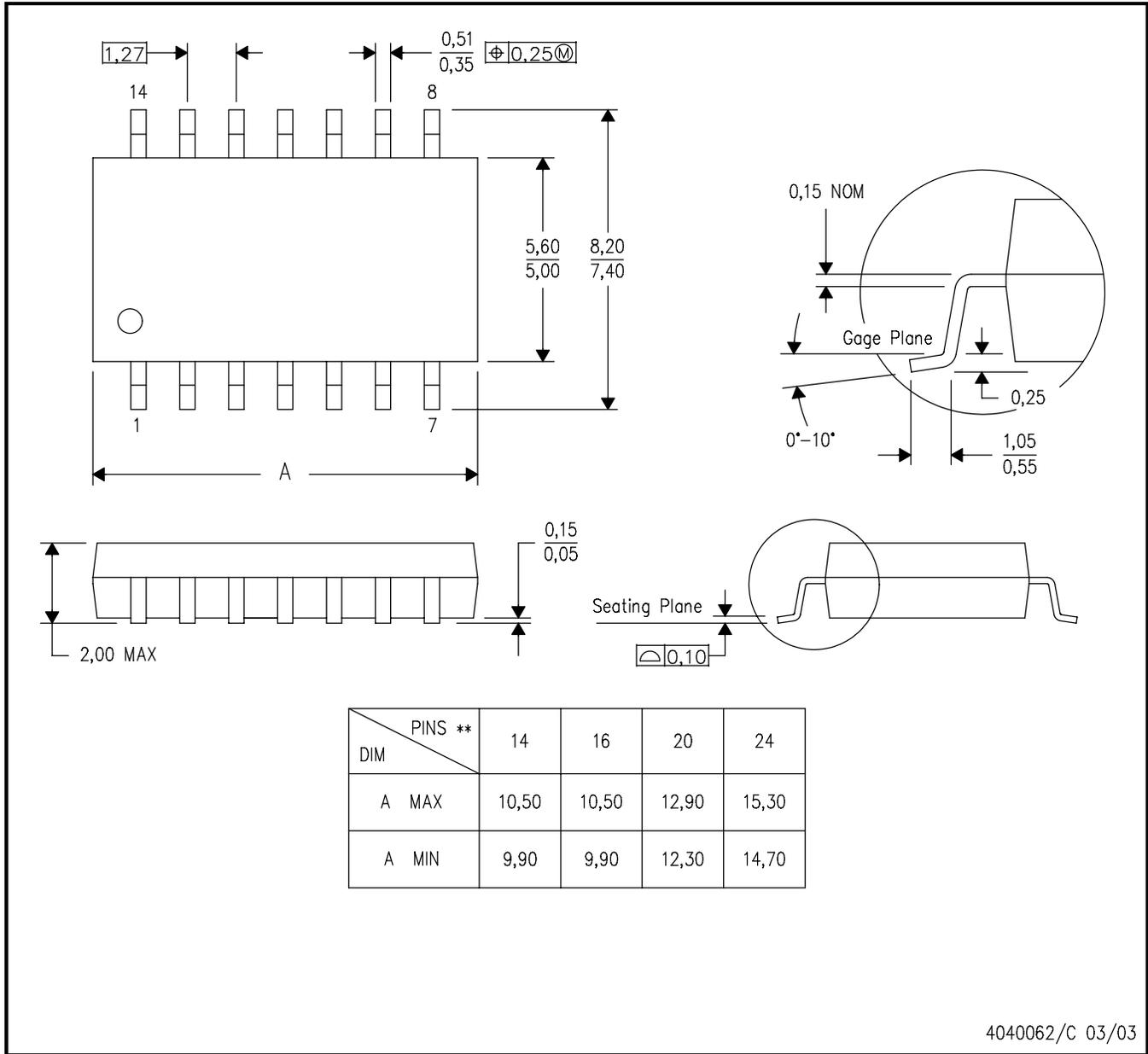
NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
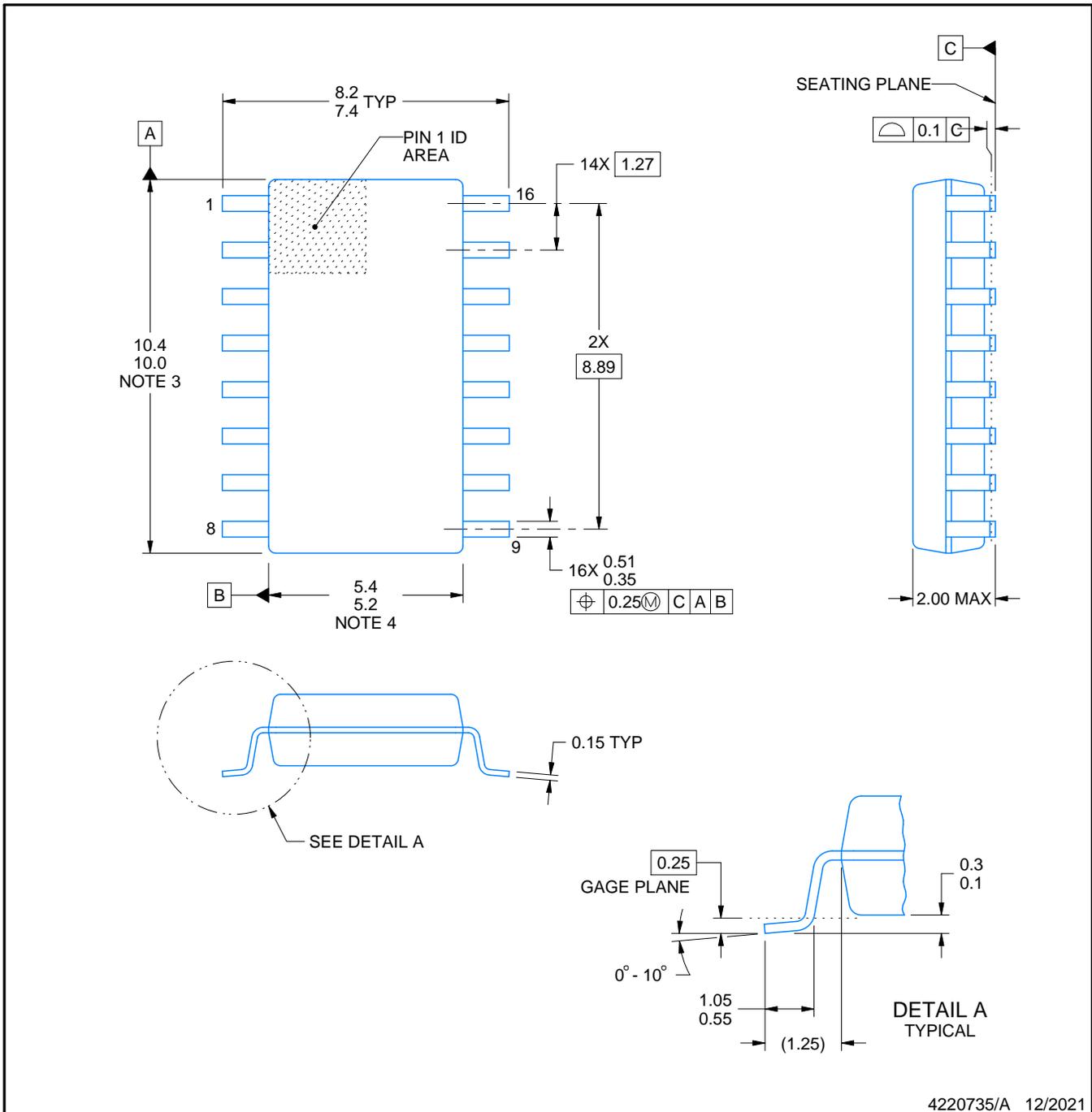   C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

C

SEATING PLANE

0.1 | C

8.2 / 7.4 TYP

A

PIN 1 ID AREA

14X 1.27

1

16

2X 8.89

10.4 / 10.0 NOTE 3

8

9

16X 0.51 / 0.35

⊕ | 0.25 Ⓜ | C | A | B

B

5.4 / 5.2 NOTE 4

2.00 MAX

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0.3 / 0.1

0° - 10°

1.05 / 0.55

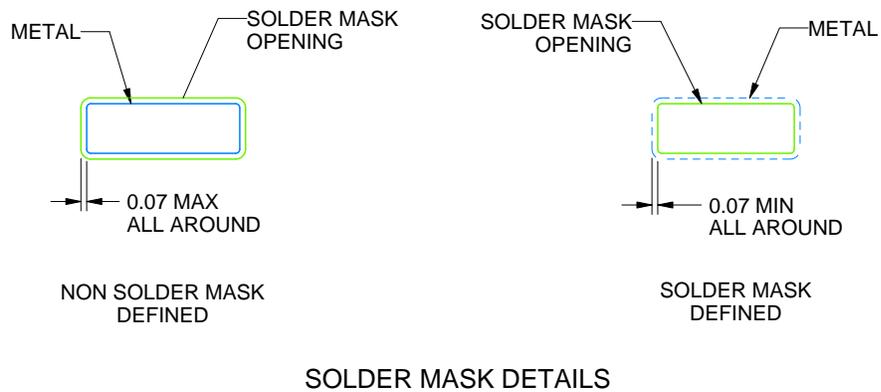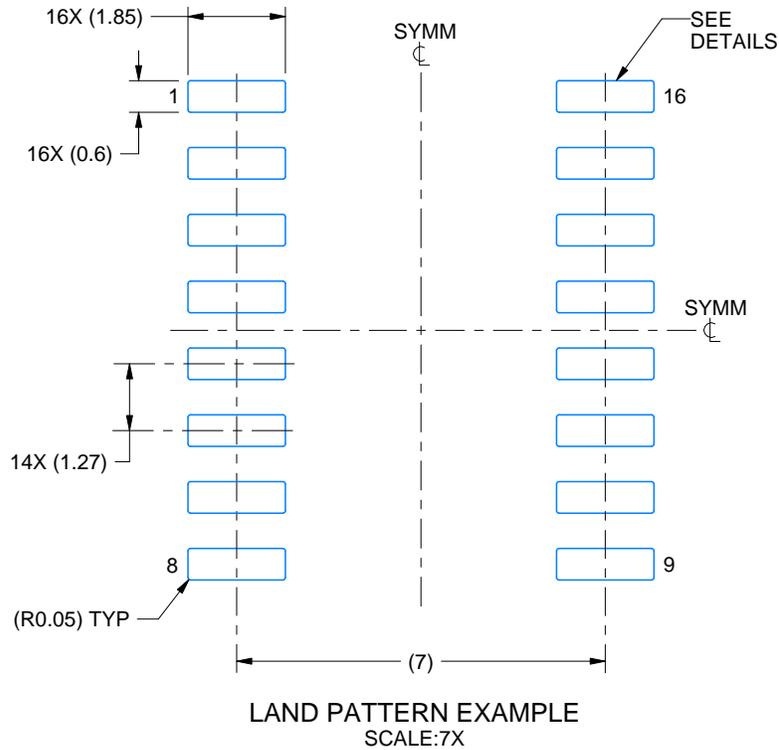(1.25)

DETAIL A
TYPICAL

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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM

SEE DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
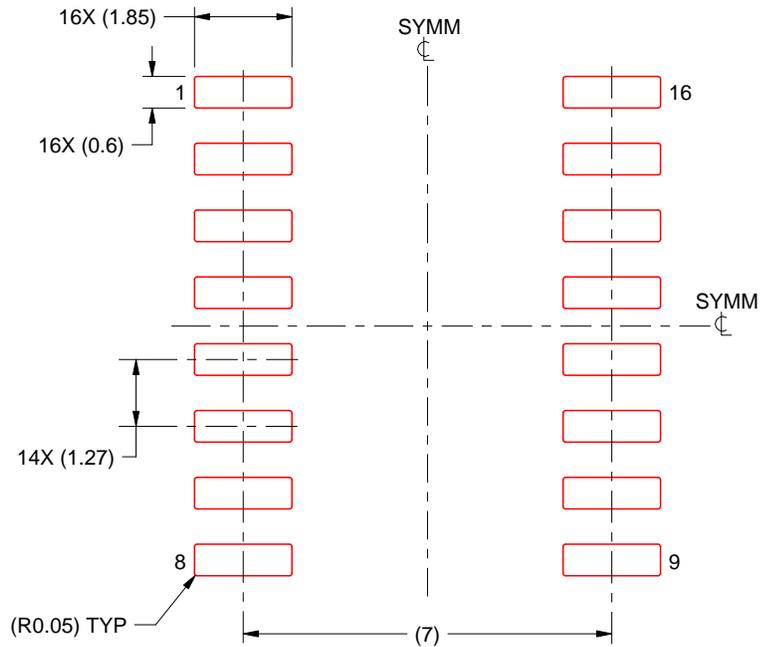
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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.85)

SYMM

1

16X (0.6)

SYMM

16

9

14X (1.27)

8

(R0.05) TYP

(7)

SOLDER PASTE EXAMPLE
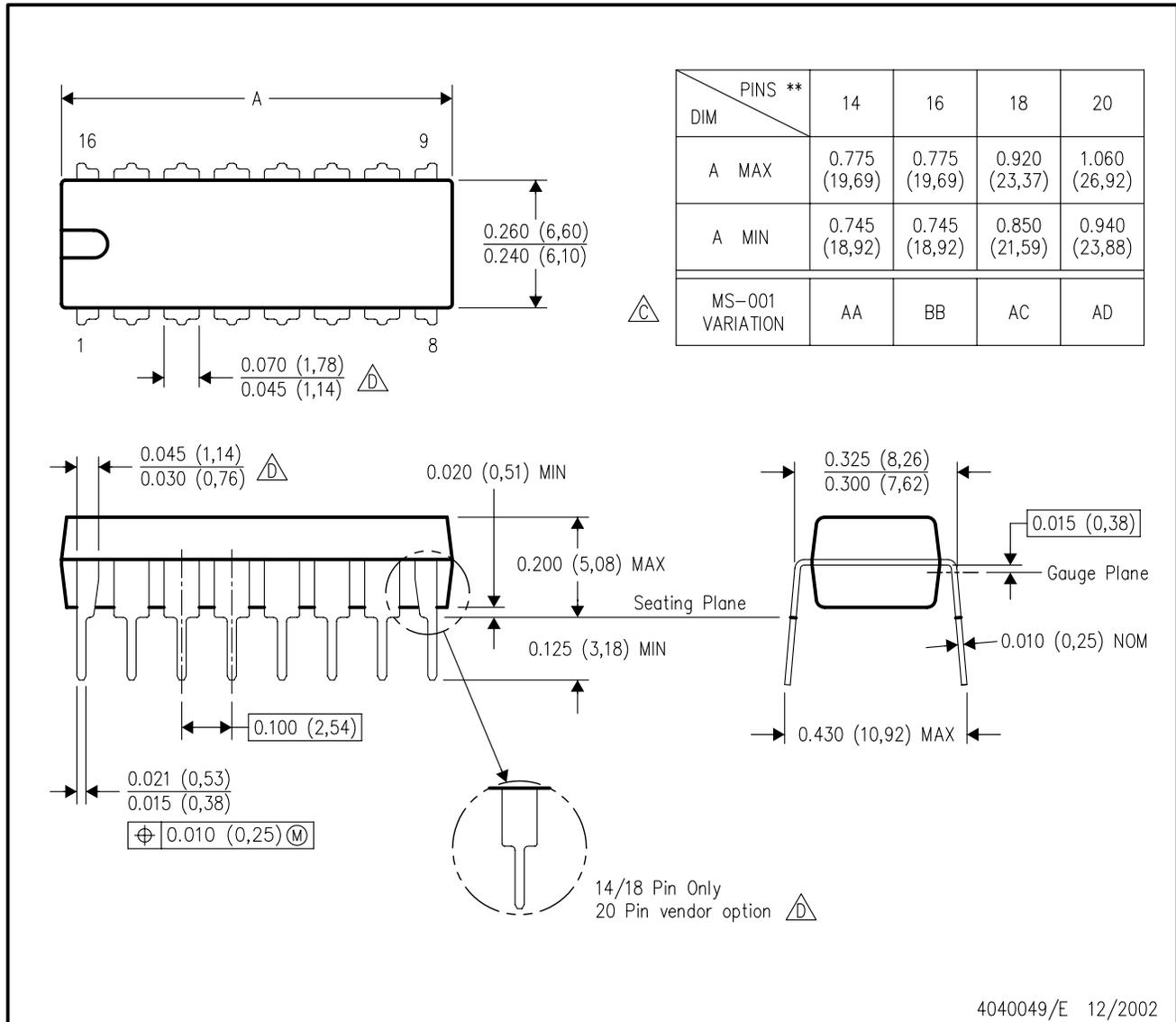BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

4040049/E   12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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