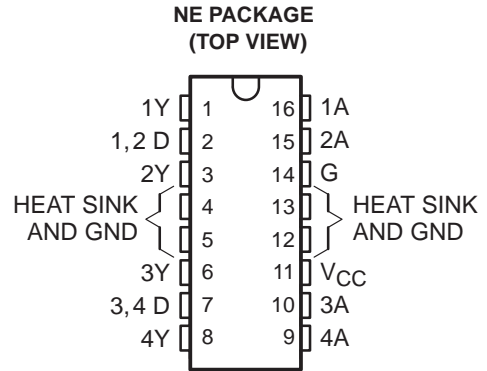


# SN75437A QUADRUPLE PERIPHERAL DRIVER

SLRS019B – DECEMBER 1986 – REVISED SEPTEMBER 2000

- Saturating Outputs With Low On-State Resistance
- High-Impedance Inputs Compatible With CMOS and TTL Levels
- Very Low Standby Power . . . 21 mW Max
- High-Voltage Outputs . . . 70 V Min
- No Power-Up or Power-Down Output Glitch
- No Latch-Up Within Recommended Operating Conditions
- Output-Clamp Diodes for Transient Suppression
- Packaged in 2-W Power, Thermally Enhanced Plastic DIP



## description

The SN75437A quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. This device features four inverting open-collector outputs with a common-enable (G) input that, when taken low, disables all four outputs. The envelope of 1-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

The SN75437A is characterized for operation over the free-air temperature range of 0°C to 70°C.

FUNCTION TABLE  
(each NAND driver)

INPUTS		OUTPUT
A	G	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,  
X = irrelevant



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

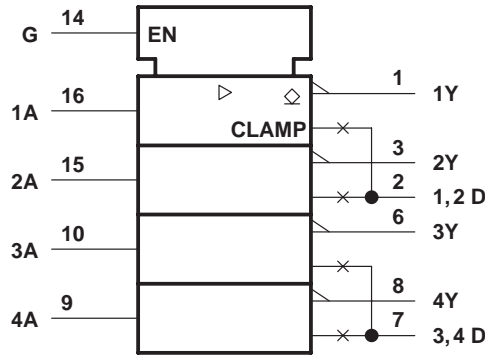
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

# SN75437A QUADRUPLE PERIPHERAL DRIVER

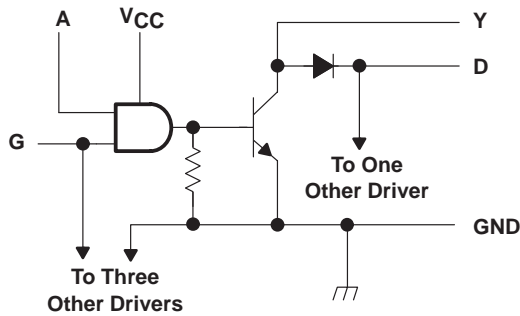
SLRS019B – DECEMBER 1986 – REVISED SEPTEMBER 2000

## logic diagram (positive logic)†

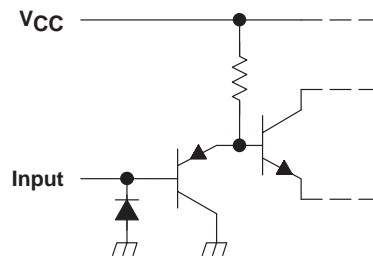


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

## logic diagram (positive logic, each driver)



## equivalent schematic of each input



## absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	30 V
Output current (see Note 1)	0.75 A
Output clamp-diode current, $I_{OK}$	1.25 A
Output voltage, $V_O$ (off state)	70 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075 mW
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	-65°C to 150°C

- NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.  
2. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

## recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
Output supply voltage in inductive switching circuit (see Figure 2), $V_S$			35	V
Output current, $I_O$			0.5	A
Operating free-air temperature, $T_A$	0		70	°C



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

# SN75437A QUADRUPLE PERIPHERAL DRIVER

SLRS019B – DECEMBER 1986 – REVISED SEPTEMBER 2000

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$V_{CC} = 4.75 \text{ V}$ ,	$I_I = -12 \text{ mA}$	-0.9	-1.5		V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.75 \text{ V}$ , $V_{IH} = 2 \text{ V}$	$I_{OL} = 250 \text{ mA}$	0.14	0.25		V
			$I_{OL} = 500 \text{ mA}$	0.28	0.5		
$V_{R(K)}$	Output clamp-diode reverse voltage	$V_{CC} = 4.75 \text{ V}$ ,	$I_R = 100 \mu\text{A}$	70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage	$I_F = 500 \text{ mA}$		1	1.6		V
$I_{OH}$	High-level output current	$V_{CC} = 4.75 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ ,	$V_{IH} = 2 \text{ V}$ , $V_{OH} = 70 \text{ V}$	1	100		$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = 5.25 \text{ V}$ ,	$V_I = 5.25 \text{ V}$	0.1	10		$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{CC} = 5.25 \text{ V}$ ,	$V_I = 0.8 \text{ V}$	-0.25	-10		$\mu\text{A}$
$I_{CCH}$	Supply current, outputs high	$V_{CC} = 5.25 \text{ V}$ ,	$V_I = 0$	1	4		mA
$I_{CCL}$	Supply current, outputs low	$V_{CC} = 5.25 \text{ V}$ ,	$V_I = 5 \text{ V}$	45	65		mA

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

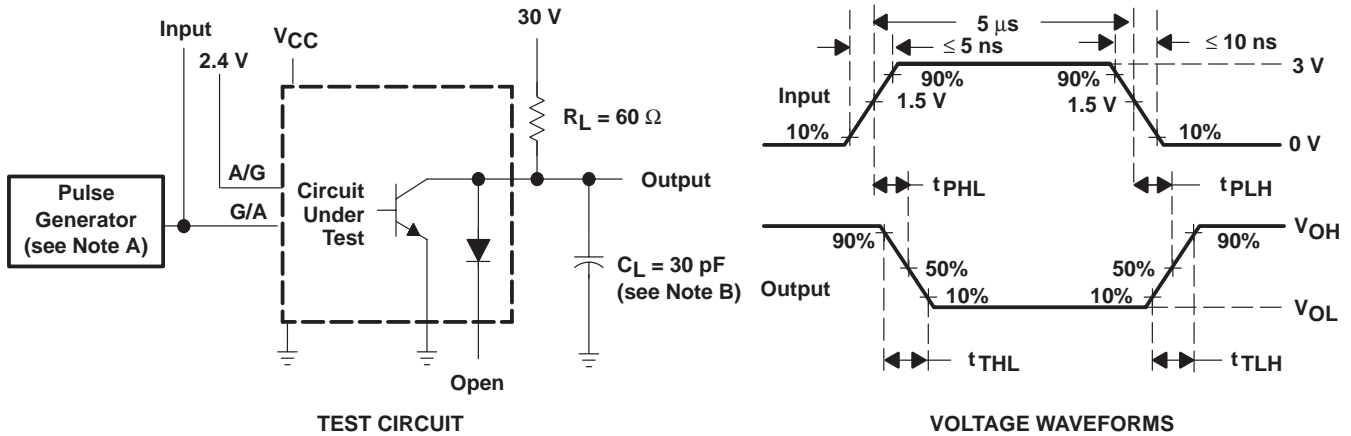
**switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$C_L = 30 \text{ pF}$ , $R_L = 60 \Omega$ , See Figure 1			1950	5000	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output				150	500	ns
$t_{TLH}$	Transition time, low-to-high-level output				40		ns
$t_{THL}$	Transition time, high-to-low-level output				36		ns
$V_{OH}$	High-level output voltage after switching	$V_S = 35 \text{ V}$ , $R_L = 70 \Omega$ ,	$I_O \approx 500 \text{ mA}$ , See Figure 2	$V_S - 10$			mV

# SN75437A QUADRUPLE PERIPHERAL DRIVER

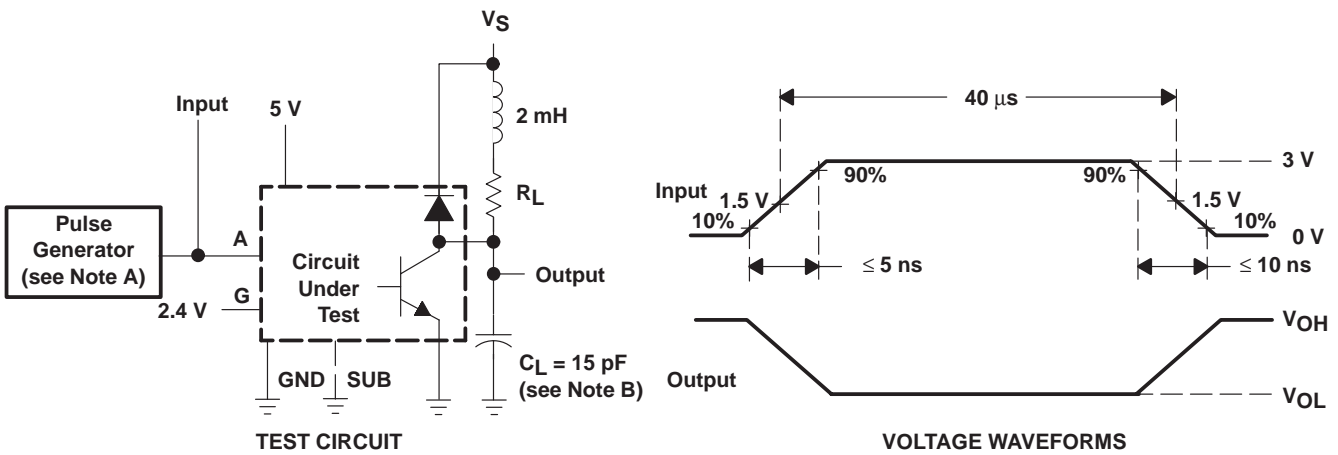
SLRS019B – DECEMBER 1986 – REVISED SEPTEMBER 2000

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75437ANE	ACTIVE	PDIP	NE	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75437ANE	<a href="#">Samples</a>
SN75437ANEE4	ACTIVE	PDIP	NE	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75437ANE	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TUBE**

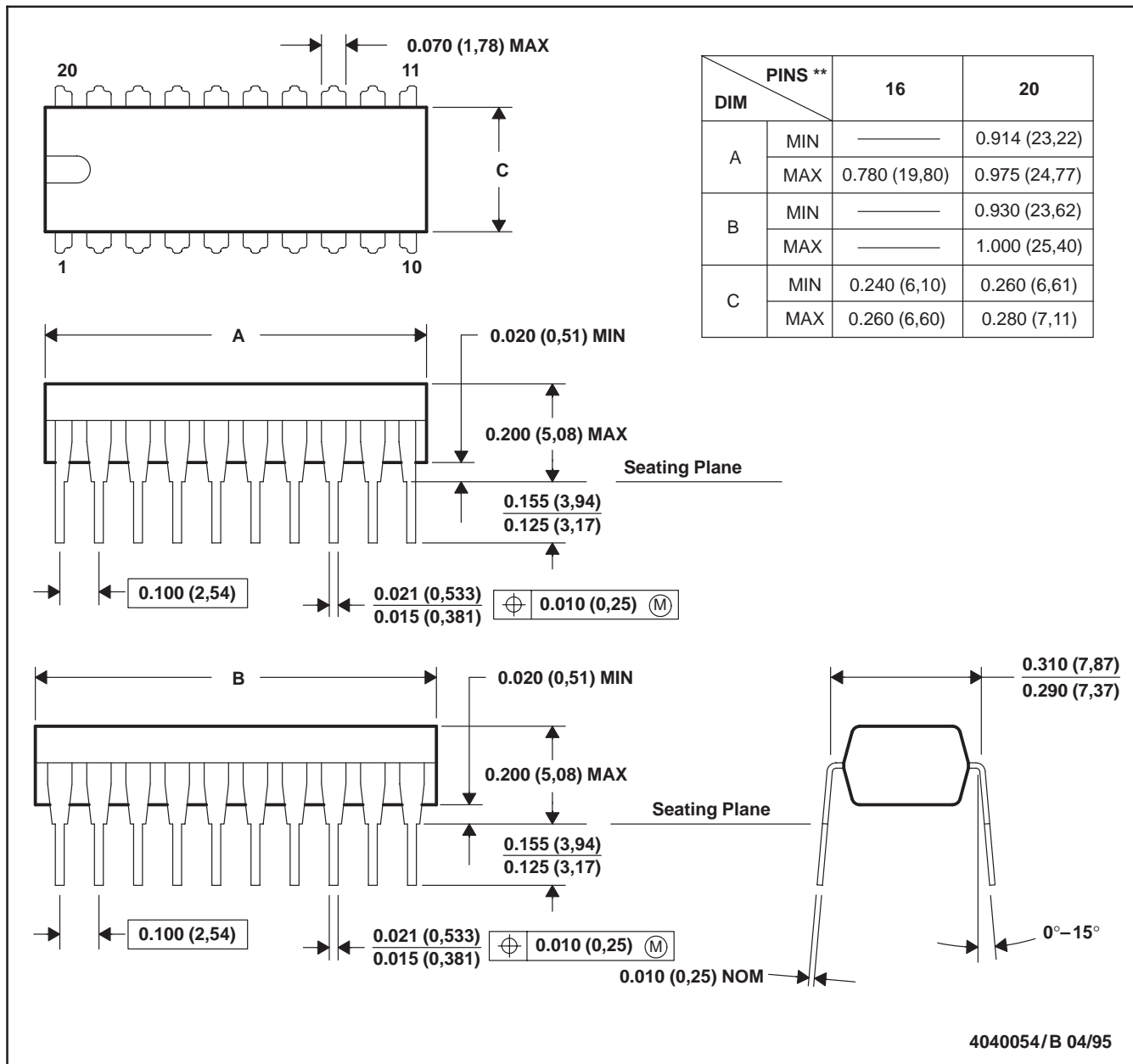

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75437ANE	NE	PDIP	16	25	506	13.97	11230	4.32
SN75437ANEE4	NE	PDIP	16	25	506	13.97	11230	4.32

NE (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (16 pin only)



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated