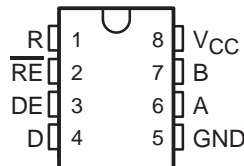


SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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- Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-485-A† and ITU Recommendations V.11 and X.27
- Operate at Data Rates up to 35 Mbaud
- Four Skew Limits Available:
SN65ALS176 . . . 15 ns
SN75ALS176 . . . 10 ns
SN75ALS176A . . . 7.5 ns
SN75ALS176B . . . 5 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirements
. . . 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design

D OR P PACKAGE
(TOP VIEW)



description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS176 and SN75ALS176 series combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from -40°C to 85°C . The SN75ALS176 series is characterized for operation from 0°C to 70°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† These devices meet or exceed the requirements of TIA/EIA-485-A, except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are -6 V to 8 V for the SN75ALS176, SN75ALS176A, and SN75ALS176B and -4 V to 8 V for the SN65ALS180.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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AVAILABLE OPTIONS

| T _A | t _{sk(lim)} † | PACKAGED DEVICES | |
|----------------|------------------------|--------------------|-----------------|
| | | SMALL OUTLINE (D)‡ | PLASTIC DIP (P) |
| 0°C to 70°C | 10 | SN75ALS176D | SN75ALS176P |
| | 7.5 | SN75ALS176AD | SN75ALS176AP |
| | 5 | SN75ALS176BD | SN75ALS176BP |
| -40°C to 85°C | 15 | SN65ALS176D | SN65ALS176P |

† This is the maximum range that the driver or receiver delay times vary over temperature, V_{CC}, and process (device to device).

‡ The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS176DR).

Function Tables

DRIVER

| INPUT D | ENABLE DE | OUTPUTS | |
|---------|-----------|---------|---|
| | | A | B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

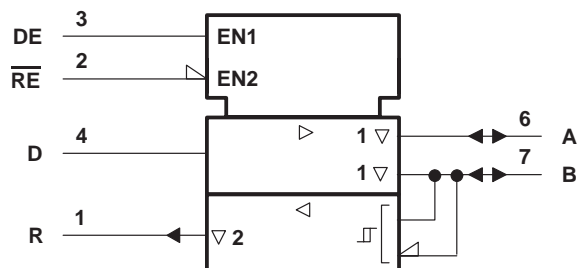
H = high level, L = low level, X = irrelevant, Z = high impedance

RECEIVER

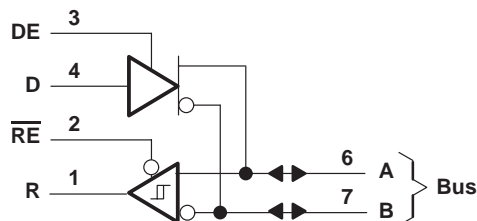
| DIFFERENTIAL INPUTS A-B | ENABLE RE | OUTPUT R |
|----------------------------------|-----------|----------|
| V _{ID} ≥ 0.2 V | L | H |
| -0.2 V < V _{ID} < 0.2 V | L | ? |
| V _{ID} ≤ -0.2 V | L | L |
| X | H | Z |
| Inputs open | L | H |

H = high level, L = low level, X = irrelevant, Z = high impedance

logic symbol§



logic diagram (positive logic)

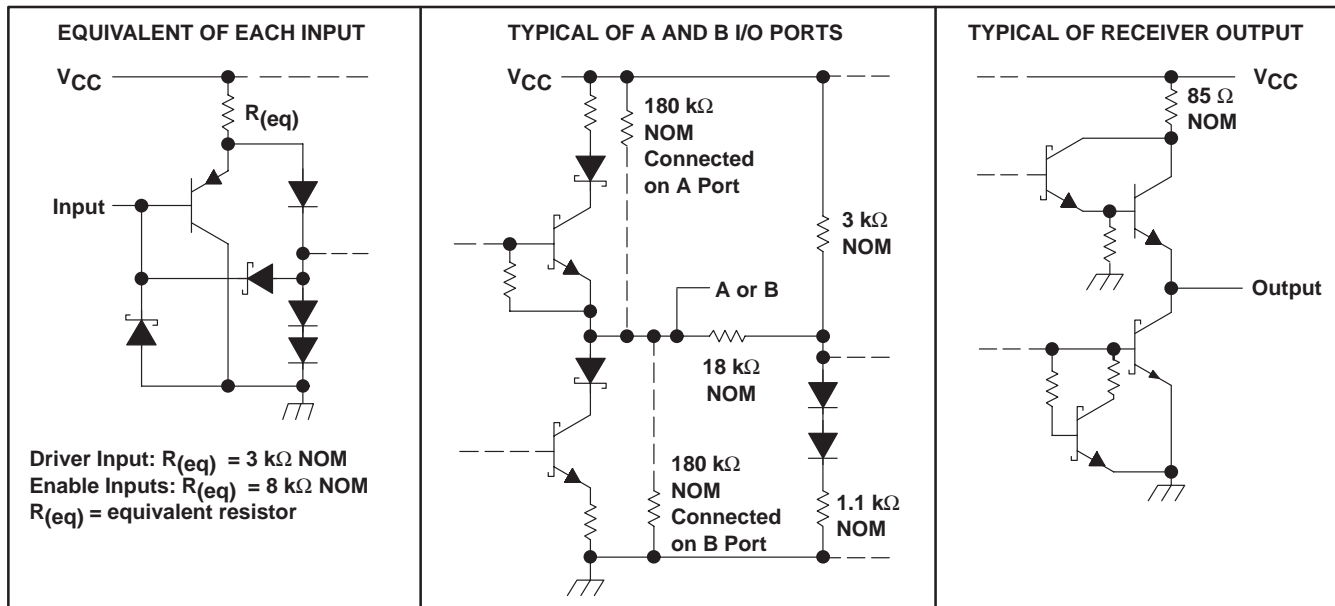


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Voltage range at any bus terminal | -7 V to 12 V |
| Enable input voltage, V_I | 5.5 V |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 97°C/W |
| P package | 85°C/W |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
 2. The package thermal impedance is calculated in accordance with JESD 51.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B

DIFFERENTIAL BUS TRANSCEIVERS

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recommended operating conditions (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|----------------------------|----------|-----|------|-------------|
| Supply voltage, V_{CC} | | 4.75 | 5 | 5.25 | V |
| Input voltage at any bus terminal (separately or common mode), V_I or V_{IC} | | 12 | | | V |
| | | -7 | | | |
| High-level input voltage, V_{IH} | D, DE, and \overline{RE} | 2 | | | V |
| Low-level input voltage, V_{IL} | D, DE, and \overline{RE} | 0.8 | | | V |
| Differential input voltage, V_{ID} (see Note 3) | | ± 12 | | | V |
| High-level output current, I_{OH} | Driver | -60 | | | mA |
| | Receiver | -400 | | | μA |
| Low-level output current, I_{OL} | Driver | 60 | | | mA |
| | Receiver | 8 | | | |
| Operating free-air temperature, T_A | SN65ALS176 | -40 | | | $^{\circ}C$ |
| | SN75ALS176 series | 0 | 70 | | |

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | MIN | TYP‡ | MAX | UNIT |
|-------------------|---|-----------------------------------|-----------------------|------------------------------|------|---------|------|
| V _{IK} | Input clamp voltage | I _I = -18 mA | | | | -1.5 | V |
| V _O | Output voltage | I _O = 0 | | 0 | | 6 | V |
| V _{OD1} | Differential output voltage | I _O = 0 | | 1.5 | | 6 | V |
| V _{OD2} | Differential output voltage | R _L = 100 Ω, | See Figure 1 | 1/2V _{OD1} or 2§ | | | V |
| | | R _L = 54 Ω, | See Figure 1 | 1.5 | 2.5 | 5 | V |
| V _{OD3} | Differential output voltage | V _{test} = -7 V to 12 V, | See Figure 2 | 1.5 | | 5 | V |
| Δ V _{OD} | Change in magnitude of differential output voltage¶ | R _L = 54 Ω or 100 Ω, | See Figure 1 | | | ±0.2 | V |
| V _{OC} | Common-mode output voltage | R _L = 54 Ω or 100 Ω, | See Figure 1 | | | 3 -1 | V |
| Δ V _{OC} | Change in magnitude of common-mode output voltage¶ | R _L = 54 Ω or 100 Ω, | See Figure 1 | | | ±0.2 | V |
| I _O | Output current | Outputs disabled (see Note 4) | V _O = 12 V | | | 1 | mA |
| | | | V _O = -7 V | | | -0.8 | |
| I _{IH} | High-level input current | V _I = 2.4 V | | | | 20 | μA |
| I _{IL} | Low-level input current | V _I = 0.4 V | | | | -400 | μA |
| I _{OS} | Short-circuit output current# | V _O = -4 V | SN65ALS176 | | | -250 | mA |
| | | V _O = -6 V | SN75ALS176 | | | -250 | |
| | | V _O = 0 | | | | -150 | |
| | | V _O = V _{CC} | | | | 250 | |
| | | V _O = 8 V | | | | 250 | |
| I _{CC} | Supply current | No load | Outputs enabled | | 23 | 30 | mA |
| | | | Outputs disabled | | 19 | 26 | |

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

¶ Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

SN65ALS176

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|-----------------------|-------------------------------------|-------------------------|-------------------------|--------------|-----|------|-----|------|
| t _d (OD) | Differential output delay time | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | | | 15 | ns |
| t _{sk} (p) | Pulse skew‡ | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | | 0 | 2 | ns |
| t _{sk} (lim) | Pulse skew§ | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | | | 15 | ns |
| t _t (OD) | Differential output transition time | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | | 8 | | ns |
| t _{PZH} | Output enable time to high level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 4 | | | 80 | ns |
| t _{PZL} | Output enable time to low level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 5 | | | 30 | ns |
| t _{PHZ} | Output disable time from high level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 4 | | | 50 | ns |
| t _{PLZ} | Output disable time from low level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 5 | | | 30 | ns |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SN75ALS176, SN75ALS176A, SN75ALS176B

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT | |
|-----------------------|-------------------------------------|-------------------------|-------------------------|-------------------------|--------------|------|-----|------|----|
| t _d (OD) | Differential output delay time | 'ALS176 | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | 3 | 8 | 13 | ns |
| | | 'ALS176A | | | | 4 | 7 | 11.5 | |
| | | 'ALS176B | | | | 5 | 8 | 10 | |
| t _{sk} (p) | Pulse skew‡ | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | | 0 | 2 | ns | |
| t _{sk} (lim) | Pulse skew§ | 'ALS176 | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | | | 10 | ns |
| | | 'ALS176A | | | | | | 7.5 | |
| | | 'ALS176B | | | | | | 5 | |
| t _t (OD) | Differential output transition time | R _L = 54 Ω, | C _L = 50 pF, | See Figure 3 | | 8 | | ns | |
| t _{PZH} | Output enable time to high level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 4 | | 23 | 50 | ns | |
| t _{PZL} | Output enable time to low level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 5 | | 14 | 20 | ns | |
| t _{PHZ} | Output disable time from high level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 4 | | 20 | 35 | ns | |
| t _{PLZ} | Output disable time from low level | R _L = 110 Ω, | C _L = 50 pF, | See Figure 5 | | 8 | 17 | ns | |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SYMBOL EQUIVALENTS

| DATA-SHEET PARAMETER | TIA/EIA-422-B | TIA/EIA-485-A |
|----------------------|---|---|
| V _O | V _{oa} , V _{ob} | V _{oa} , V _{ob} |
| V _{OD1} | V _o | V _o |
| V _{OD2} | V _t (R _L = 100 Ω) | V _t (R _L = 54 Ω) |
| V _{OD3} | None | V _t (test termination measurement 2) |
| Δ V _{OD} | V _t - V _{tl} | V _t - V _{tl} |
| V _{OC} | V _{os} | V _{os} |
| Δ V _{OC} | V _{os} - V _{os} | V _{os} - V _{os} |
| I _{OS} | I _{sa} , I _{sb} | None |
| I _O | I _{xa} , I _{xb} | I _{ia} , I _{ib} |



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-----------|--|---|--------------------------------------|-------|------|----------|------------------|
| V_{IT+} | Positive-going input threshold voltage | $V_O = 2.7\text{ V}$, | $I_O = -0.4\text{ mA}$ | | | 0.2 | V |
| V_{IT-} | Negative-going input threshold voltage | $V_O = 0.5\text{ V}$, | $I_O = 8\text{ mA}$ | -0.2‡ | | | V |
| V_{hys} | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | | | | 60 | | mV |
| V_{IK} | Enable-input clamp voltage | $I_I = -18\text{ mA}$ | | | | -1.5 | V |
| V_{OH} | High-level output voltage | $V_{ID} = 200\text{ mV}$, See Figure 6 | $I_{OH} = -400\text{ }\mu\text{A}$, | 2.7 | | | V |
| V_{OL} | Low-level output voltage | $V_{ID} = -200\text{ mV}$, See Figure 6 | $I_{OL} = 8\text{ mA}$, | | | 0.45 | V |
| I_{OZ} | High-impedance-state output current | $V_O = 0.4\text{ V to }2.4\text{ V}$ | | | | ± 20 | μA |
| V_I | Line input current | Other input = 0 V (see Note 5) | $V_I = 12\text{ V}$ | | | 1 | mA |
| | | | $V_I = -7\text{ V}$ | | | -0.8 | |
| I_{IH} | High-level-enable input current | $V_{IH} = 2.7\text{ V}$ | | | | 20 | μA |
| I_{IL} | Low-level-enable input current | $V_{IL} = 0.4\text{ V}$ | | | | -100 | μA |
| r_I | Input resistance | | | 12 | 20 | | $\text{k}\Omega$ |
| I_{OS} | Short-circuit output current | $V_{ID} = 200\text{ mV}$, | $V_O = 0$ | -15 | | -85 | mA |
| I_{CC} | Supply current | No load | Outputs enabled | | 23 | 30 | mA |
| | | | Outputs disabled | | 19 | 26 | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

SN65ALS176

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|----------------------|-------------------------------------|--|---|-----|------|-----|------|
| t _{pd} | Propagation time | V _{ID} = -1.5 V to 1.5 V, See Figure 7 | C _L = 15 pF, | | | 25 | ns |
| t _{sk(p)} | Pulse skew§ | V _{ID} = -1.5 V to 1.5 V, See Figure 7 | C _L = 15 pF, | | 0 | 2 | ns |
| t _{sk(lim)} | Pulse skew¶ | R _L = 54 Ω, See Figure 3 | C _L = 50 pF, | | | 15 | ns |
| t _{PZH} | Output enable time to high level | | C _L = 15 pF, See Figure 8 | | 11 | 18 | ns |
| t _{PZL} | Output enable time to low level | | C _L = 15 pF, See Figure 8 | | 11 | 18 | ns |
| t _{PHZ} | Output disable time from high level | | C _L = 15 pF, See Figure 8 | | | 50 | ns |
| t _{PLZ} | Output disable time from low level | | C _L = 15 pF, See Figure 8 | | | 30 | ns |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.

¶ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SN75ALS176, SN75ALS176A, SN75ALS176B

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|----------------------|-------------------------------------|--|--|-------------------------|------|-----|------|----|
| t _{pd} | Propagation time | 'ALS176 | V _{ID} = -1.5 V to 1.5 V, See Figure 7 | C _L = 15 pF, | 9 | 14 | 19 | ns |
| | | 'ALS176A | | | 10.5 | 14 | 18 | |
| | | 'ALS176B | | | 11.5 | 13 | 16.5 | |
| t _{sk(p)} | Pulse skew‡ | V _{ID} = -1.5 V to 1.5 V, See Figure 7 | C _L = 15 pF, | | 0 | 2 | ns | |
| t _{sk(lim)} | Pulse skew§ | 'ALS176 | R _L = 54 Ω, See Figure 3 | C _L = 50 pF, | | 10 | ns | |
| | | 'ALS176A | | | | 7.5 | | |
| | | 'ALS176B | | | | 5 | | |
| t _{PZH} | Output enable time to high level | | C _L = 15 pF, See Figure 8 | | 7 | 14 | ns | |
| t _{PZL} | Output enable time to low level | | C _L = 15 pF, See Figure 8 | | 20 | 35 | ns | |
| t _{PHZ} | Output disable time from high level | | C _L = 15 pF, See Figure 8 | | 20 | 35 | ns | |
| t _{PLZ} | Output disable time from low level | | C _L = 15 pF, See Figure 8 | | 8 | 17 | ns | |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.

§ Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

PARAMETER MEASUREMENT INFORMATION

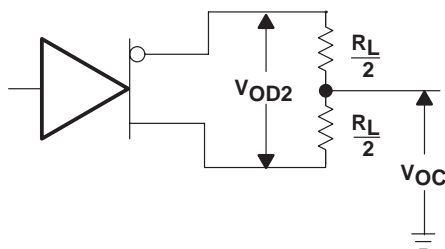


Figure 1. Driver V_{OD2} and V_{OC}

PARAMETER MEASUREMENT INFORMATION

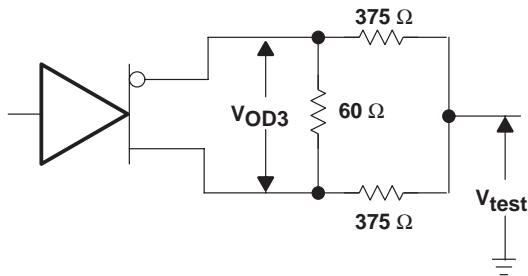
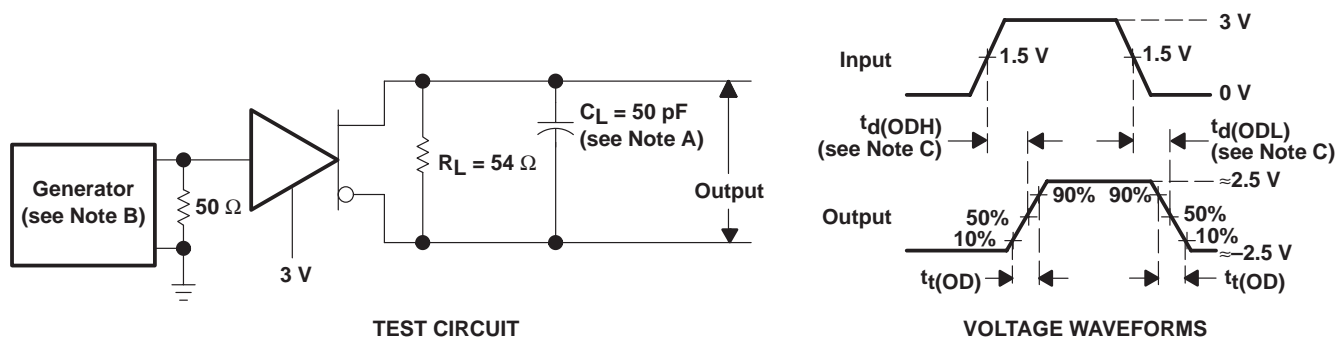
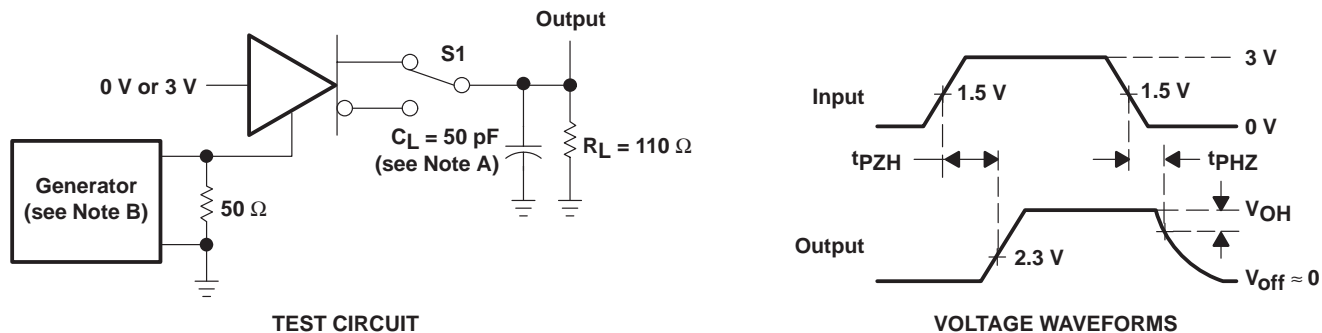


Figure 2. Driver V_{OD3}



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.
 C. $t_d(OD) = t_d(ODH)$ or $t_d(ODL)$

Figure 3. Driver Test Circuit and Voltage Waveforms



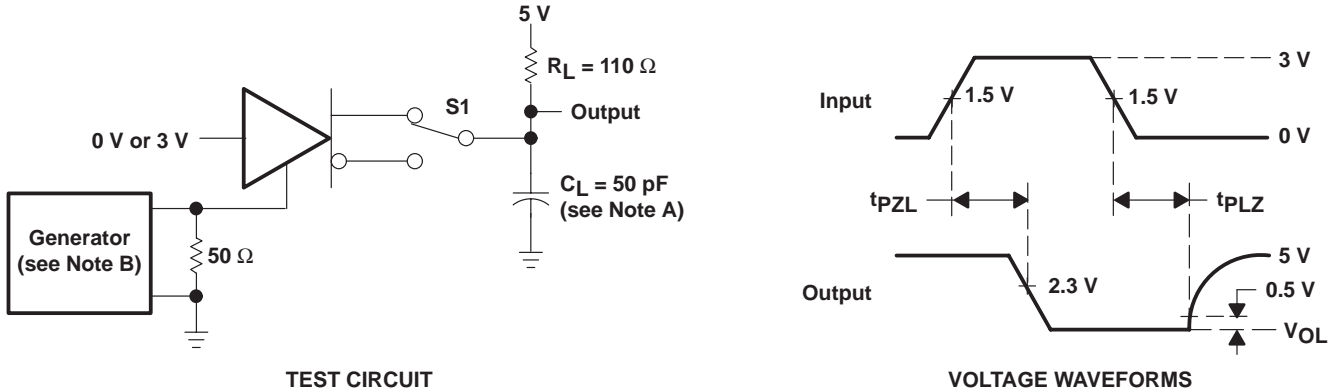
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.

Figure 4. Driver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 5. Driver Test Circuit and Voltage Waveforms

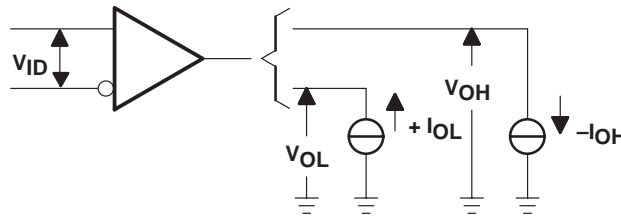
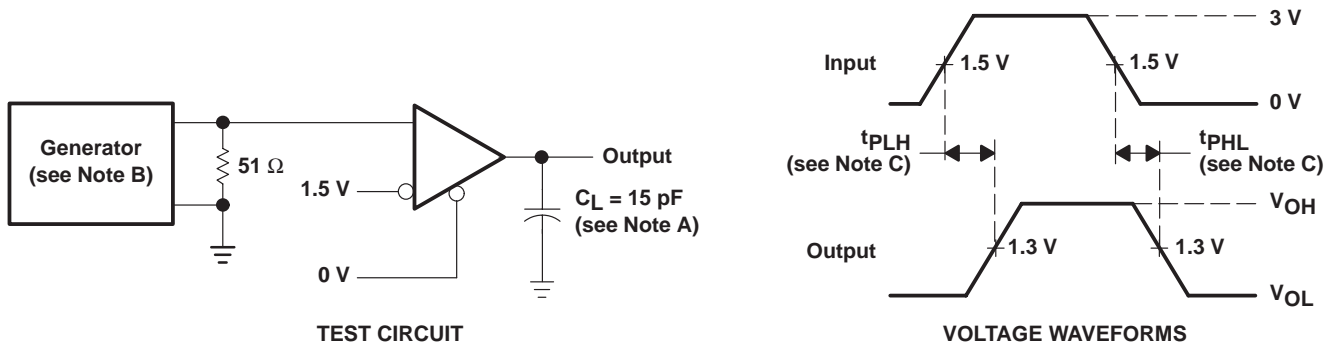


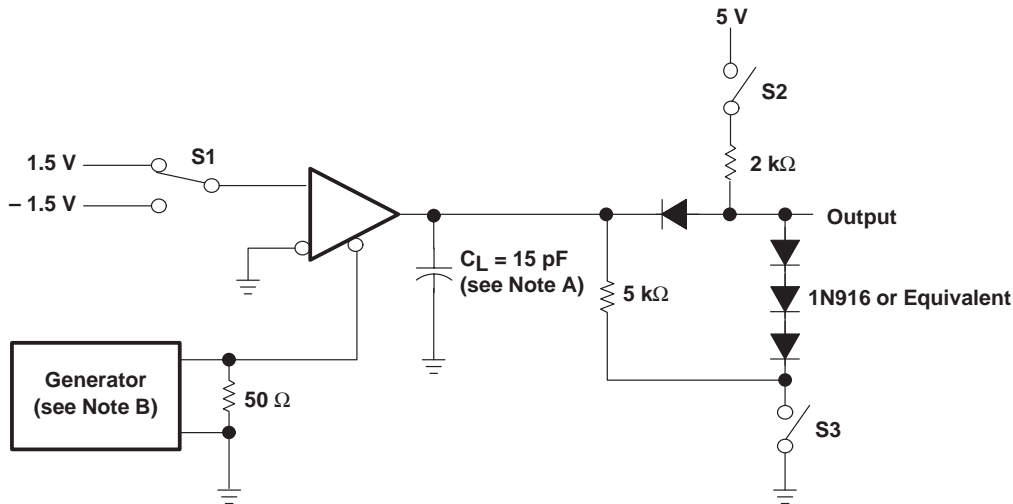
Figure 6. Receiver V_{OH} and V_{OL} Test Circuit



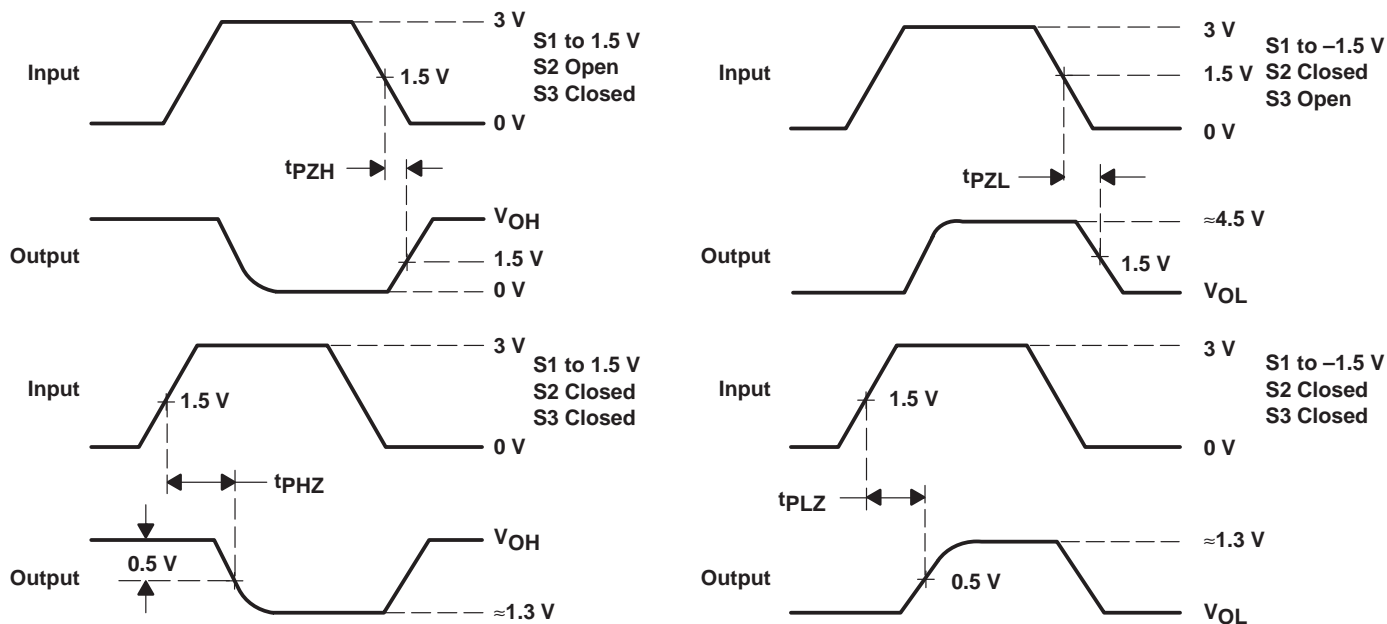
- NOTES: A. C_L includes probe and jig capacitance.
 B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
 C. $t_{pd} = t_{PLH}$ or t_{PHL}

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

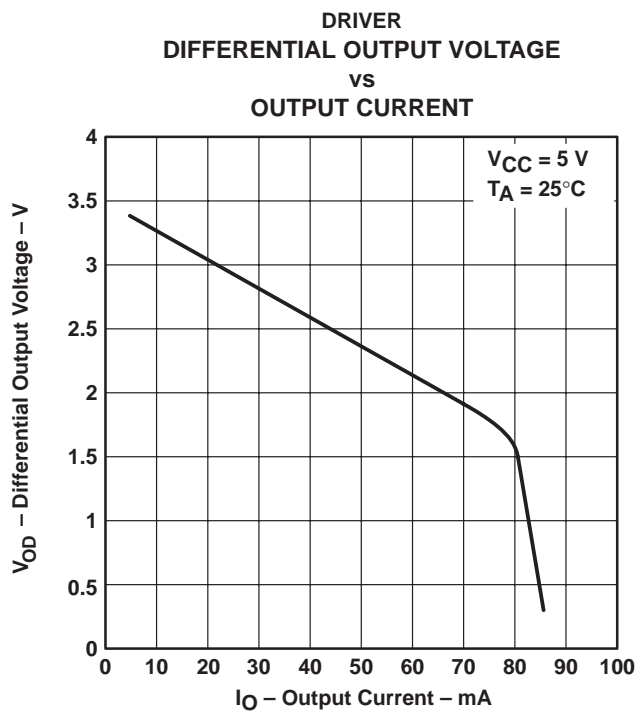
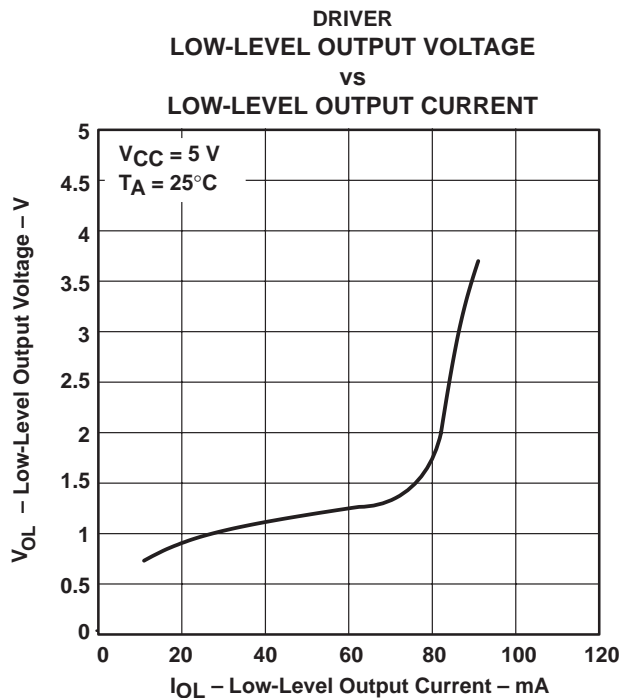
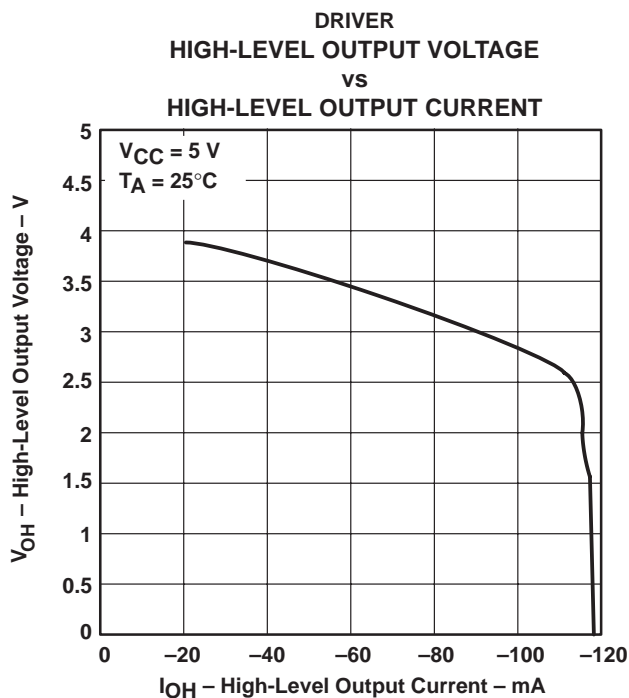
- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.

Figure 8. Receiver Test Circuit and Voltage Waveforms

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

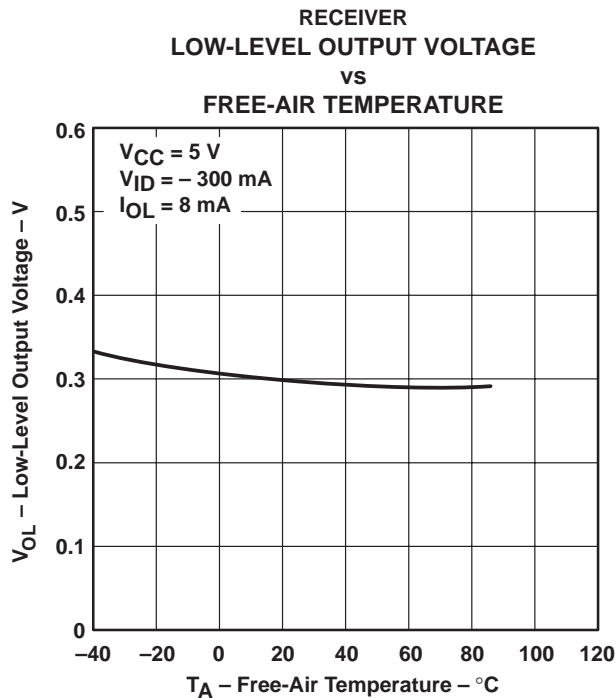
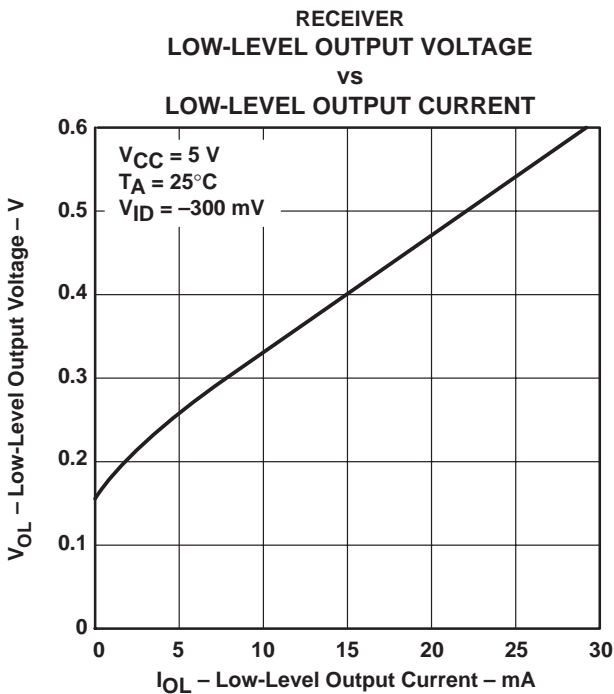
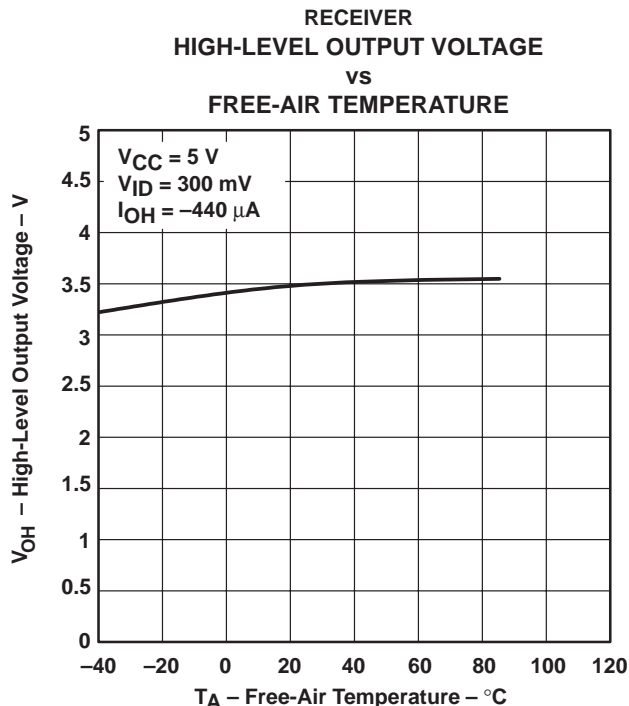
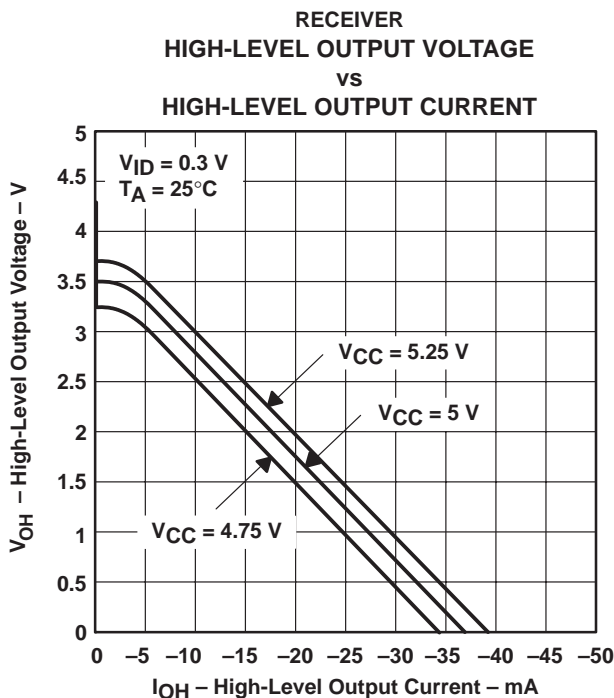
SLLS040H – AUGUST 1987 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

RECEIVER TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS†

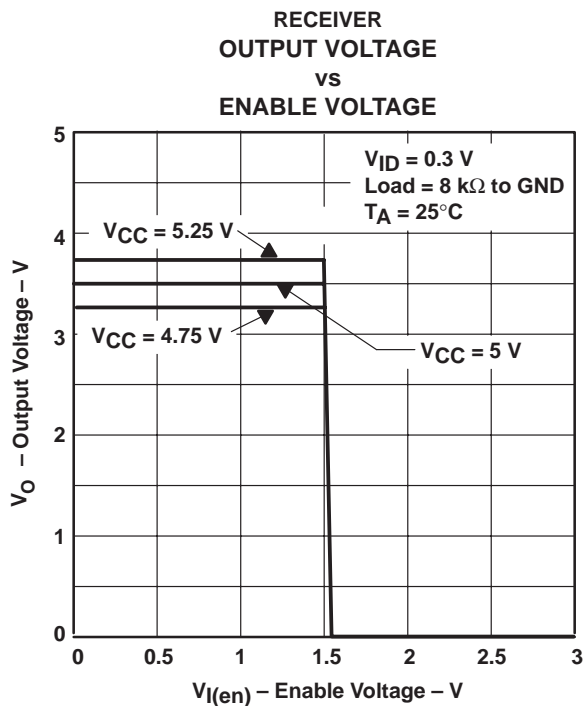


Figure 16

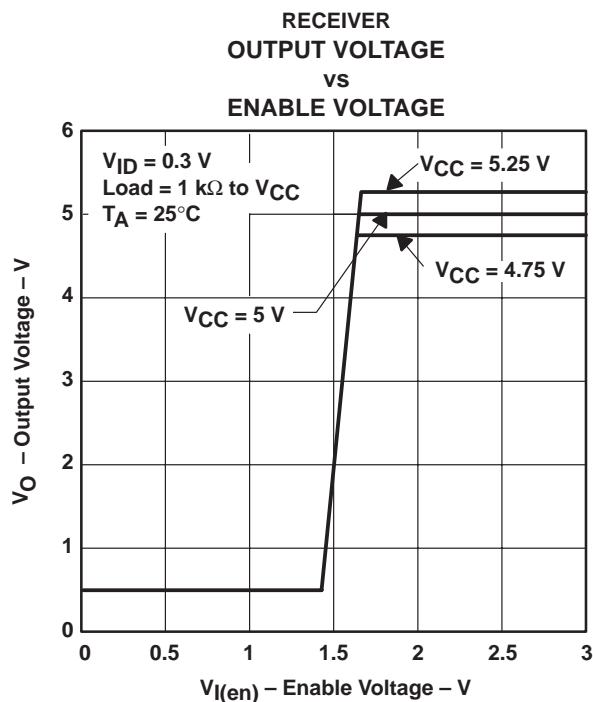
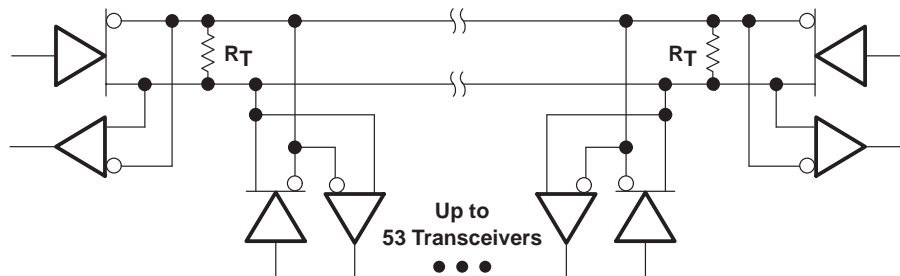


Figure 17

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

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| Military | www.ti.com/military |
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| Security | www.ti.com/security |
| Telephony | www.ti.com/telephony |
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| Wireless | www.ti.com/wireless |

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN65ALS176D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65ALS176DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65ALS176DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65ALS176DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65ALS176DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65ALS176DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65ALS176P | OBSOLETE | PDIP | P | 8 | | TBD | Call TI | Call TI |
| SN75ALS176AD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176ADE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176ADG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176ADR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176ADRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176ADRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176AP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75ALS176APE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75ALS176BD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176BDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176BDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176BDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176BDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176BDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176BP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75ALS176BPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75ALS176D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176DE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN75ALS176DG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176DRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176DRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN75ALS176P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN75ALS176PE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65ALS176DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75ALS176ADR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75ALS176BDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75ALS176DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65ALS176DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN75ALS176ADR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN75ALS176BDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| SN75ALS176DR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65ALS176D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65A176 | Samples |
| SN65ALS176DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65A176 | Samples |
| SN75ALS176AD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7A176A | Samples |
| SN75ALS176ADR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7A176A | Samples |
| SN75ALS176ADRG4 | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7A176A | Samples |
| SN75ALS176AP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | 75ALS176A | Samples |
| SN75ALS176BD | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7A176B | Samples |
| SN75ALS176BDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 7A176B | Samples |
| SN75ALS176BP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | 75ALS176B | Samples |
| SN75ALS176D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75A176 | Samples |
| SN75ALS176DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75A176 | Samples |
| SN75ALS176P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | 75ALS176 | Samples |
| SN75ALS176PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | 75ALS176 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65ALS176DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75ALS176ADR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75ALS176BDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| SN75ALS176DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65ALS176DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| SN75ALS176ADR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| SN75ALS176BDR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |
| SN75ALS176DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65ALS176D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75ALS176AD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75ALS176AP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75ALS176BD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75ALS176BP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75ALS176D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| SN75ALS176P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| SN75ALS176PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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