TCA6408A-Q1 具有中断输出的低电压 8 位 I^2C 和 SMBus I/O 扩展器

1 特性

- I^2C 至并行端口扩展器
- 1.65V 至 3.6V 工作电源电压范围
- 支持 1.8V、2.5V、3.3V I^2C 总线和 P 端口之间进行双向电平转换和通用输入/输出 (GPIO) 扩展
- 低待机流耗
- 400kHz 快速 I^2C 总线
- 硬件寻址引脚允许同一 I^2C/SMBus 总线存在两个 TCA6408A-Q1 器件
- 低电平有效复位 ($\overline{\text{RESET}}$) 输入
- 开漏低电平有效中断 ($\overline{\text{INT}}$) 输出
- 输入和输出配置寄存器
- 极性反转寄存器
- 内部加电复位
- 在所有通道均被配置为输入的情况下加电
- 在加电时无毛刺脉冲
- SCL/SDA 输入端上的噪声滤波器
- 具有最大高电流驱动能力的锁存输出，适用于直接驱动 LED
- 锁存性能可达 100mA，符合 AEC Q100-004 标准
- 施密特触发器操作支持在串行时钟 (SCL) 和串行数据 (SDA) 输入实现缓慢输入转换并提升开关噪声抗扰度
- 静电放电 (ESD) 保护
  - 2000V 人体模型 (Q100-002)
  - 1000V 带电器件模型 (Q100-011)

2 应用

- 车用信息娱乐
- 高级驾驶员辅助系统 (ADAS)
- 汽车车身电子设备
- 混合动力汽车 (HEV)、电动汽车 (EV) 和动力传动
- 工业、工厂和楼宇自动化
- 测试和测量
- 电子销售点 (EPOS)

3 说明

TCA6408A-Q1 是一款 16 引脚器件，可为两线双向 I^2C 总线（或 SMBus）协议提供 8 位通用并行输入/输出 (I/O) 扩展。在器件运行过程中，I^2C 总线侧 (V_{CCI}) 和 P 端口侧 (V_{CCP}) 均可由电压介于 1.65V 至 3.6V 之间的电源供电。这使得 TCA6408A-Q1 能够在 SDA/SCL 侧（电源电平在此逐渐降低以节省功率）与下一代微处理器和微控制器相连。与微处理器和微控制器的降压电源相比，部分 PCB 组件（例如 LED）仍由高电压电源供电。

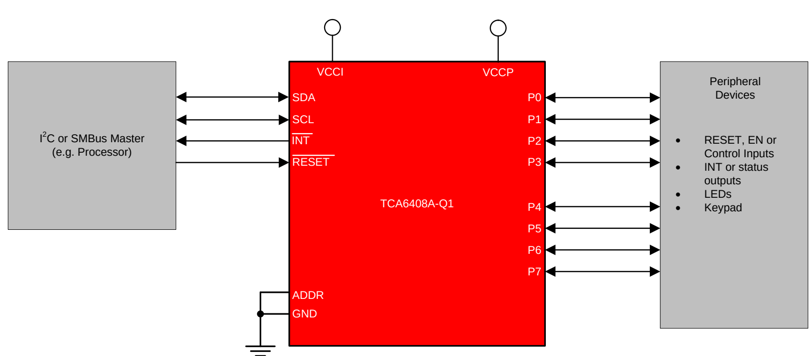
该器件支持 100kHz（标准模式）和 400kHz（快速模式）时钟频率。当开关、传感器、按钮、LED、风扇等设备需要额外使用 I/O 时，I/O 扩展器（如 TCA6408A-Q1）可提供简易解决方案。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCA6408A-Q1	TSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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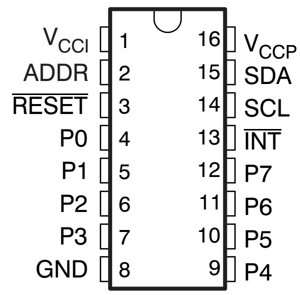
4 修订历史记录

日期	修订版本	注释
2016 年 9 月	*	最初发布版本。

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR	2	I	Address input. Connect directly to V_{CCP} or ground
GND	8	—	Ground
$\overline{INT}$	13	O	Interrupt output. Connect to V_{CCI} through a pull-up resistor
P0	4	I/O	P-port input-output (push-pull design structure). At power on, P0 is configured as an input
P1	5	I/O	P-port input-output (push-pull design structure). At power on, P1 is configured as an input
P2	6	I/O	P-port input-output (push-pull design structure). At power on, P2 is configured as an input
P3	7	I/O	P-port input-output (push-pull design structure). At power on, P3 is configured as an input
P4	9	I/O	P-port input-output (push-pull design structure). At power on, P4 is configured as an input
P5	10	I/O	P-port input-output (push-pull design structure). At power on, P5 is configured as an input
P6	11	I/O	P-port input-output (push-pull design structure). At power on, P6 is configured as an input
P7	12	I/O	P-port input-output (push-pull design structure). At power on, P7 is configured as an input
$\overline{RESET}$	3	I	Active-low reset input. Connect to V_{CCI} through a pull-up resistor, if no active connection is used
SCL	14	I	Serial clock bus. Connect to V_{CCI} through a pull-up resistor
SDA	15	I/O	Serial data bus. Connect to V_{CCI} through a pull-up resistor
V_{CCI}	1	—	Supply voltage of I^2C bus. Connect directly to the V_{CC} of the external I^2C master. Provides voltage level translation
V_{CCP}	16	—	Supply voltage of TCA6408A-Q1 for P-ports

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see [1])

				MIN	MAX	UNIT
V_{CCI}	Supply voltage for I^2C pins			–0.5	3.6	V
V_{CCP}	Supply voltage for P-ports			–0.5	3.6	V
V_I	Input voltage [2]			–0.5	3.6	V
V_O	Output voltage [2]			–0.5	3.6	V
I_{IK}	Input clamp current	ADDR, $\overline{\text{RESET}}$, SCL	$V_I < 0$		±20	mA
I_{OK}	Output clamp current	$\overline{\text{INT}}$	$V_O < 0$		±20	mA
I_{IOK}	Input/output clamp current	P-port	$V_O < 0$ or $V_O > V_{CCP}$		±20	mA
		SDA	$V_O < 0$ or $V_O > V_{CCI}$		±20	
I_{OL}	Continuous output low current	P-port	$V_O = 0$ to V_{CCP}		50	mA
	Continuous output low current	SDA, $\overline{\text{INT}}$	$V_O = 0$ to V_{CCI}		25	
I_{OH}	Continuous output high current	P-port	$V_O = 0$ to V_{CCP}		50	mA
I_{CC}	Continuous current through GND				200	mA
	Continuous current through V_{CCP}				160	
	Continuous current through V_{CCI}				10	
$T_{j(MAX)}$	Maximum junction temperature				135	°C
T_{stg}	Storage temperature			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 [1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCI} [1]	Supply voltage for I^2C pins	SCL, SDA, $\overline{\text{INT}}$	1.65	3.6	V
V_{CCP}	Supply voltage for P-ports	P-ports, ADDR, $\overline{\text{RESET}}$	1.65	3.6	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CCI}$	V_{CCI}	V
		$\overline{\text{RESET}}$	$0.7 \times V_{CCI}$	3.6	
		ADDR, P7–P0	$0.7 \times V_{CCP}$	3.6	
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{\text{RESET}}$	–0.5	$0.3 \times V_{CCI}$	V
		ADDR, P7–P0	–0.5	$0.3 \times V_{CCP}$	
I_{OH}	High-level output current	P00-P07		10	mA

(1) For voltages applied above V_{CCI}, and increase in I_{CC} will result.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
I_{OL} (2)	Low-level output current	P00-P07	T_j = 65°C		25	mA
			T_j = 85°C		18	
			T_j = 105°C		9	
			T_j = 125°C		4.5	
			T_j = 135°C		3.5	
		$\overline{INT}$, SDA	T_j = 85°C		6	
			T_j = 105°C		3	
			T_j = 125°C		1.8	
			T_j = 135°C		1.5	
T_A	Operating free-air temperature			–40	125	°C

(2) The values shown apply to specific junction temperature. See the *Calculating Junction Temperature and Power Dissipation* section on how to calculate the junction temperature.

6.4 Thermal Information

THERMAL METRIC (1)		TCA6408A-Q1 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, V_{CCI} = 1.65 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCP}	MIN	TYP (1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 3.6 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CCP} rising (2)	$V_I = V_{CCP}$ or GND, I_O = 0	1.65 V to 3.6 V		1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CCP} falling (2)	$V_I = V_{CCP}$ or GND, I_O = 0	1.65 V to 3.6 V	0.6	1		V
V_{OH}	P-port high-level output voltage	I_{OH} = –8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			3.6 V	3.3			
		I_{OH} = –10 mA	1.65 V	1.0			
			2.3 V	1.7			
			3 V	2.5			
			3.6 V	3.2			

(1) All typical values are at nominal supply voltage (1.8-V, 2.5-V, or 3.3-V V_{CC}) and T_A = 25°C.
(2) When power (from 0 V) is applied to V_{CCP}, an internal power-on reset holds the TCA6408A-Q1 in a reset condition until V_{CCP} has reached V_{PORR}. At that time, the reset condition is released, and the TCA6408A-Q1 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CCP} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

Electrical Characteristics (continued)

over recommended operating free-air temperature range, V_{CCI} = 1.65 V to 3.6 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCP}	MIN	TYP[(1)]	MAX	UNIT
V_{OL}	P-port low-level output voltage		I_{OL} = 8 mA	1.65 V			0.45	V
				2.3 V			0.25	
				3 V			0.25	
				3.6 V			0.23	
			I_{OL} = 10 mA	1.65 V			0.6	
				2.3 V			0.3	
				3 V			0.25	
				3.6 V			0.23	
I_{OL}	SDA		V_{OL} = 0.4 V	1.65 V to 3.6 V	3			mA
	$\overline{INT}$				3	15		
I_I	SCL, SDA, $\overline{RESET}$		$V_I = V_{CCI}$ or GND	1.65 V to 3.6 V			±0.1	μA
	ADDR		$V_I = V_{CCP}$ or GND				±0.1	
I_{IH}	P-port		$V_I = V_{CCP}$	1.65 V to 3.6 V			1	μA
I_{IL}	P-port		V_I = GND	1.65 V to 3.6 V			1	μA
I_{CC} ($I_{CCI} + I_{CCP}$)	Operating mode	SDA, P-port, ADDR, $\overline{RESET}$	$V_I = V_{CC}$ or GND, I/O = inputs, f_{SCL} = 400 kHz, No load	2.3 V to 3.6 V		9	36	μA
				1.65 V to 2.3 V		5	33	
	Standby mode	SCL, SDA, P-port, ADDR, $\overline{RESET}$	$V_I = V_{CC}$ or GND, I/O = inputs, f_{SCL} = 0 kHz, No load	2.3 V to 3.6 V		1.2	10	
				1.65 V to 2.3 V		0.6	7	
ΔI_{CCI}	Additional current in standby mode	SCL, SDA	One input at V_{CCI} – 0.6 V, Other inputs at V_{CCI} or GND	1.65 V to 3.6 V		6	10	μA
		$\overline{RESET}$	$\overline{RESET}$ at V_{CCI} – 0.6 V, Other inputs at V_{CCI} or GND			6	55	
ΔI_{CCP}		P-port, ADDR	One input at V_{CCP} – 0.6 V, Other inputs at V_{CCP} or GND	1.65 V to 3.6 V		6	80	μA
C_i	SCL		$V_I = V_{CCI}$ or GND	1.65 V to 3.6 V		7	9	pF
C_{io}	SDA		$V_{IO} = V_{CCI}$ or GND	1.65 V to 3.6 V		8	10.5	pF
	P-port		$V_{IO} = V_{CCP}$ or GND			7	8	

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 17)

		MIN	MAX	UNIT
I²C BUS—STANDARD MODE				
f_{scl}	I²C clock frequency	0	100	kHz
t_{sch}	I²C clock high time	4		μs
t_{scl}	I²C clock low time	4.7		μs
t_{sp}	I²C spike time	0	50	ns
t_{sds}	I²C serial data setup time	250		ns
t_{sdh}	I²C serial data hold time	0		ns
t_{icr}	I²C input rise time		1000	ns
t_{icf}	I²C input fall time		300	ns
t_{ocf}	I²C output fall time, 10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between Stop and Start	4.7		μs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		μs
t_{sth}	I²C Start or repeater Start condition hold time	4		μs
t_{sps}	I²C Stop condition setup time	4		μs

I^2C Interface Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 17)

		MIN	MAX	UNIT
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid		1	µs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1	µs
I^2C BUS—FAST MODE				
f_{scl}	I^2C clock frequency	0	400	kHz
t_{sch}	I^2C clock high time	0.6		µs
t_{scl}	I^2C clock low time	1.3		µs
t_{sp}	I^2C spike time	0	50	ns
t_{sds}	I^2C serial data setup time	100		ns
t_{sdh}	I^2C serial data hold time	0		ns
t_{icr}	I^2C input rise time	20	300	ns
t_{icf}	I^2C input fall time	20 x (Vcc/ 5.5 V)	300	ns
t_{ocf}	I^2C output fall time, 10-pF to 400-pF bus	20 x (Vcc/ 5.5 V)	300	ns
t_{buf}	I^2C bus free time between Stop and Start	1.3		µs
t_{sts}	I^2C Start or repeater Start condition setup time	0.6		µs
t_{sth}	I^2C Start or repeater Start condition hold time	0.6		µs
t_{sps}	I^2C Stop condition setup time	0.6		µs
$t_{vd(data)}$	Valid data time, SCL low to SDA output valid		1	µs
$t_{vd(ack)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1	µs

6.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 20)

		MIN	MAX	UNIT
I^2C BUS—STANDARD and FAST MODE				
t_W	Reset pulse duration	40		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset	600		ns

6.8 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 17)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
I^2C BUS—STANDARD and FAST MODE						
t_{iv}	Interrupt valid time	P-Port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P7–P0		400	ns
t_{ps}	Input data setup time	P-Port	SCL	0		ns
t_{ph}	Input data hold time	P-Port	SCL	300		ns

6.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

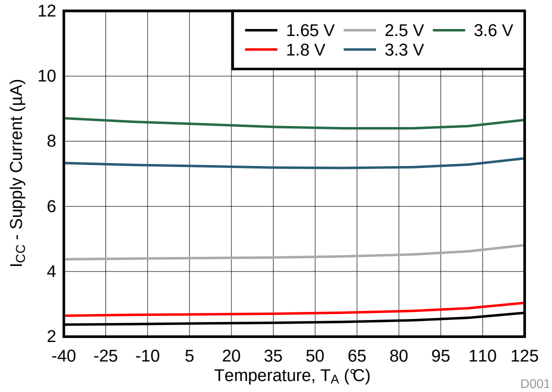


Figure 1. Supply Current vs Temperature

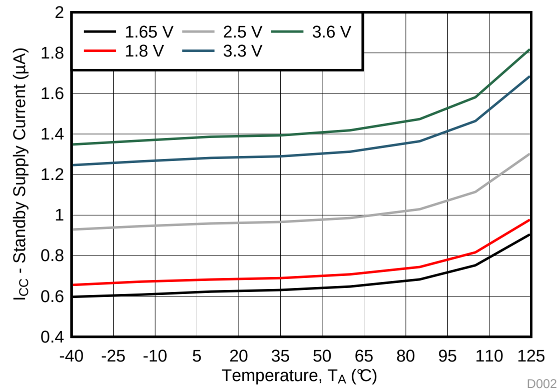


Figure 2. Standby Supply Current vs Temperature

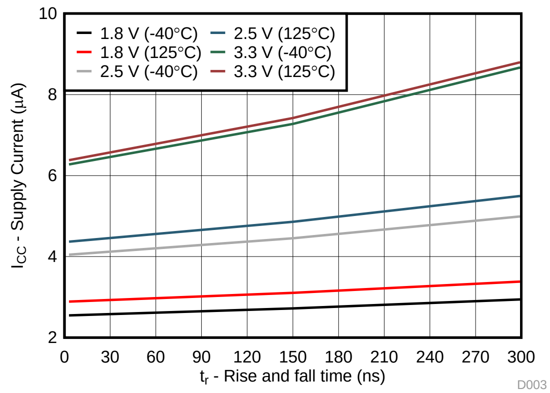


Figure 3. Supply Current vs Rise and Fall Times (t_r)

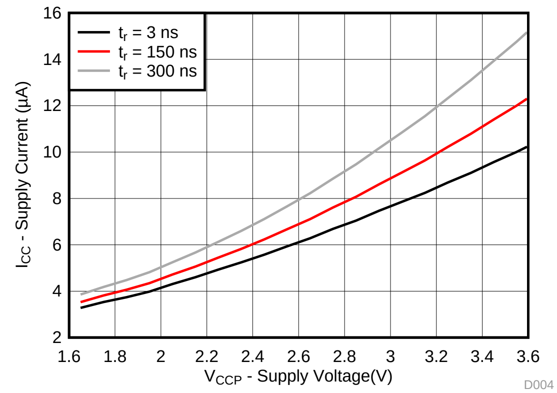


Figure 4. Supply Current vs Supply Voltage

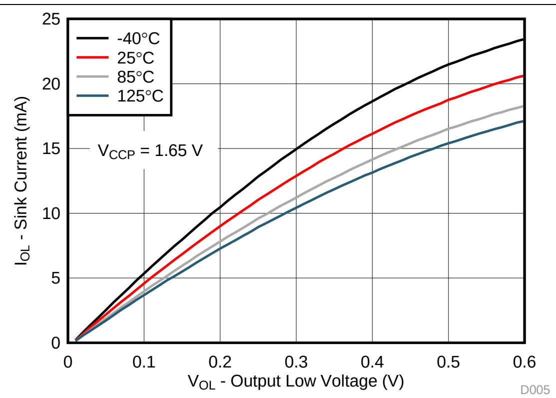


Figure 5. I/O Sink Current vs Output Low Voltage (V_{CCP} = 1.65 V)

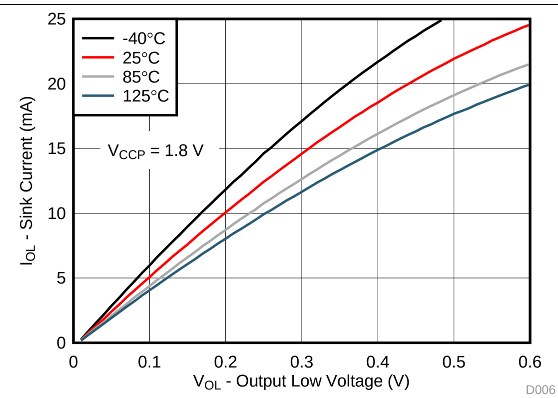


Figure 6. I/O Sink Current vs Output Low Voltage (V_{CCP} = 1.8 V)

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

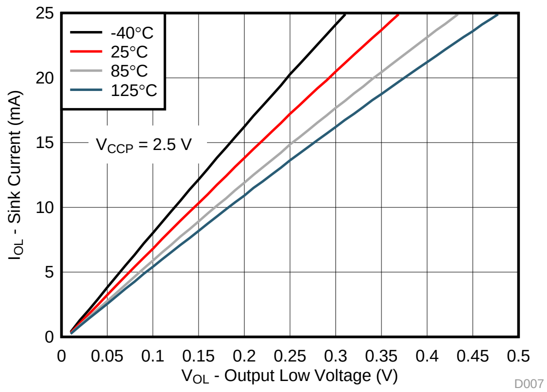


Figure 7. I/O Sink Current vs Output Low Voltage (V_{CCP} = 2.5 V)

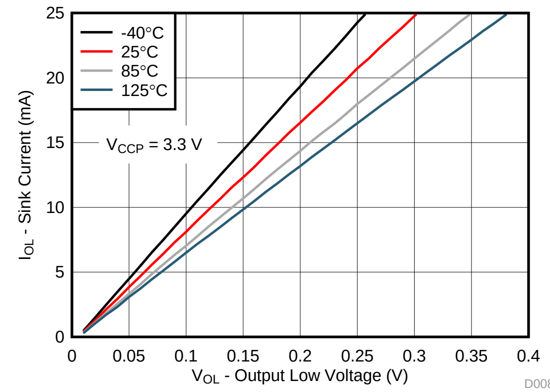


Figure 8. I/O Sink Current vs Output Low Voltage (V_{CCP} = 3.3 V)

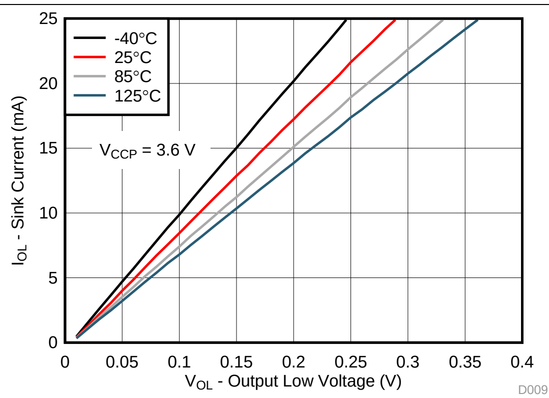


Figure 9. I/O Sink Current vs Temperature (V_{CCP} = 3.6 V)

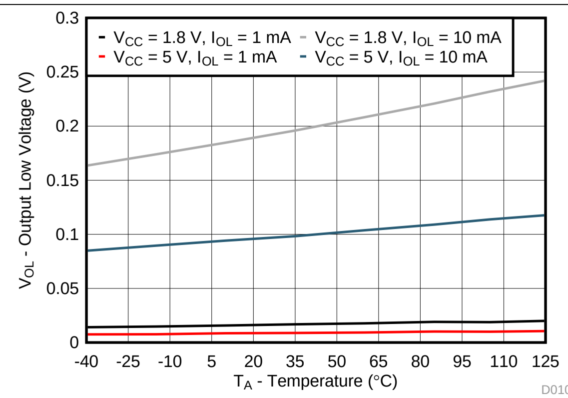


Figure 10. I/O Low Voltage vs Temperature

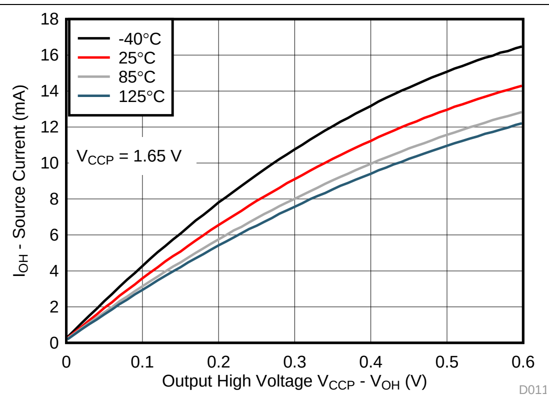


Figure 11. I/O Source Current vs Output High Voltage (V_{CCP} = 1.65 V)

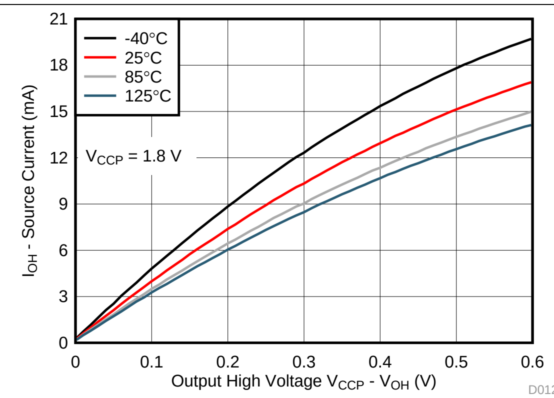


Figure 12. I/O Source Current vs Output High Voltage (V_{CCP} = 1.8 V)

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

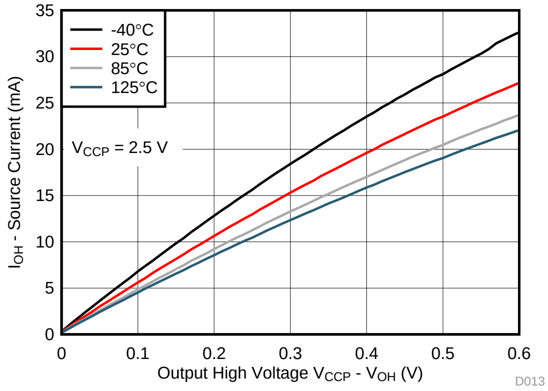


Figure 13. I/O Source Current vs Output High Voltage (V_{CCP} = 2.5 V)

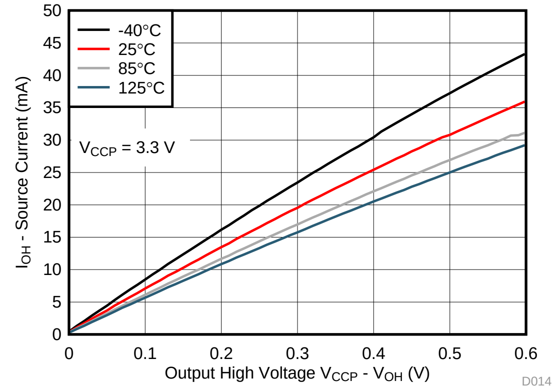


Figure 14. I/O Source Current vs Output High Voltage (V_{CCP} = 3.3 V)

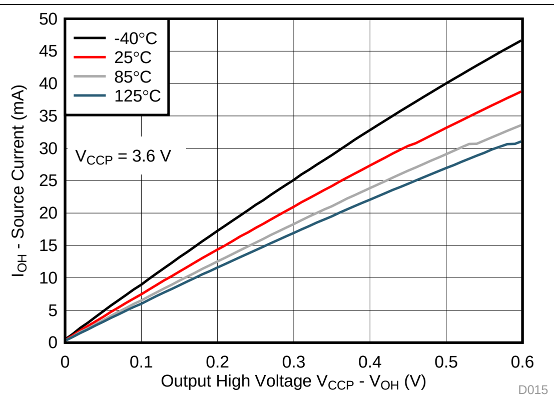


Figure 15. I/O Source Current vs Output High Voltage (V_{CCP} = 3.6 V)

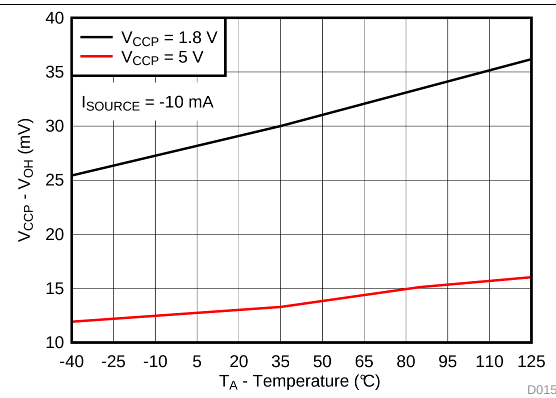
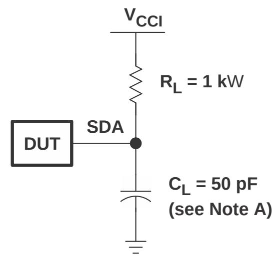
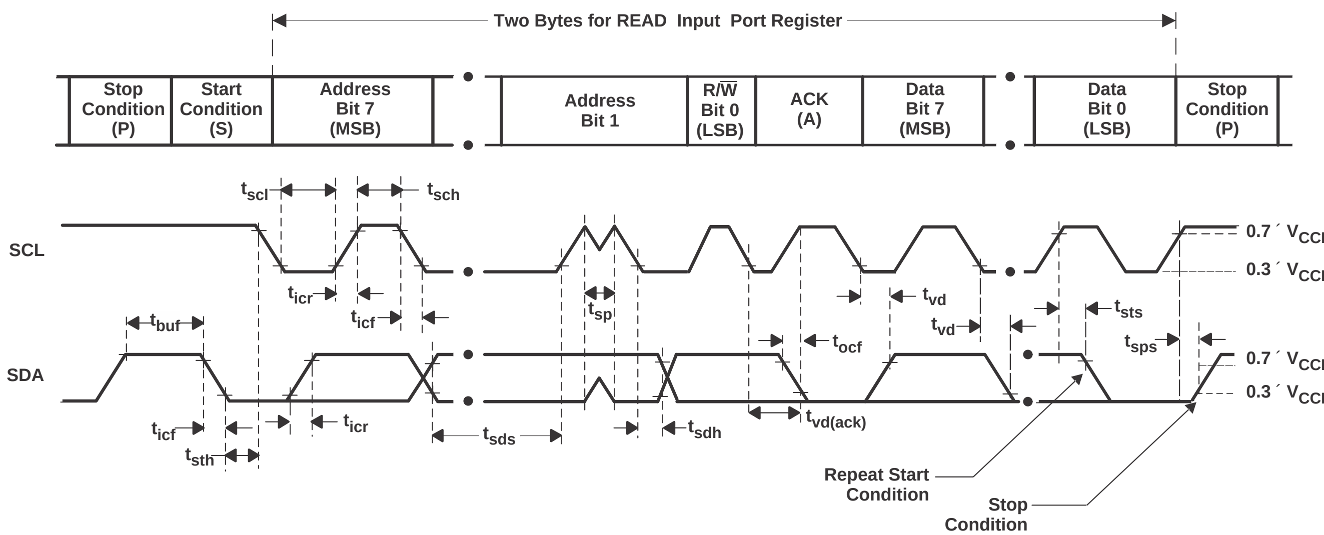


Figure 16. I/O High Voltage vs Temperature

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

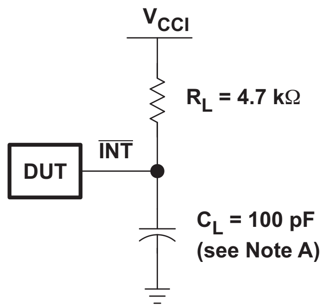
BYTE	DESCRIPTION
1	I^2C address
2	Input register port data

A. C_L includes probe and jig capacitance. t_{ocf} is measured with C_L of 10 pF or 400 pF.

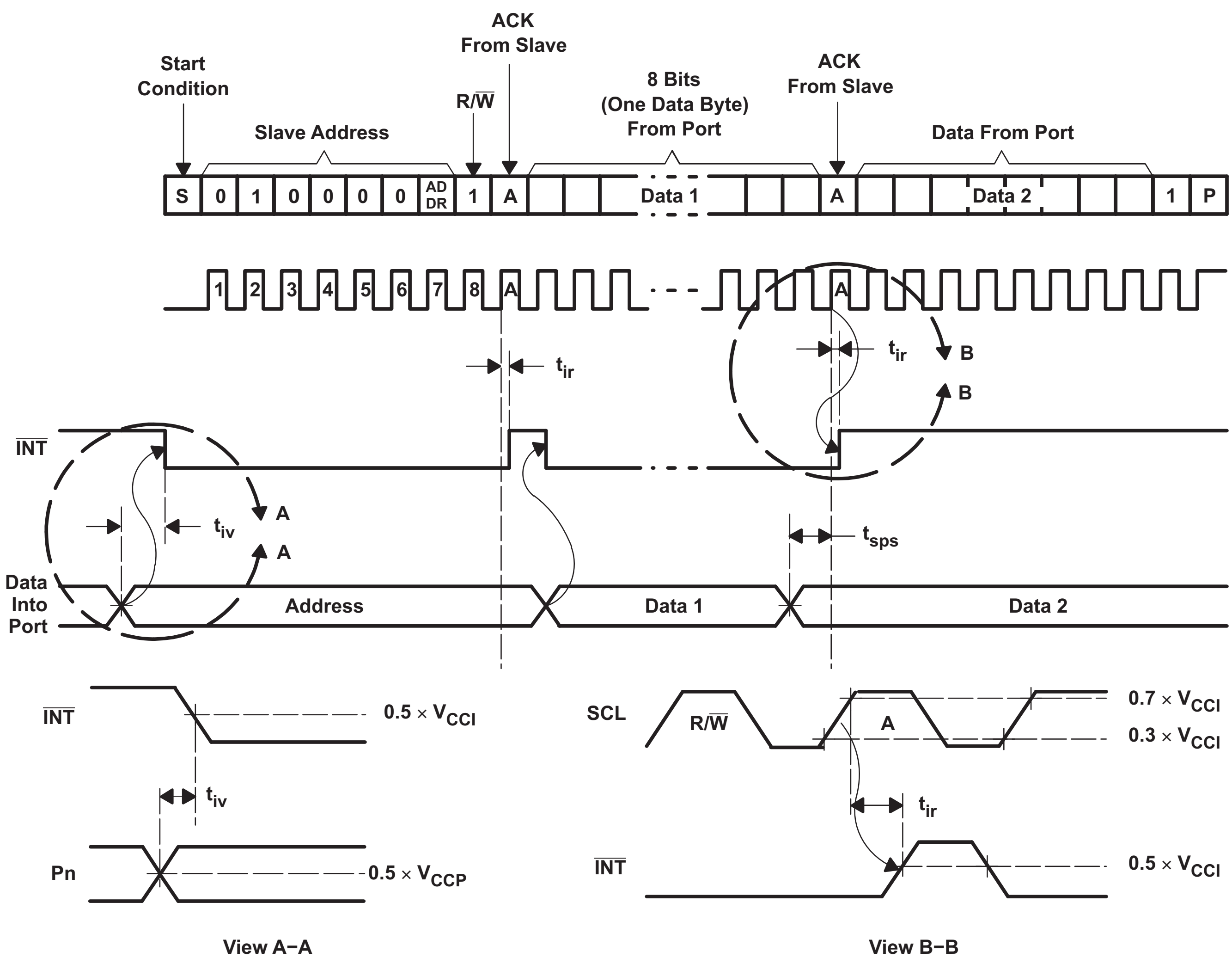
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

Figure 17. I^2C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION

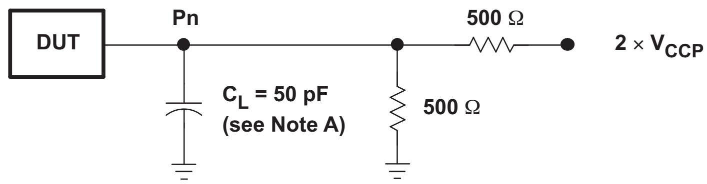


A. C_L includes probe and jig capacitance.

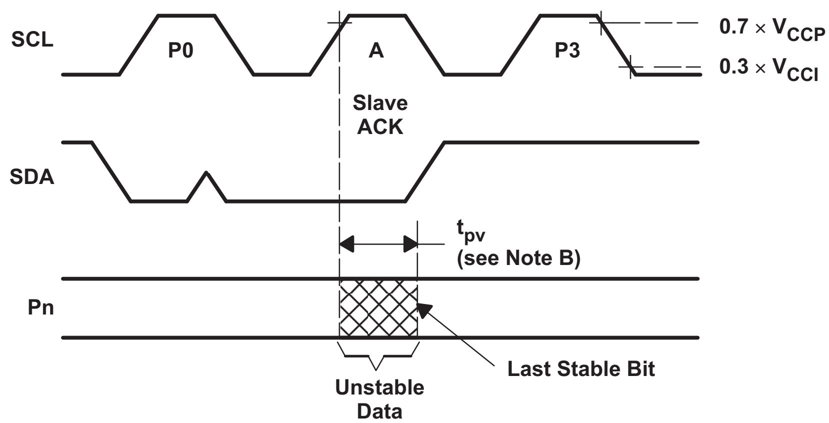
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

Figure 18. Interrupt Load Circuit and Voltage Waveforms

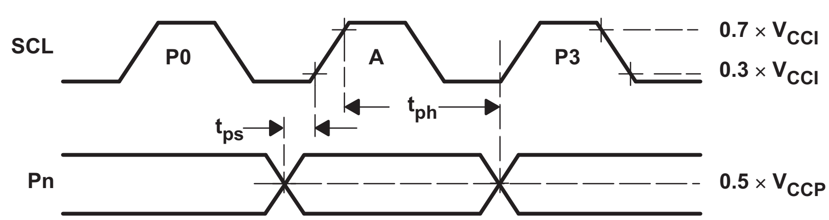
Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE ($R/\overline{W}$ = 0)

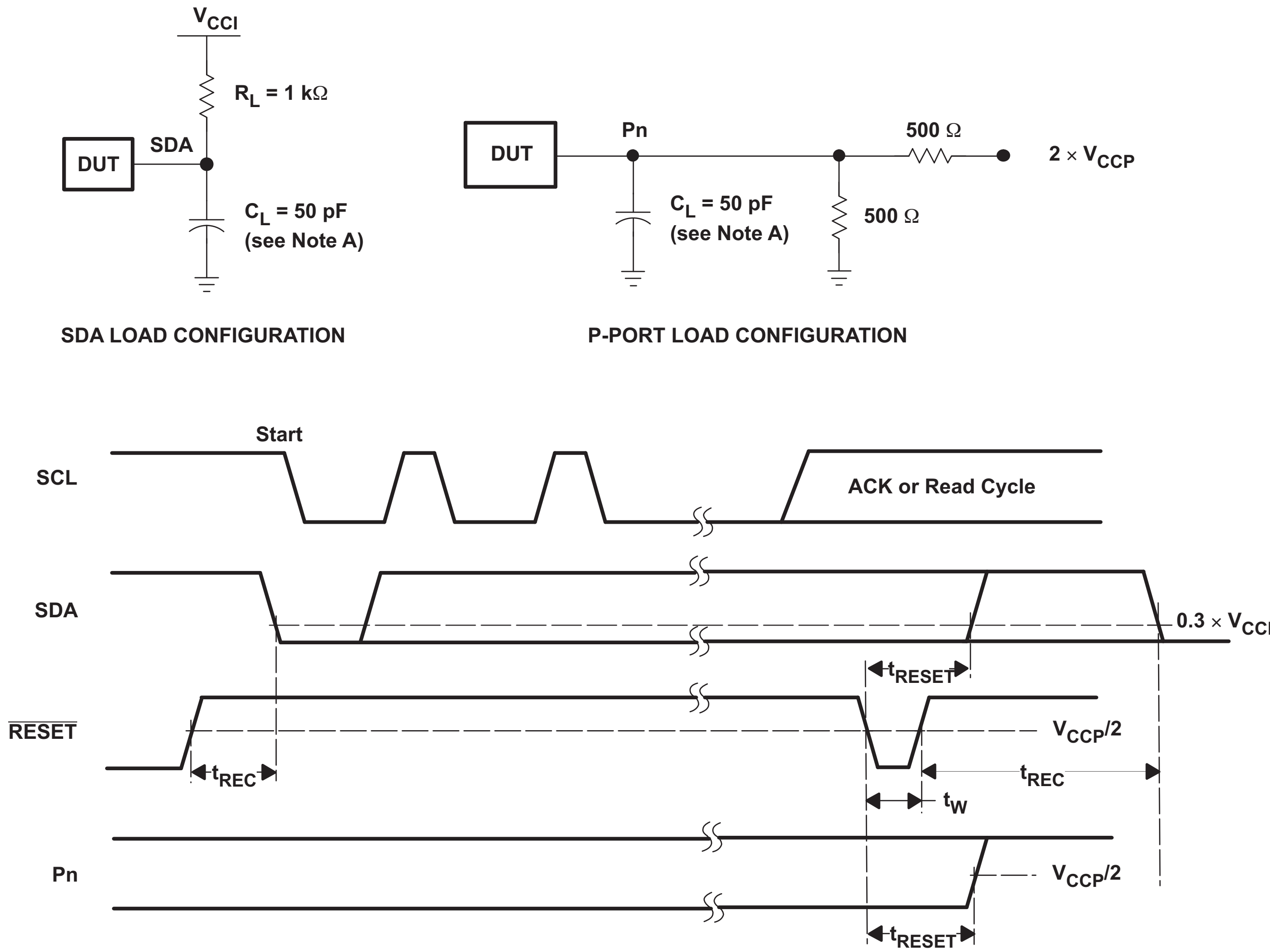


READ MODE ($R/\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 19. P-Port Load Circuit and Timing Waveforms

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. I/Os are configured as inputs.

Figure 20. Reset Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The bidirectional voltage-level translation in the TCA6408A-Q1 is provided through V_{CCI}. V_{CCI} must be connected to the V_{CC} of the external SCL/SDA lines. This indicates the V_{CC} level of the I^2C bus to the TCA6408A-Q1. The voltage level on the P-port of the TCA6408A-Q1 is determined by V_{CCP}.

The TCA6408A-Q1 consists of one 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) Register. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or Output Register. The polarity of the Input Port Register can be inverted with the Polarity Inversion Register. All registers can be read by the system master.

The system master can reset the TCA6408A-Q1 in the event of a timeout or other improper operation by asserting a low in the $\overline{RESET}$ input. The power-on reset puts the registers in their default state and initializes the I^2C/SMBus state machine. The $\overline{RESET}$ pin causes the same reset/initialization to occur without depowering the part.

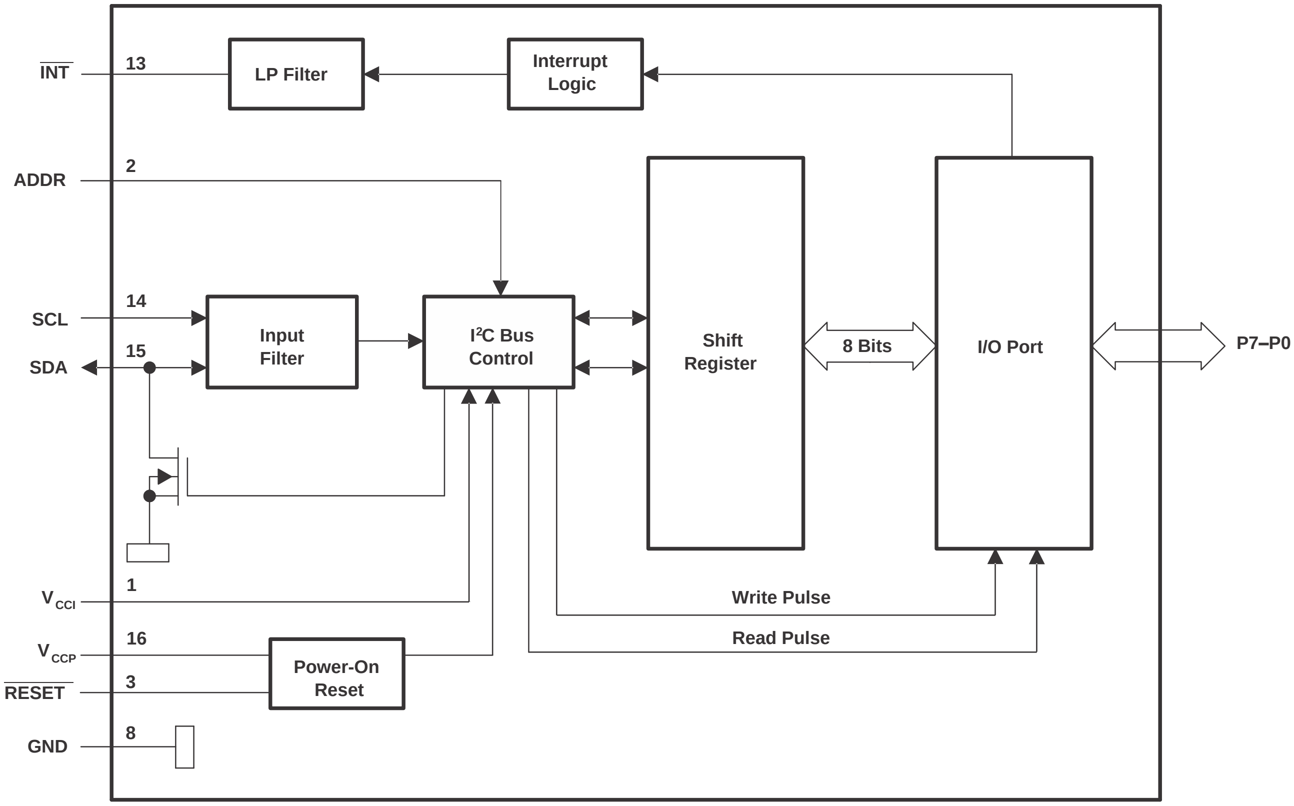
The TCA6408A-Q1 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port Register state and is used to indicate to the system master that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA6408A-Q1 can remain a simple slave device.

The device P-port outputs have high-current sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I^2C address and allow up to two devices to share the same I^2C bus or SMBus.

8.2 Functional Block Diagrams

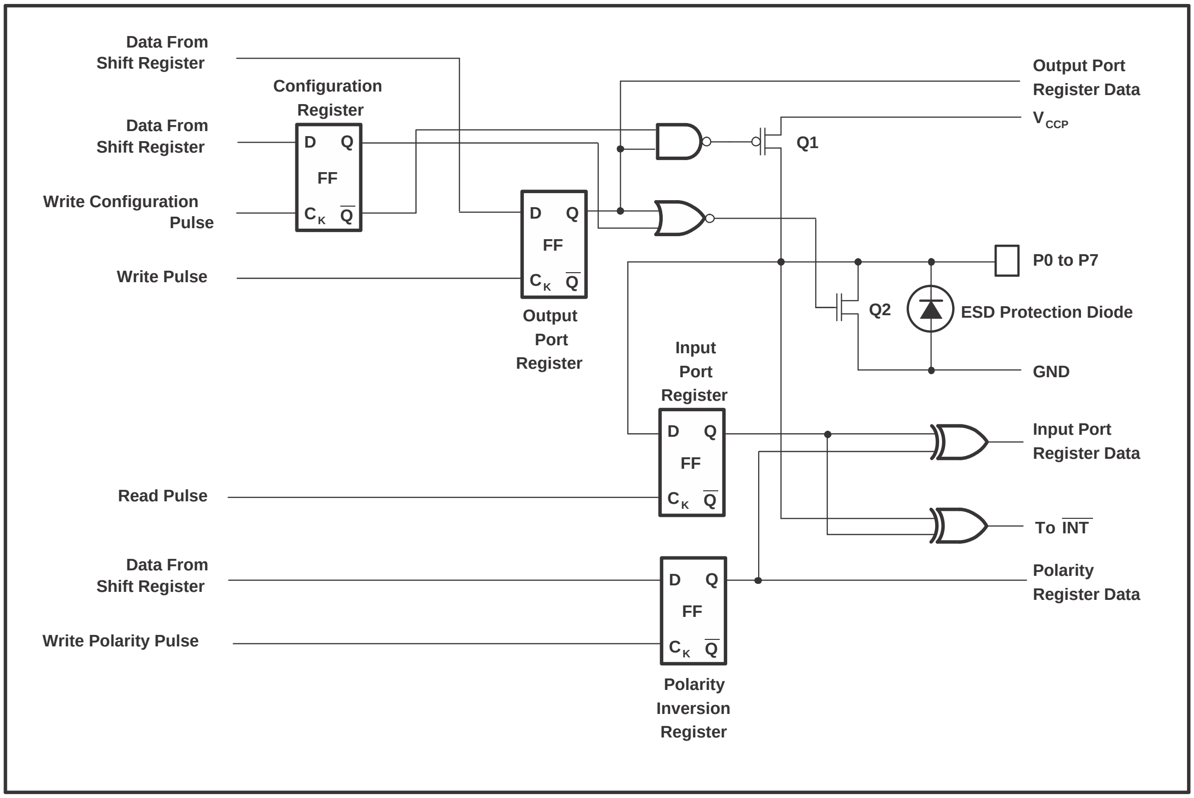


All pin numbers shown are for the PW package.

All I/Os are set to inputs at reset.

Figure 21. Logic Diagram (Positive Logic)

Functional Block Diagrams (continued)



On power up or reset, all registers return to default values.

Figure 22. Simplified Schematic of P0 to P7

8.3 Feature Description

8.3.1 Voltage Translation

Table 1 shows some common supply voltage options for voltage translation between the I^2C bus and the P-ports of the TCA6408A-Q1.

Table 1. Voltage Translation

V_{CCI} (SCL AND SDA OF I^2C MASTER) (V)	V_{CCP} (P-PORT) (V)
1.8	1.8
1.8	2.5
1.8	3.3
2.5	1.8
2.5	2.5
2.5	3.3
3.3	1.8
3.3	2.5
3.3	3.3

8.3.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 3.6 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

8.3.3 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CCP} or V_{CCI}, depending on the application. $\overline{INT}$ must be connected to the voltage source of the device that requires the interrupt information.

8.3.4 Reset Input ($\overline{RESET}$)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the V_{CCP} at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of t_W. The TCA6408A-Q1 registers and I^2C/SMBus state machine are changed to their default state when $\overline{RESET}$ is low (0). When $\overline{RESET}$ is high (1), the I/O levels at the P-port can be changed externally or through the master. This input requires a pull-up resistor to V_{CCI}, if no active connection is used. It is not recommended to assert the $\overline{RESET}$ pin during communication with the TCA6408A-Q1. Assertion of $\overline{RESET}$ during communication can result in data corruption.

8.4 Device Functional Modes

8.4.1 Power-On Reset (POR)

When power (from 0 V) is applied to V_{CCP}, an internal power-on reset holds the TCA6408A-Q1 in a reset condition until V_{CCP} has reached V_{PORR}. At that time, the reset condition is released, and the TCA6408A-Q1 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CCP} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

8.4.2 Powered-Up

When power has been applied to both V_{CCP} and V_{CCI} and a POR has taken place, the device is in a functioning mode. The device is always ready to receive new requests via the I^2C bus.

8.5 Programming

8.5.1 I^2C Interface

The TCA6408A-Q1 has a standard bidirectional I^2C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I^2C bus has a specific device address to differentiate between other slave devices that are on the same I^2C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read.

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. (For further details, see the application report, *I^2C Pull-up Resistor Calculation* (SLVA689)). Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition. See Figure 23 and Figure 24.

The following is the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
   – Master-transmitter sends a START condition and addresses the slave-receiver.
   – Master-transmitter sends data to slave-receiver.
   – Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
   – Master-receiver sends a START condition and addresses the slave-transmitter.
   – Master-receiver sends the requested register to read to slave-transmitter.
   – Master-receiver receives data from the slave-transmitter.

Programming (continued)

– Master-receiver terminates the transfer with a STOP condition.

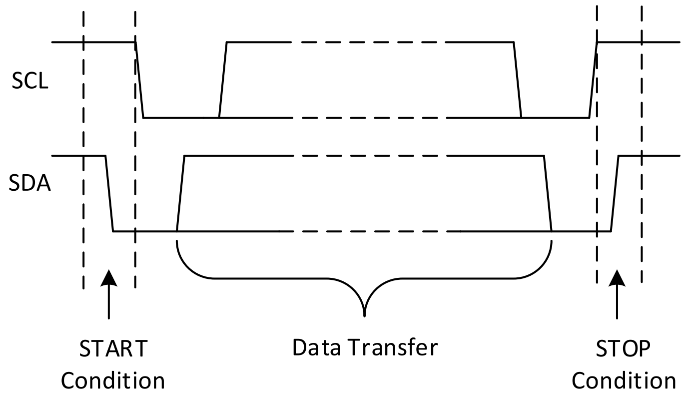


Figure 23. Definition of Start and Stop Conditions

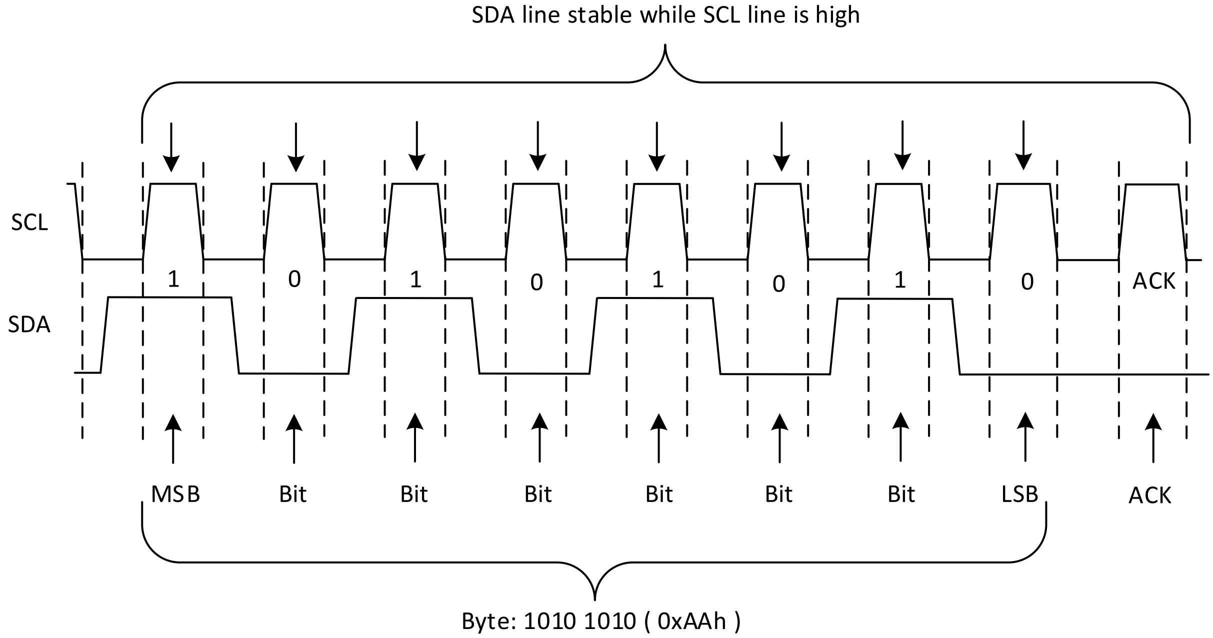


Figure 24. Bit Transfer

Table 2 shows the interface definition for the TCA6408A-Q1 device.

Table 2. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.5.2 Bus Transactions

Data must be sent to and received from the slave devices, and this is accomplished by reading from or writing to registers in the slave device.

Programming (continued)

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

While it is common to have registers in I²C slaves, note that not all slave devices will have registers. Some devices are simple and contain only 1 register, which may be written to directly by sending the register data immediately after the slave address, instead of addressing a register. An example of a single-register device is an 8-bit I²C switch, which is controlled via I²C commands. Since it has 1 bit to enable or disable a channel, there is only 1 register needed, and the master merely writes the register data after the slave address, skipping the register number.

8.5.2.1 Writes

To write on the I²C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave will acknowledge again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

Figure 25 and Figure 26 show an example of writing a single byte to a slave register.

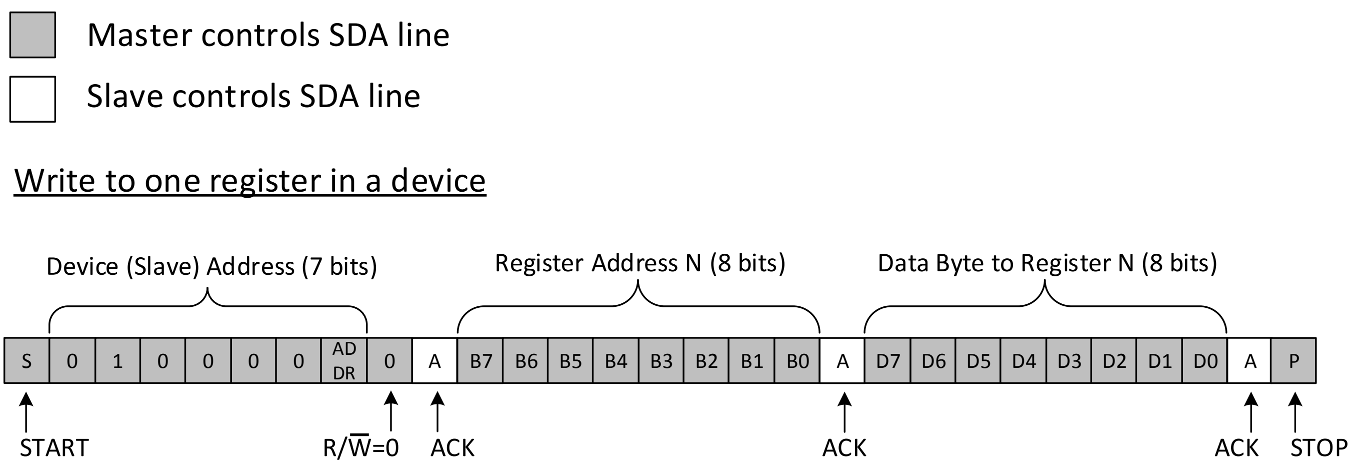


Figure 25. Write to Register

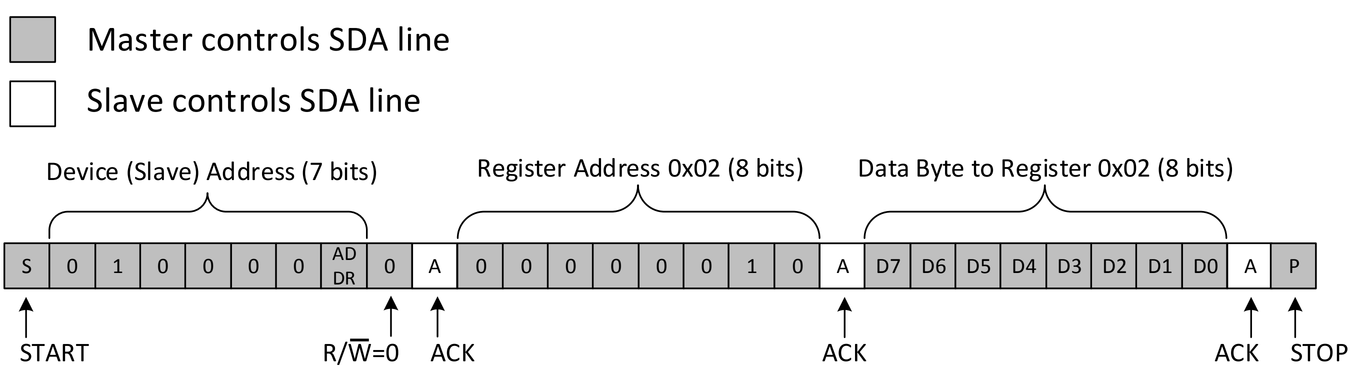


Figure 26. Write to the Polarity Inversion Register

Programming (continued)

8.5.2.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/W̄ bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/W̄ bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

Read transactions that are performed without writing to the address of the device and simply supply the command byte will result in a NACK.

Figure 27 and Figure 28 show an example of reading a single byte from a slave register.

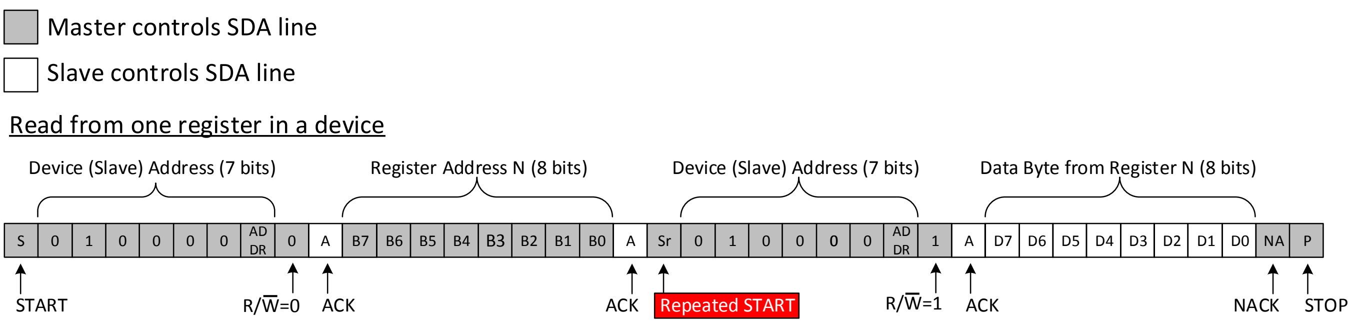
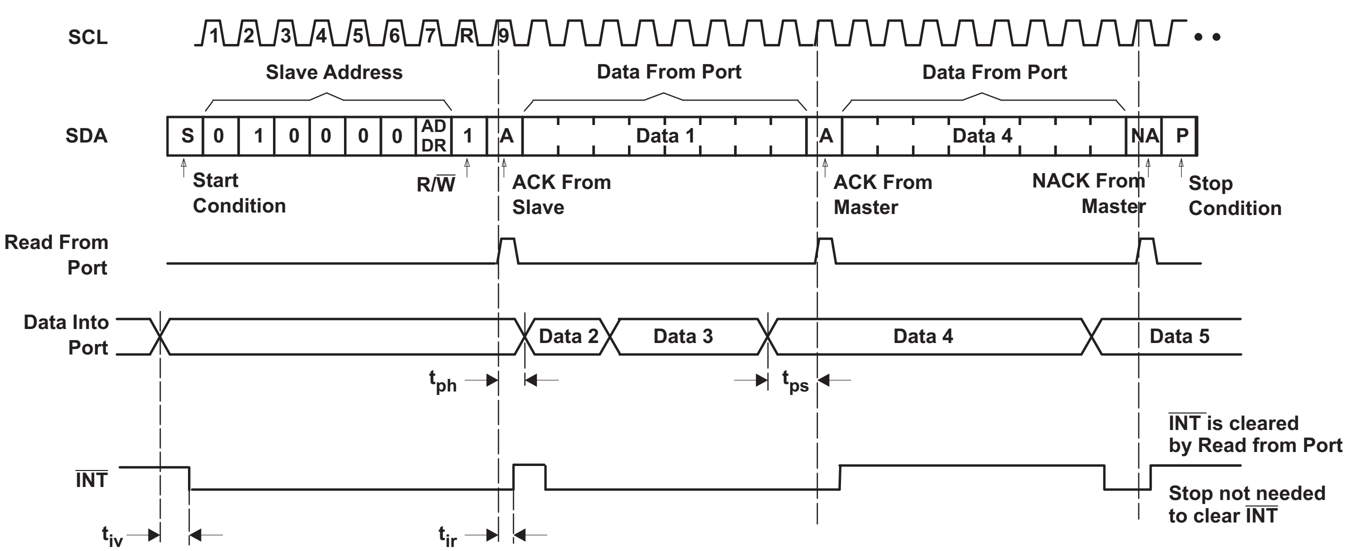


Figure 27. Read from Register



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port Register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from P-port (see Figure 27).

Figure 28. Read from Input Port Register

8.6 Register Map

8.6.1 Device Address

The address of the TCA6408A-Q1 is shown in Figure 29.

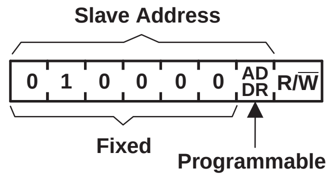


Figure 29. TCA6408A-Q1 Address

Table 3 shows the TCA6408A-Q1 address reference.

Table 3. Address Reference

ADDR	I^2C BUS SLAVE ADDRESS
L	32 (decimal), 20 (hexadecimal)
H	33 (decimal), 21 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte (see Table 4), which is stored in the Control Register in the TCA6408A-Q1. Two bits of this data byte state both the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission. See Figure 30.

B7	B6	B5	B4	B3	B2	B1	B0

Figure 30. Control Register Bits

Table 4. Command Byte

CONTROL REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00	Input Port	Read byte	xxxx xxxx
0	0	0	0	0	0	0	1	01	Output Port	Read/write byte	1111 1111
0	0	0	0	0	0	1	0	02	Polarity Inversion	Read/write byte	0000 0000
0	0	0	0	0	0	1	1	03	Configuration	Read/write byte	1111 1111

8.6.3 Register Descriptions

The Input Port Register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration Register. They act only on read operation. Writes to this register have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port Register will be accessed next. See Table 5.

Table 5. Register 0 (Input Port Register)

BIT	I-7	I-6	I-5	I-4	I-3	I-2	I-1	I-0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port Register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration Register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See Table 6.

Table 6. Register 1 (Output Port Register)

BIT	O-7	O-6	O-5	O-4	O-3	O-2	O-1	O-0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion Register (register 2) allows polarity inversion of pins defined as inputs by the Configuration Register. If a bit in this register is set (written with 1), the polarity of the corresponding port pin is inverted. If a bit in this register is cleared (written with a 0), the original polarity of the corresponding port pin is retained. See Table 7.

Table 7. Register 2 (Polarity Inversion Register)

BIT	N-7	N-6	N-5	N-4	N-3	N-2	N-1	N-0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration Register (register 3) configures the direction of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See Table 8.

Table 8. Register 3 (Configuration Register)

BIT	C-7	C-6	C-5	C-4	C-3	C-2	C-1	C-0
DEFAULT	1	1	1	1	1	1	1	1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

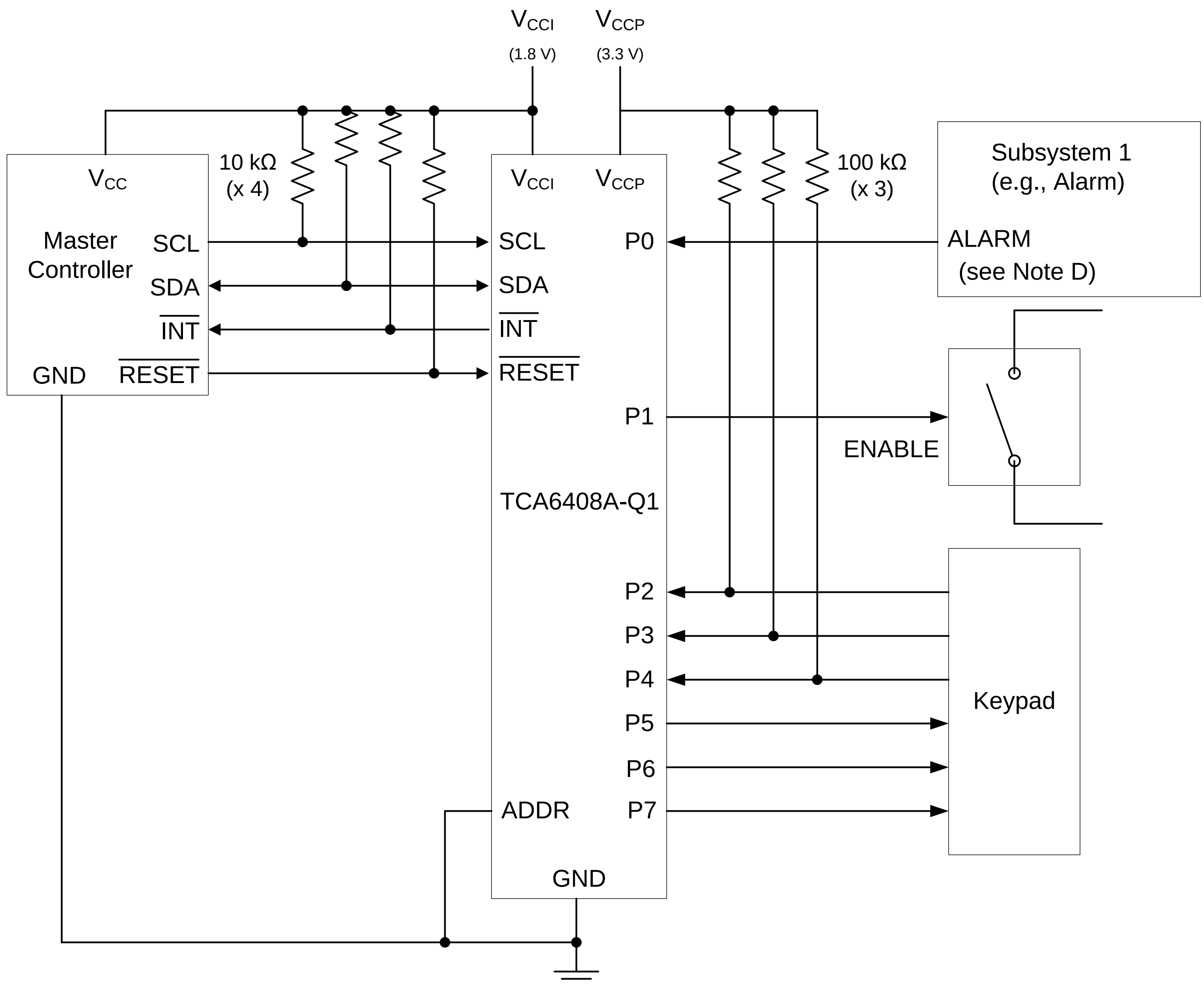
9.1 Application Information

Applications of the TCA6408A-Q1 has this device connected as a slave to an I^2C master (processor), and the I^2C bus may contain any number of other slave devices. The TCA6408A-Q1 is in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.

A typical application of the TCA6408A-Q1 operates with a lower voltage on the master side (V_{CCI}), and a higher voltage on the P-port side (V_{CCP}). The P-ports can be configured as outputs connected to inputs of devices such as enable, reset, power select, the gate of a switch, and LEDs. The P-ports can also be configured as inputs to receive data from interrupts, alarms, status outputs, or push buttons.

9.2 Typical Application

Figure 31 shows an application in which the TCA6408A-Q1 can be used.



A. Device address configured as 0100000 for this example.

B. P0 and P2–P4 are configured as inputs.

C. P1 and P5–P7 are configured as outputs.

D. Resistors are required for inputs (on P-port) that may float. If a driver to an input will never let the input float, a resistor is not needed. Outputs (in the P-port) do not need pull-up resistors.

Figure 31. Typical Application Schematic

9.2.1 Design Requirements

9.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with the TCA6408A-Q1, it is important that the *Recommended Operating Conditions* not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

Typical Application (continued)

θ_{JA} is the standard junction to ambient thermal resistance measurement of the package, as seen in *Thermal Information* table. P_d is the total power dissipation of the device, and the approximation is shown in Equation 2.

$$P_d \approx \left(I_{CC\_STATIC} \times V_{CC}\right) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

Equation 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using Equation 3 to calculate the power dissipation in $\overline{INT}$ or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = \left(I_{OL} \times V_{OL}\right) \quad (3)$$

Equation 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the V_{OL} of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = \left(I_{OH} \times \left(V_{CC} - V_{OH}\right)\right) \quad (4)$$

Equation 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between V_{CC} and the output voltage).

9.2.1.2 Minimizing I_{CC} When I/O is Used to Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 31. The LED acts as a diode, so when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in the *Electrical Characteristics* table shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. Designs that must minimize current consumption, such as battery power applications, must consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off.

Figure 32 shows a high-value resistor in parallel with the LED. Figure 33 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

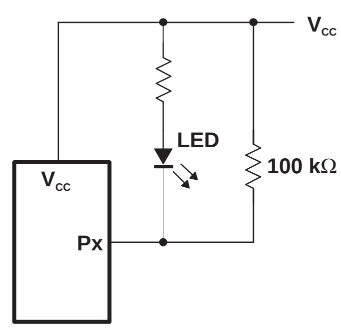


Figure 32. High-Value Resistor in Parallel With LED

Typical Application (continued)

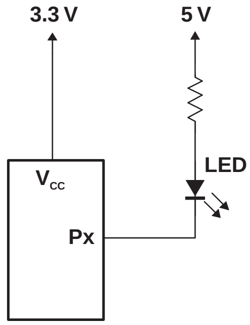


Figure 33. Device Supplied by a Low Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 5.

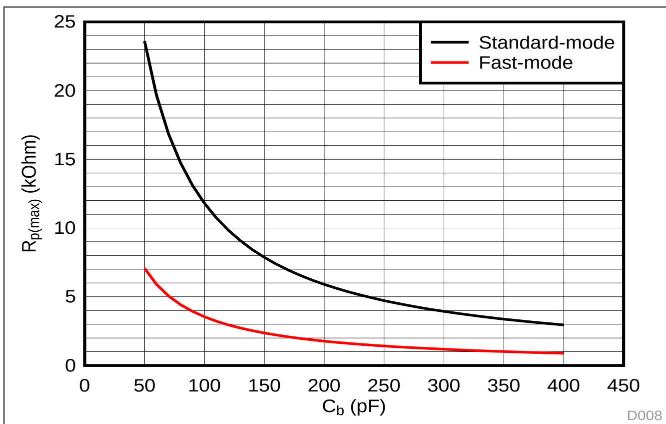
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (5)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (6)$$

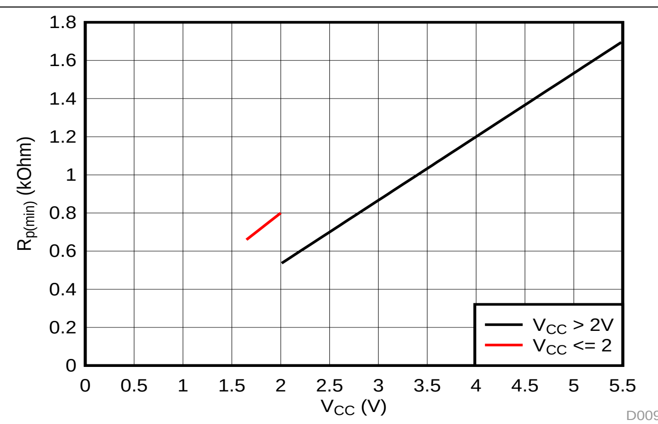
The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA6408A-Q1, C_i for SCL or C_{io} for SDA, the capacitance of wires, connections, traces, and the capacitance of additional slaves on the bus.

9.2.3 Application Curves



Standard-mode: f_{SCL}= 100 kHz, t_r = 1 µs
Fast-mode: f_{SCL}= 400 kHz, t_r= 300 ns_b

Figure 34. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C)



V_{OL} = 0.2 × V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 35. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CCI})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA6408A-Q1 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 36 and Figure 37.

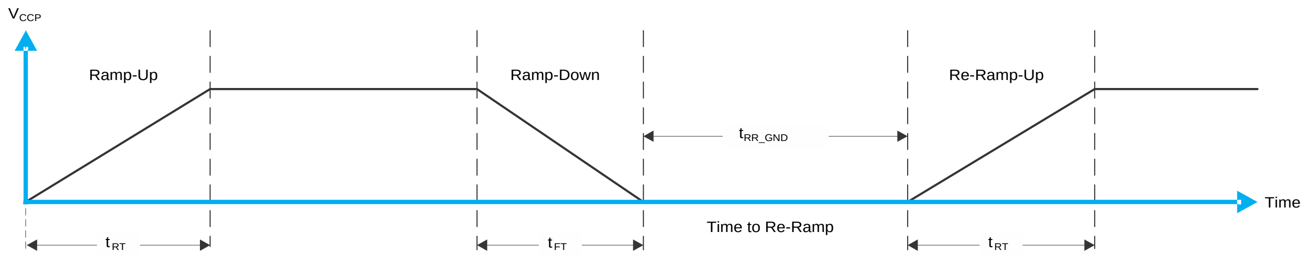


Figure 36. V_{CCP} is Lowered Below 0.2 V and then Ramped Up to V_{CCP}

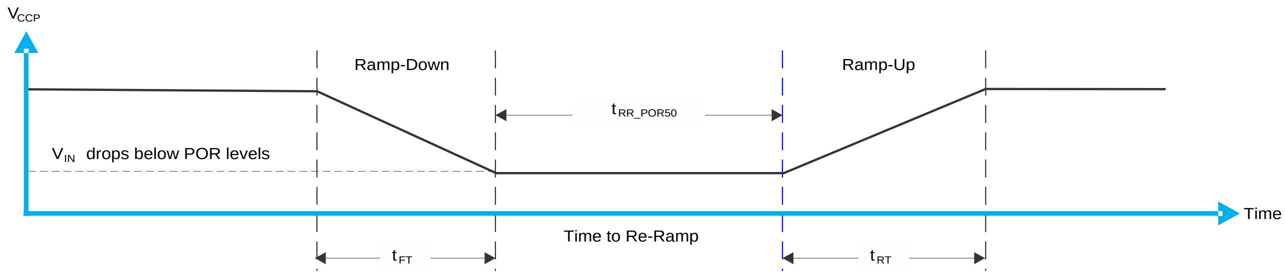


Figure 37. V_{CCP} is Lowered Below the POR Threshold, then Ramped Back Up to V_{CCP}

Table 9 specifies the performance of the power-on reset feature for TCA6408A-Q1 for both types of power-on reset.

Table 9. Recommended Supply Sequencing and Ramp Rates at T_A = 25°C(1)

PARAMETER			MIN	TYP	MAX	UNIT
t_{FT}	Fall rate	See Figure 36	0.1		2000	ms
t_{RT}	Rise rate	See Figure 36	0.1		2000	ms
t_{RR_GND}	Time to re-ramp (when V_{CCP} drops to GND)	See Figure 36	1			µs
t_{RR_POR50}	Time to re-ramp (when V_{CCP} drops to V_{POR_MIN} – 50 mV)	See Figure 37	1			µs
V_{CCP_GH}	Level that V_{CCP} can glitch down from V_{CCP}, but not cause a functional disruption when t_{VCCP_GW} = 1 µs	See Figure 38			1.2	V
V_{CCP_MV}	The minimum voltage that VCC can glitch down to without causing a reset (V_{CC_GH} must not be violated)	See Figure 38	1.5			V
t_{VCCP_GW}	Glitch width that does not cause a functional disruption when t_{VCCP_GH} = 0.5 × V_{CCx}	See Figure 38			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CCP}		0.6	1		V
V_{PORR}	Voltage trip point of POR on rising V_{CCP}			1.2	1.5	V

(1) Not tested. Specified by design.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t_{VCCP_GW}) and height (V_{CCP_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 38 and Table 9 provide more information on how to measure these specifications.

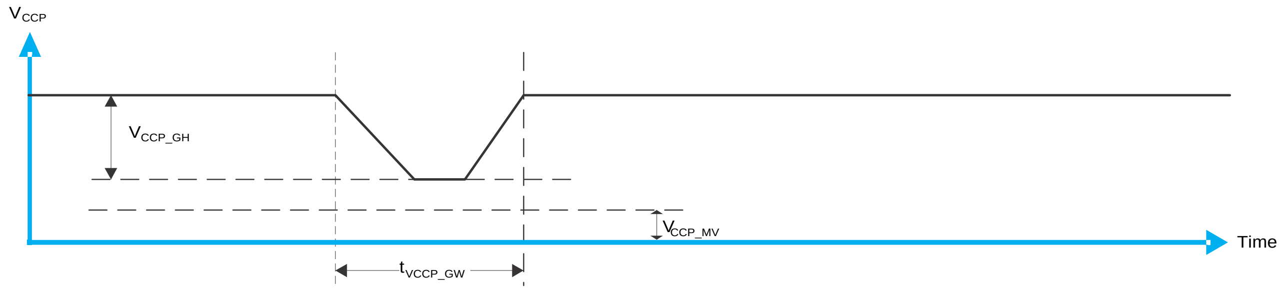


Figure 38. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{PORR} / V_{PORF} is the voltage level at which the reset condition is released/asserted and all the registers and the I^{2}C/SMBus state machine are initialized to their default states (upon a release of a reset condition). The voltage that the device has a reset condition asserted or released differs based on whether V_{CCP} is being lowered to or from 0. Figure 39 and Table 9 provide more details on this specification.

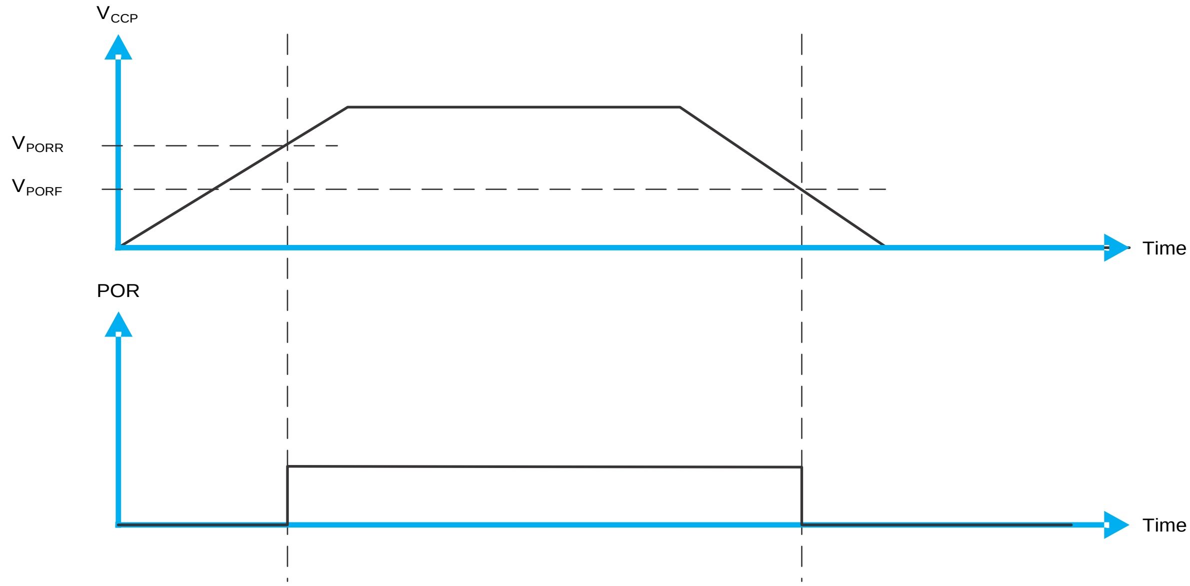


Figure 39. Power On Reset

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA6408A-Q1, common PCB layout practices must be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^{2}C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CCI} and V_{CCP} pins, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA6408A-Q1 as possible. These best practices are shown in *Layout Example*.

For the layout example provided in *Layout Example*, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CCI} and V_{CCP}) and ground (GND). However, a 4-layer board is preferable for boards with higher density signal routing. On a 4-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CCI}, V_{CCP}, or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in *Layout Example*.

11.2 Layout Example

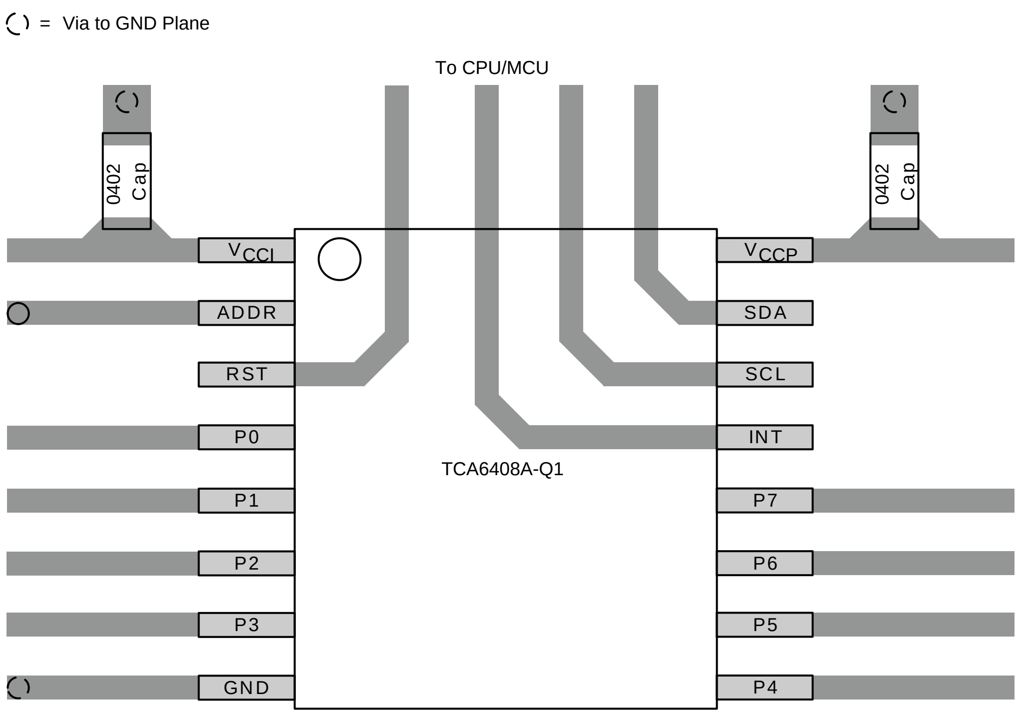


Figure 40. Example Layout (PW Package)

12 器件和文档支持

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA6408AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6408AQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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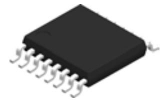
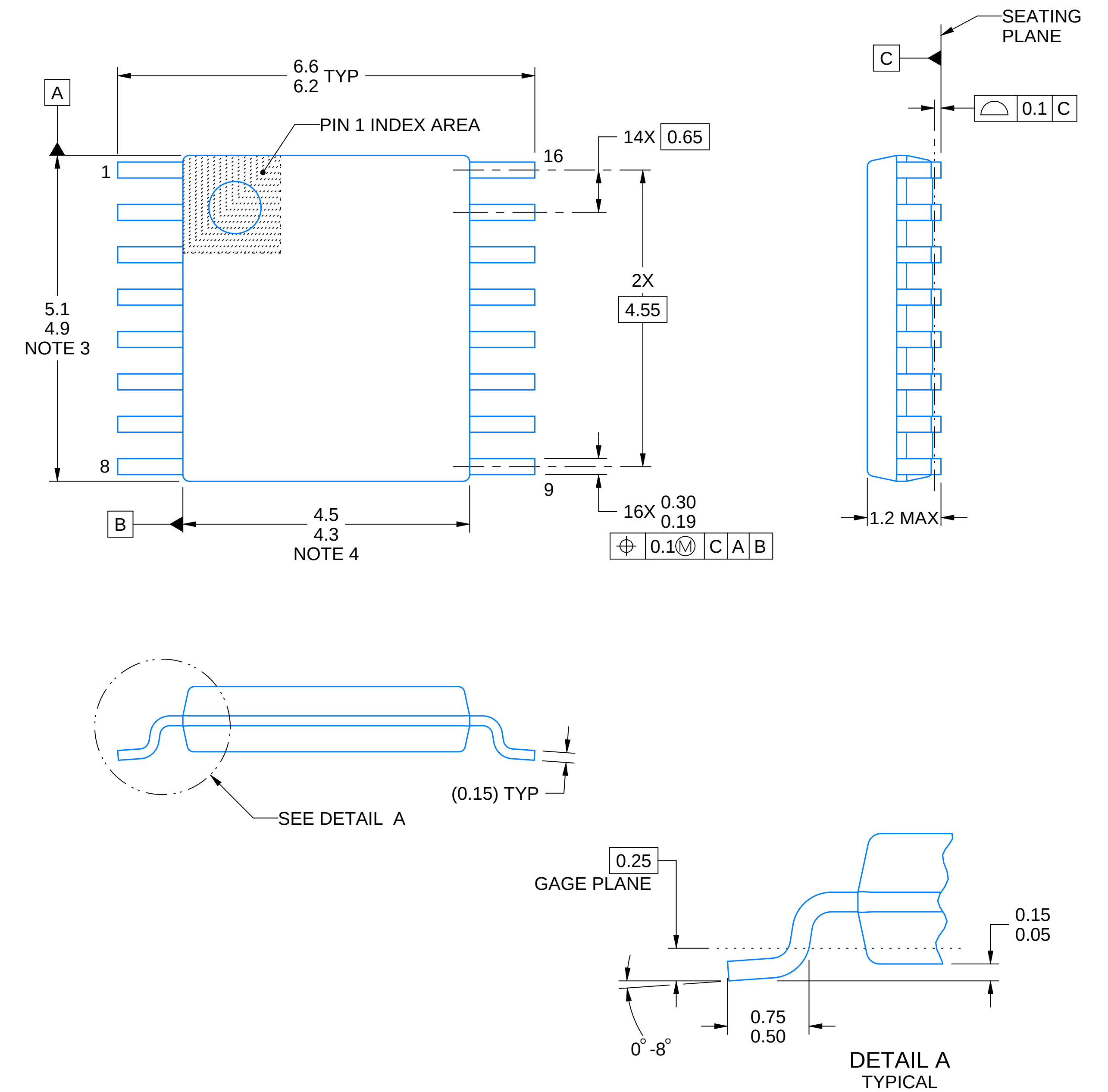


PACKAGE OUTLINE

TSSOP - 1.2 mm max height

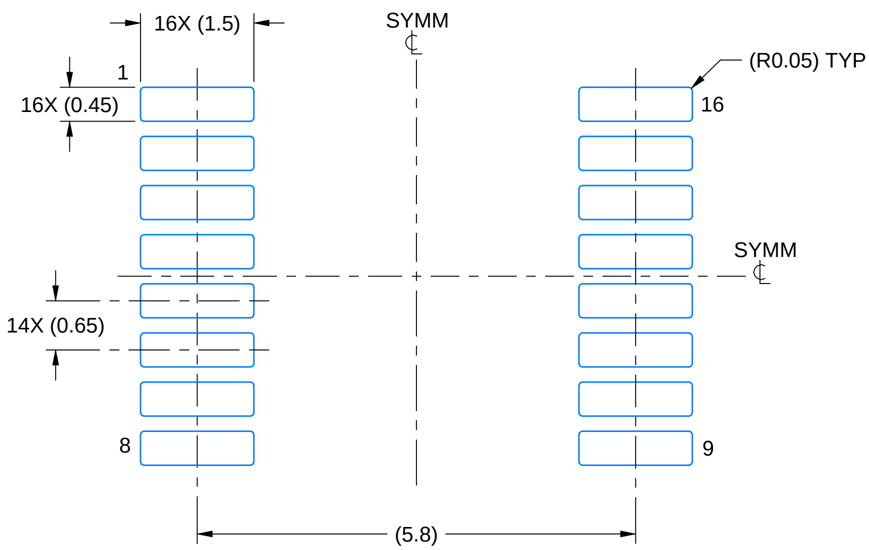
SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



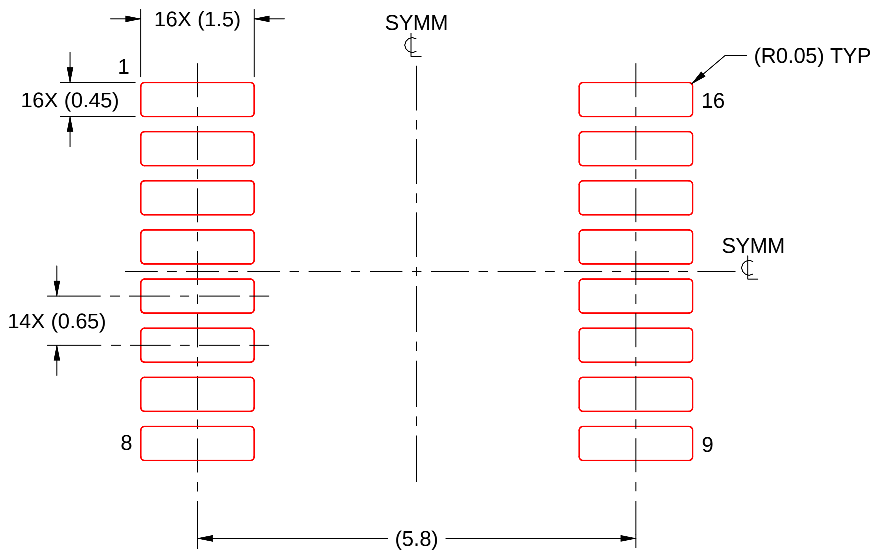
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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