# 具有极性控制功能的 TCAN4420 CAN 收发器

## 1 特性

- 符合 ISO 11898-2 (2016) 物理层标准要求
- 通过 SW（开关）引脚进行外部极性控制
  - 可用于将极性切换为 CAN 总线的正常（默认）或反向配置
- 双电源
  - 5V $V_{CC}$ 引脚用于为 CAN 驱动器和接收器供电
  - 2.8V 至 5V $V_{IO}$ 引脚用于为 RXD、TXD 和 SW 引脚供电
- 宽运行范围
  - ±46V 总线故障保护
  - ±12V 共模
  - –40°C 至 125°C 环境温度
- 保护特性
  - 人体放电模型 (HBM) ESD 保护高达 ±12kV
  - $V_{CC}$ 和 $V_{IO}$ 电源欠压保护
  - TXD 显性超时 (TXD DTO) - 支持低至 9.2kbps 的数据速率
  - 热关断保护 (TSD)
- 优化了未上电时的性能
  - 总线和逻辑终端处于高阻态（运行总线或应用上无负载）
  - 上电/断电无毛刺脉冲运行
- 快速循环时间：150ns

## 2 应用

- 楼宇自动化
  - 楼宇安全网关
  - HVAC 网关和系统控制器
  - 电梯主面板

## 3 说明

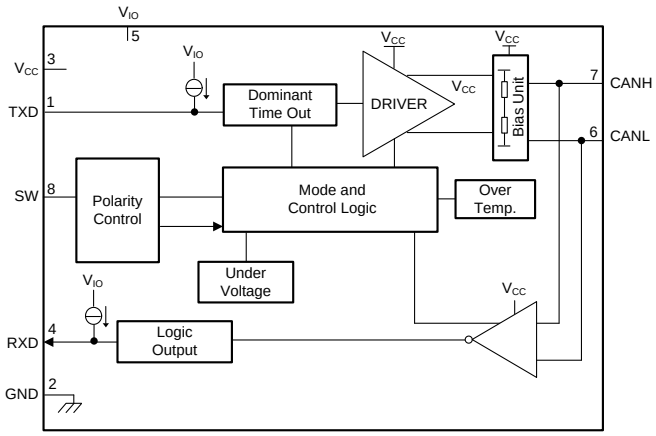
TCAN4420 是一款符合 ISO 11898-2 (2016) 物理层标准规格要求的高速控制器局域网 (CAN) 收发器。该器件还支持通过微控制器由 SW 引脚从外部控制 CAN 总线极性。TCAN4420 包含众多可 实现 器件和 CAN 网络可靠性的保护特性。支持 2.8V 至 5V MCU，且包含可通过 $V_{IO}$ 引脚实现的 I/O 接口。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TCAN4420 | SOIC (D) (8) | 4.90mm x 3.91mm |

(1) 如需了解所有可用型号，请参阅数据表末尾的可订购产品附录。

功能框图



# 目录



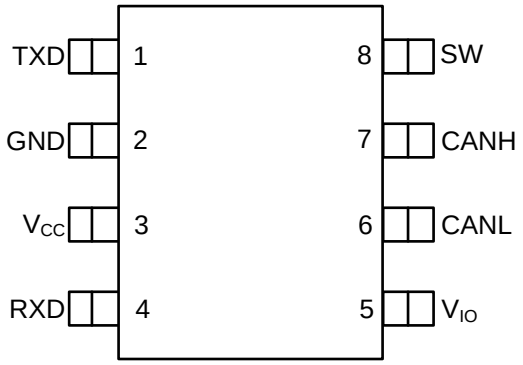
## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| 日期 | 修订版本 | 说明 |
|---|---|---|
| 2017 年 12 月 | * | 初始发行版 |

# 5 Pin Configuration and Functions

**D Package**
**8-Pin SOIC**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| TXD | 1 | Logic Input | CAN transmit data input (LOW for dominant and HIGH for recessive bus states) |
| GND | 2 | Ground | Ground connection |
| $V_{CC}$ | 3 | Power | 5 V ±10% supply voltage |
| RXD | 4 | Logic Output | CAN receive data output (LOW for dominant and HIGH for recessive bus states) |
| $V_{IO}$ | 5 | Power | Transceiver I/O level shifting supply voltage |
| CANL | 6 | Bus I/O | Low level CAN bus input/output line |
| CANH | 7 | Bus I/O | High level CAN bus input/output line |
| SW | 8 | Logic Input | Polarity switch pin. Set to low for normal polarity (default), and high to reverse the polarity of the CAN pins |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.3 | 6 | V |
| $V_{IO}$ | Supply voltage select for I/O level shifter | –0.3 | 6 | |
| $V_{BUS}$ | CAN Bus I/O voltage (CANH, CANL) | –46 | 46 | |
| $V_{Logic\_Input}$ | Logic input terminal voltage | –0.3 | 6 | |
| $V_{RXD}$ | RXD output terminal voltage range | –0.3 | 6 | |
| $I_{O(RXD)}$ | RXD output current | | 8 | mA |
| $T_J$ | Operating virtual junction temperature range, packaged units | –40 | 150 | °C |
| $T_A$ | Ambient temperature | –40 | 125 | |
| $T_{STG}$ | Storage temperature | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 | All pins(1) | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins(2) | ±750 | |

(1) Tested in accordance to AEC-Q100-002.
(2) Tested in accordance to AEC-Q100-011.

## 6.3 ESD Ratings Specifications

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge(1) | Human bodt model (HBM) | CAN bus terminal (CANH, CANL) | ±12000 | V |
| | IEC 61400-4-2 according to IBEE CAN EMC test spec(2) | CANH and CANL terminals to GND(3) (4) | | ±8000 | V |
| | IEC 61400-4-2 Air Discharge(2) | CANH and CANL terminals to GND(3) (4) | | ±15000 | V |
| | ISO7637 Transients according to IBEE CAN EMC test spec(5) | CAN bus terminals (CANH, CANL) | Pulse 1 | –100 | V |
| | | | Pulse 2 | 75 | V |
| | | | Pulse 3a | –150 | V |

(1) System level ESD test, results given here were performed at the system level with appropriate external components such TVS diodes. Different system level configurations may lead to different results.
(2) IEC 61000-4-2 is a system level ESD test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations may lead to different results.
(3) IEC 61000-4-2 is a system level ESD test. Results given here were performed at the system level with appropriate external components such TVS diodes. Different system level configurations may lead to different results.
(4) Testing performed in accordance with 3rd party IBEE Zwickau test method.
(5) ISO7637 is a system level transient test. Results given here are specific to the IBEE CAN EMC Test specification conditions. Different system level configurations may lead to different results.

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IO}$ | Supply Voltage for I/O Level Shifter | 2.8 | | 5.5 | V |
| $I_{OH(RXD)}$ | RXD terminal HIGH level output current | –2 | | | mA |
| $I_{OL(RXD)}$ | RXD terminal LOW level output current | | | 2 | mA |
| $T_A$ | Operational free-air temperature (see Thermal Characteristics table) | –40 | | 125 | °C |

## 6.5 Thermal Information

| THERMAL METRIC(1) | | TCAN4420 SOIC 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 114 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 59.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 9.5 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 58.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.6 Power Supply Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current Normal Mode | Dominant | See 图 6, TXD = 0 V, $R_L$ = 60 Ω, $C_L$ = open, | | 55 | 70 | mA |
| | | Dominant | See 图 6, TXD = 0 V, $R_L$ = 50 Ω, $C_L$ = open, | | 60 | 80 | |
| | | Dominant with bus Fault | See 图 6, TXD = 0 V, STBx = 0 V, CANH = –25 V, $R_L$ = open, $C_L$ = open | | 100 | 180 | |
| | | Recessive | See 图 6, TXD = $V_{CC}$, $R_L$ = 60 Ω, $C_L$ = open, $R_{CM}$ = open, S or STB = 0 V | | 10 | 20 | |
| $UV_{VCC}$ | | Under voltage detection on $V_{CC}$ for protected mode | | 3.5 | | 4.4 | V |
| | | Hysteresis voltage | | | 200 | | mV |
| $UV_{VIO}$ | | Under voltage detection on $V_{IO}$ for protected mode | | 1.3 | | 2.7 | V |
| $P_D$ | Average Power Dissapation | $V_{CC}$ = $V_{IO}$= 5 V, $T_J$ = 25℃, $R_L$ = 60 Ω, Input to TXD at 250 kHz, 25% duty cycle square wave, $C_{L\_RXD}$ = 15 pF. Typical CAN operating conditions at 500 kbps with 25% transmission (domiant) rate. | | | 115 | | mW |
| | | $V_{CC}$ = $V_{IO}$= 5.5 V, $T_J$ = 150℃, $R_L$ = 50 Ω. Input to TXD at 500 kHz, 50% duty cycle square wave, $C_{L\_RXD}$ = 15 pF. Typical high load CAN operating conditions at 1 Mbps with 50% transmission (domiant) rate and loaded network. | | | 268 | | |
| Thermal Shutdown Temperature | | | | | 185 | | ℃ |
| Thermal Shutdown Hysterisis | | | | | 15 | | |

## 6.7 AC and DC Electrical Characteristics

All typical values are at 25°C and supply voltages of $V_{CC}$ = 5 V. $R_L$ = 60 Ω over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Driver Electrical Characteristics** | | | | | | | |
| $V_{O(D)}$ | Bus output voltage (dominant) | CANH | See 图 8 and 图 9, TXD = 0 V, $R_L$ = 60 Ω, $C_L$ = open, $R_{CM}$ = open | 2.75 | | 4.5 | V |
| | | CANL | | 0.5 | | 2.25 | V |
| $V_{O(R)}$ | Bus output voltage (recessive) | | See 图 6 and 图 9, TXD = $V_{CC}$, $R_L$ = open (no load), $R_{CM}$ = open | 2 | 0.5 x $V_{CC}$ | 3 | V |
| $V_{OD(D)}$ | Differential output voltage (dominant) | | See 图 6 and 图 9, TXD = 0 V, 50 Ω ≤ $R_L$ ≤ 65 Ω, $C_L$ = open, $R_{CM}$ = open 4.75 V ≤ $V_{CC}$ ≤ 5.25 V | 1.5 | | 3 | V |
| | | | See 图 6 and 图 9, TXD = 0 V, 50 Ω ≤ $R_L$ ≤ 65 Ω, $C_L$ = open, $R_{CM}$ = open 4.5 V ≤ $V_{CC}$ ≤ 5.5 V | 1.3 | | 3.2 | V |
| $V_{OD(R)}$ | Differential output voltage (recessive) | | See 图 6 and 图 9, TXD = $V_{CC}$, $R_L$ = 60 Ω, $C_L$ = open, $R_{CM}$ = open | –120 | | 12 | mV |
| | | | See图 6 and 图 9,TXD = $V_{CC}$, $R_L$ = open, $C_L$ = open, $R_{CM}$ = open | –50 | | 50 | mV |
| $V_{SYM}$ | Output symmetry (dominant or recessive) ($V_{CC}$ - $V_{O(CANH)}$ - $V_{O(CANL)}$) | | See 图 6 and 图 9, $R_L$ = 60 Ω, $C_L$ = open, $R_{CM}$ = open | –400 | | 400 | mV |
| $I_{OS(DOM)}$ | Short-circuit steady-state output current, Dominant | | See 图 6 and 图 12, $V_{(CAN\_H)}$ ≤ –5 V, CANL = open, TXD = 0 V | –115 | | | mA |
| | | | See 图 6 and 图 12, $V_{(CAN\_L)}$ = 40 V, CANH = open, TXD = 0 V | | | 115 | mA |
| $I_{OS(REC)}$ | Short-circuit steady-state output current, Recessive | | See 图 6 and 图 12, –27 V ≤ $V_{BUS}$ ≤ 32 V, $V_{BUS}$ = CANH = CANL | –5 | | 5 | mA |
| **Receiver Electrical Characteristics** | | | | | | | |
| $V_{IT}$ | Input threshold voltage | | See 图 10 | 500 | | 900 | mV |
| $V_{HYS}$ | Hysteresis voltage for input threshold | | | | 120 | | mV |
| $V_{CM}$ | Common Mode Range | | | –12 | | 12 | V |
| $I_{IOFF(LKG)}$ | Power-off (unpowered) bus input leakage current | | CANH = CANL = 5 V, $V_{CC}$ to GND via 0 Ω | | 5 | | µA |

## AC and DC Electrical Characteristics (continued)

All typical values are at 25°C and supply voltages of $V_{CC}$ = 5 V. $R_L$ = 60 Ω over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_I$ | Input capacitance to ground (CANH or CANL) | TXD = $V_{CC}$ = $V_{IO}$ | | 40 | | pF |
| $C_{ID}$ | Differential input capacitance | | | 20 | | pF |
| $R_{ID}$ | Differential input resistance | | 20 | | 80 | kΩ |
| $R_{IN}$ | Single Ended Input resistance (CANH or CANL) | | 10 | | 40 | kΩ |
| $R_{IN(M)}$ | Input resistance matching: [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 % | $V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V | –1% | | 1% | |
| **$V_{IO}$ PIN** | | | | | | |
| $V_{IO}$ | Supply voltage on $V_{IO}$ pin | | 2.8 | | 5.5 | V |
| $I_{IO}$ | Supply current on $V_{IO}$ pin | RXD pin floating, TXD = 0 V | | | 350 | µA |
| | | RXD pin floating, TXD = 5 | | | 50 | µA |
| **TXD Terminal (CAN Transmit Data Input)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7$V_{IO}$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.3$V_{IO}$ | V |
| $I_{IH}$ | High-level input leakage current | $V_{TXD}$ = $V_{IO}$ = $V_{CC}$ = 5.5 V | –2.5 | 0 | 1 | µA |
| $I_{IL}$ | Low-level input leakage current | $V_{TXD}$ = 0 V, $V_{CC}$ = 5.5 V | –200 | | –6 | µA |
| $I_{LKG(OFF)}$ | Unpowered leakage current | $V_{TXD}$ = 5.5 V, $V_{IO}$ = $V_{CC}$ = 0 V | –1 | 0 | 1 | µA |
| $C_I$ | Input Capacitance | $V_{IN}$ = 0.4 x sin(2 x M x 2 x $10^6$ x t) + 2.5 | | 20 | | pF |
| **RXD Pin (CAN Receive Data Output)** | | | | | | |
| $V_{OH}$ | High-level input voltage | See 图 10, $I_O$ = –2 mA | 0.8$V_{IO}$ | | | V |
| $V_{OL}$ | Low-level input voltage | See 图 10, $I_O$ = –2 mA | | | 0.2$V_{IO}$ | V |
| $I_{LKG(OFF)}$ | Unpowered leakage current | $V_{RXD}$ = 5.5 V, $V_{IO}$ = $V_{CC}$ = 0 V | –1 | 0 | 1 | µA |
| **SW Pin (Polarity Switch Input)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7$V_{IO}$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.3$V_{IO}$ | V |
| $I_{IH}$ | High-level input leakage current | SW = $V_{IO}$ = $V_{CC}$ = 5.5 V | 0.5 | | 20 | µA |
| $I_{IL}$ | Low-level input leakage current | SW = 0 V, $V_{CC}$ = 5.5 V | –1 | | 1 | µA |
| $I_{LKG(OFF)}$ | Unpowered leakage current | SW = 5.5 V, $V_{IO}$ = $V_{CC}$ = 0 V | –1 | 0 | 1 | µA |

## 6.8 Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Switching Characteristics** | | | | | | |
| $t_{pHR}$ | Propagation delay time, high TXD to Driver Recessive | See 图 9, Typical Conditions for DS: $R_L$ = 60 Ω, $C_L$ = 100 pF, $R_{CM}$ = open | | 50 | | ns |
| $t_{pLD}$ | Propagation delay time, low TXD to Driver Dominant | | | 40 | | |
| $t_{sk(p)}$ | Pulse skew (\|$t_{pHR}$ - $t_{pLD}$\|) | | | 10 | | |
| $t_R$ | Differential output signal rise time | | | 25 | | |
| $t_F$ | Differential output signal fall time | | | 25 | | |
| $t_{TXD\_DTO}$ | Dominant time out(1) | See 图 13, $R_L$ = 60 Ω, $C_L$ = open | 1.2 | | 4 | ms |

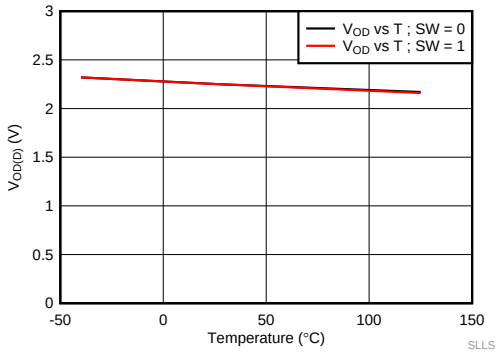
(1) The TXD dominant time out ($t_{TXD\_DTO}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{TXD\_DTO}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{TXD\_DTO}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11/ $t_{TXD\_DTO}$ = 11 bits / 1.2 ms = 9.2 kbps.

## Timing Requirements (continued)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pRH}$ | Propagation delay time, bus recessive input to high RXD_INT output | See 图 10 $C_{L(RXD)}$ = 15 pF Typical Conditions for DS: CANL = 1.5 V, CANH = 3.5 V | | 50 | | ns |
| $t_{pDL}$ | Propagation delay time, bus dominant input to RXD low output | | | 50 | | |
| $t_R$ | Differential output signal rise time | | | 8 | | |
| $t_F$ | Differential output signal fall time | | | 8 | | |
| **Device Switching Characteristics** | | | | | | |
| $t_{(LOOP1)}$ | Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant(2) | See 图 10 Typical Conditions: $R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF | | | 150 | ns |
| $t_{(LOOP2)}$ | Total loop delay, driver input (TXD) to receiver output (RXD), dominant to receissive(2) | See 图 10 Typical Conditions: $R_L$ = 60 Ω, $C_L$ = 100 pF, $C_{L(RXD)}$ = 15 pF | | | 150 | |
| $t_{MODE}$ | Mode change time from normal configuration to reverse | | | | 300 | µs |
| $t_{UV\_RE\text{-}ENABLE}$ | Re-enable time after UV event | See 图 10. Time for device to return to normal operation from $UV_{VCC}$ and $UV_{VIO}$ under voltage event | | | 300 | µs |

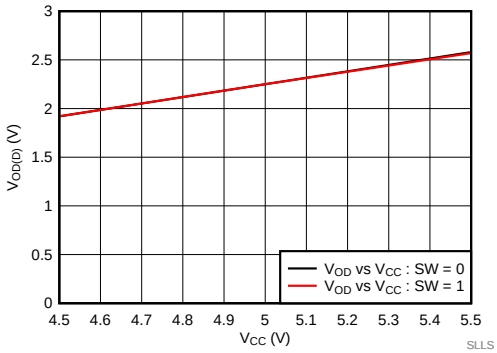
(2) Time span from signal edge on TXD input to next signal edge with same polarity on RXD output, the maximum of delay of both signal edges is to be considered.

## 6.9 Typical Characteristics



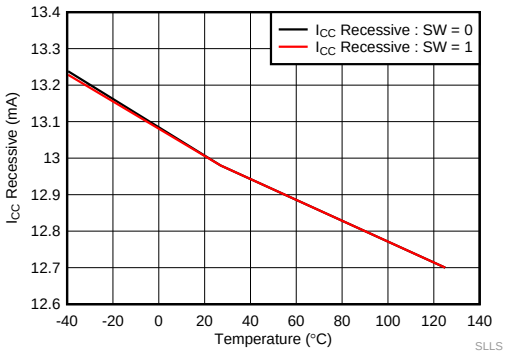

$V_{CC}$ = 5 V　$V_{IO}$ = 5 V　$R_L$= 60Ω
$C_L$ = Open　$R_{CM}$ = Open　SW = 0 / 1

**图 1. $V_{OD(D)}$ over Temperature**



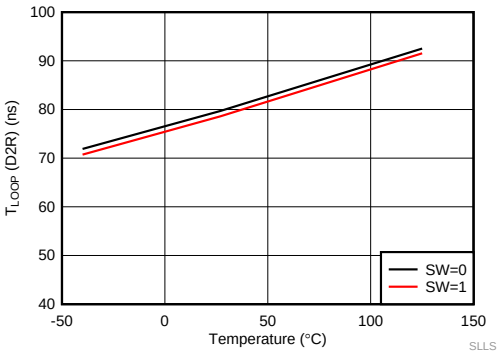

SW = 0 / 1　$V_{IO}$ = 5 V　$R_L$= 60Ω
$C_L$ = Open　$R_{CM}$ = Open　Temp = 25°C

**图 2. $V_{OD(D)}$ over $V_{CC}$ Supply Voltage**



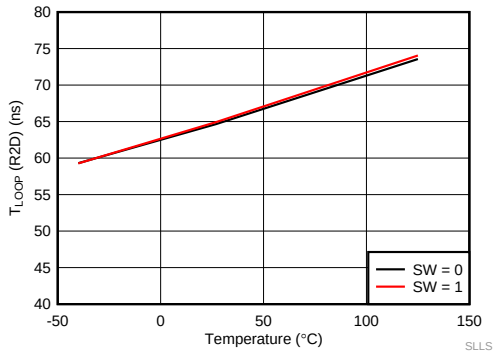

$V_{CC}$ = 5 V　$V_{IO}$ = 5 V　$R_L$= 60Ω
$C_L$ = Open　$R_{CM}$ = Open　SW = 0 / 1

**图 3. $I_{CC}$ over Temperature**




$V_{CC}$ = 5 V　$V_{IO}$ = 5 V　$R_L$= 60Ω
$C_L$ = Open　$R_{CM}$ = Open　SW = 0 / 1

**图 4. Dominant to Recessive $T_{LOOP}$ over Temperature**




$V_{CC}$ = 5 V　$V_{IO}$ = 5 V　$R_L$= 60 Ω
$C_L$ = Open　$R_{CM}$ = Open　SW = 0 / 1

**图 5. Recessive to Dominant $T_{LOOP}$ vs Temperature**

# 7 Parameter Measurement Information

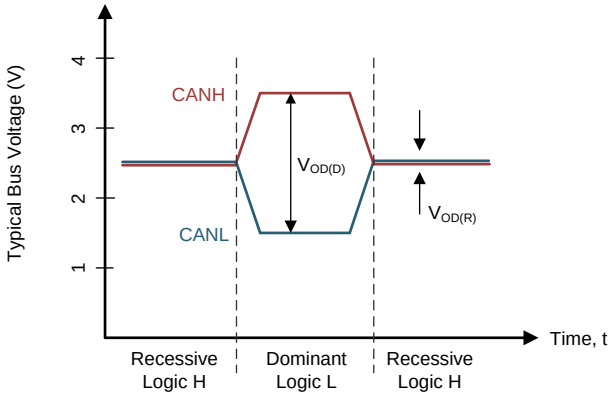



**图 6. Bus States (Physical Bit Representation)**

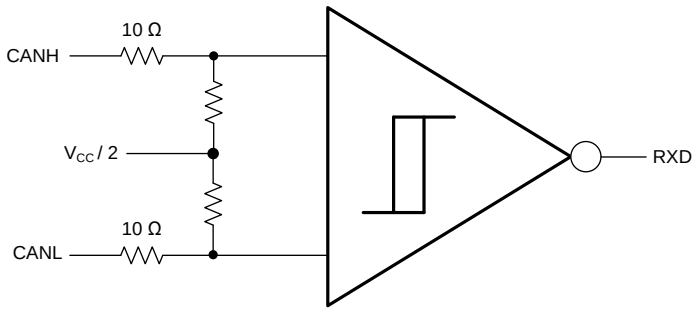



**图 7. Common Mode Bias Unit and Receiver**

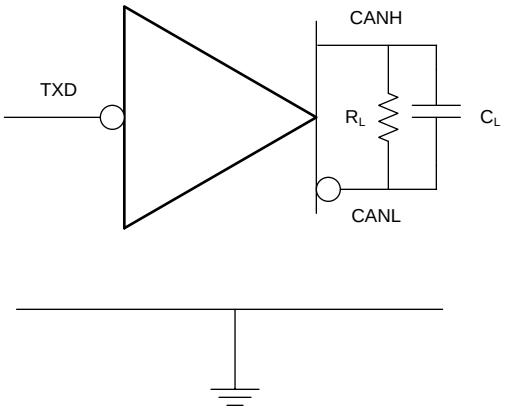



**图 8. Supply Test Circuit**

## Parameter Measurement Information (接下页)

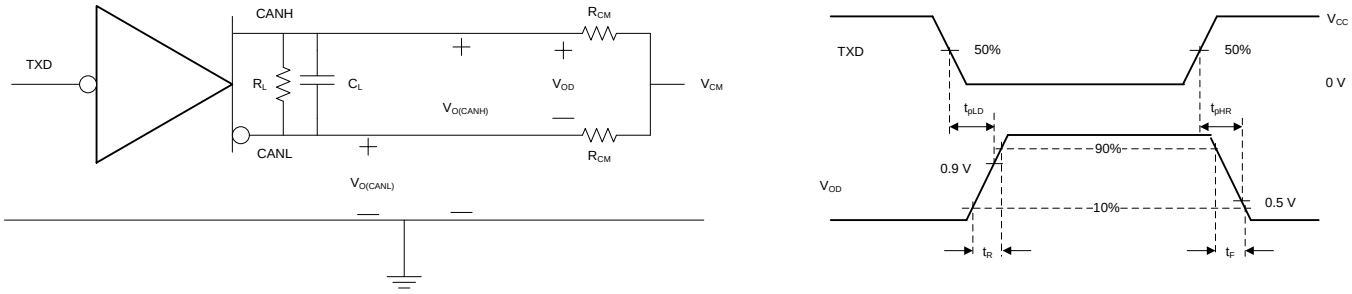



**图 9. Driver Test Circuit and Measurement**

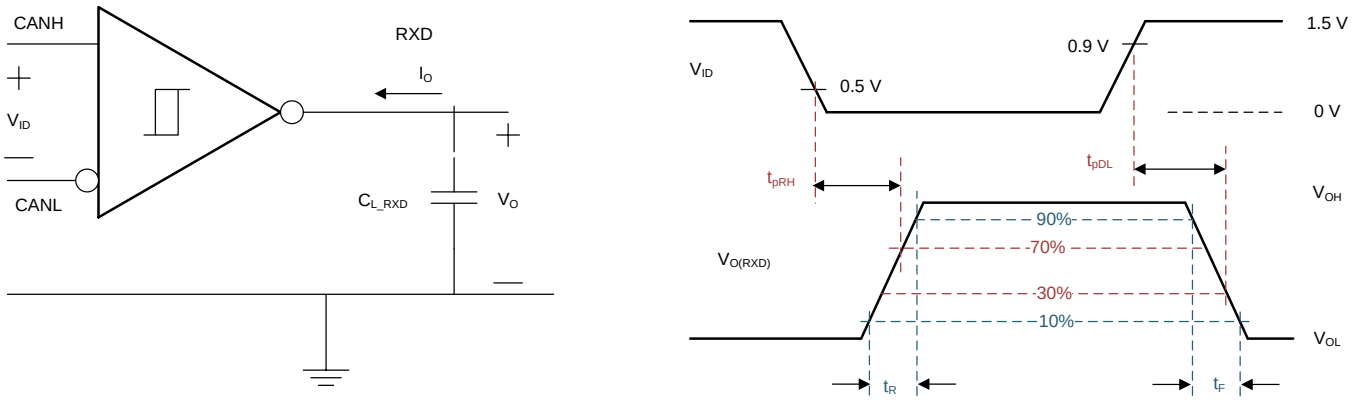



**图 10. Receiver Test Circuit and Measurement**

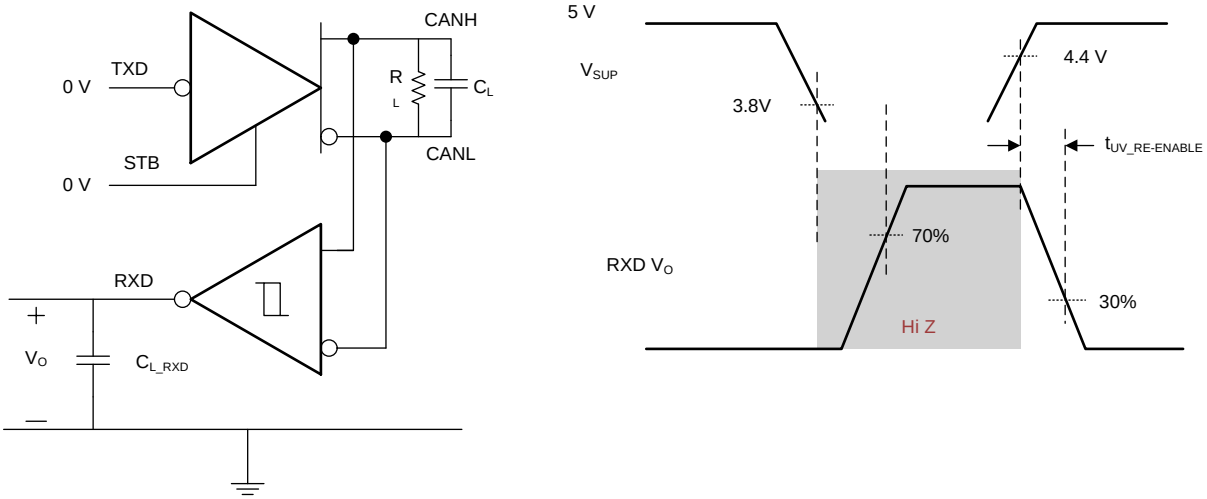



**图 11. UV Re-enable Time after UV Event**

## Parameter Measurement Information (接下页)

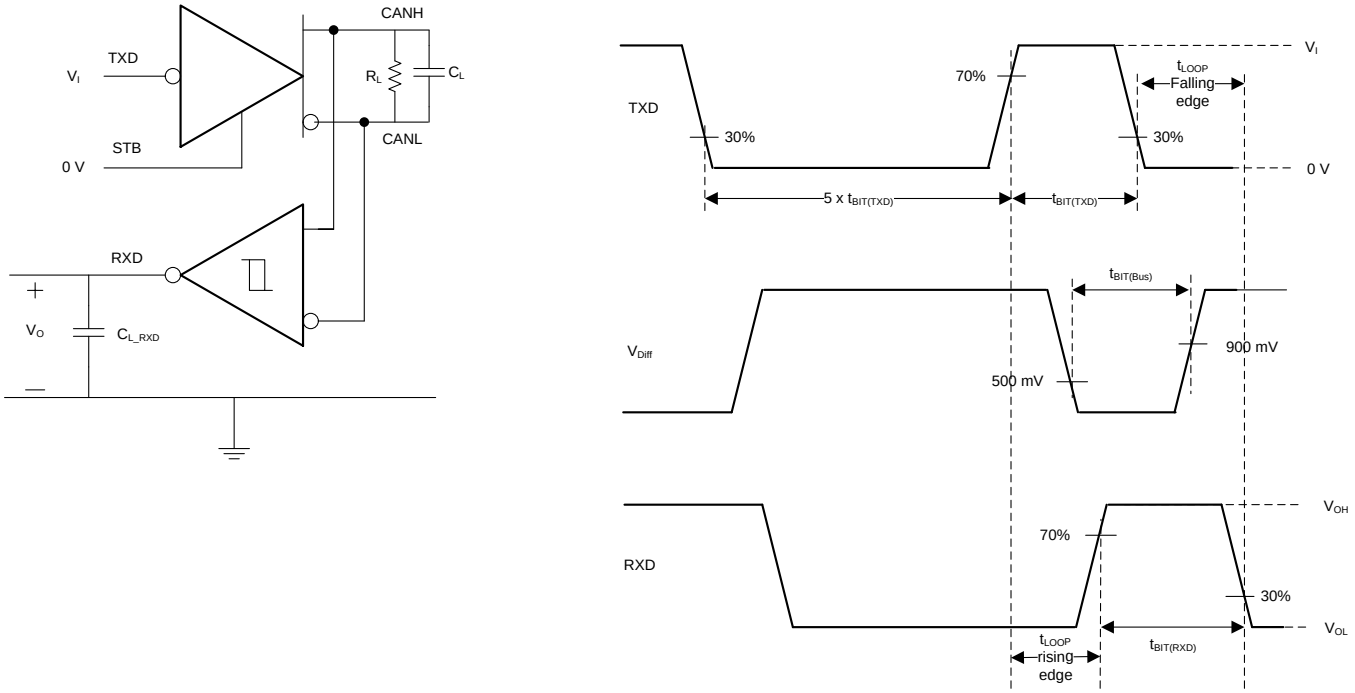



**图 12. Transmitter and Receiver Timing Behavior Test Circuit and Measurement**

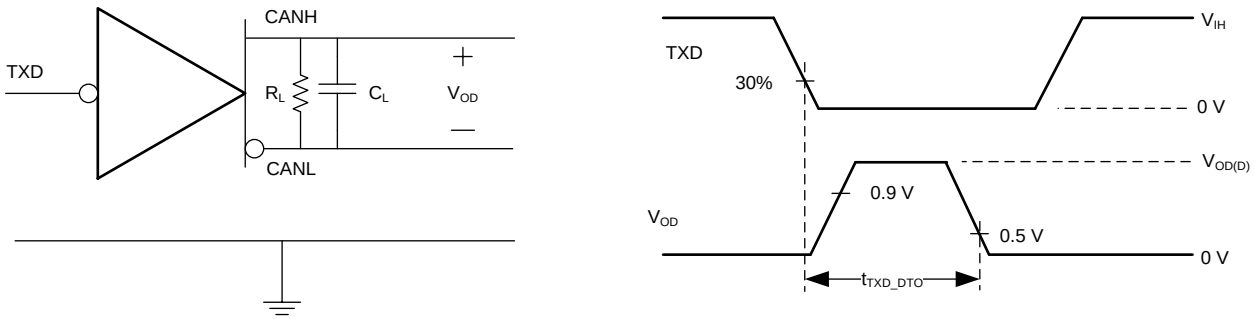



**图 13. TXD_INT Dominant Time Out Test Circuit and Measurement**

## Parameter Measurement Information (接下页)

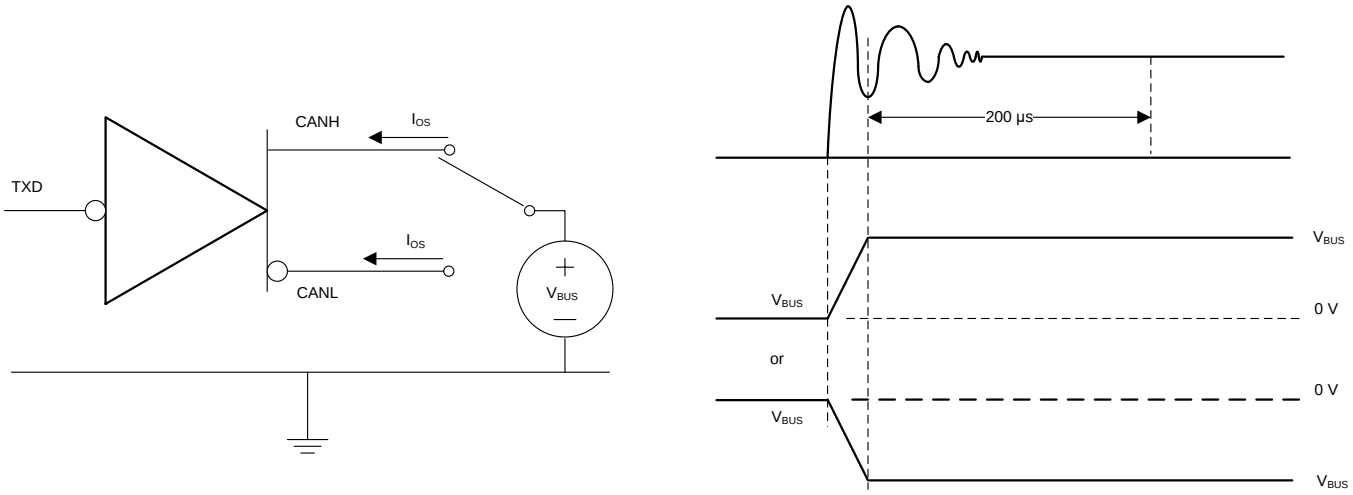



**图 14. Driver Short-Circuit Current Test and Measurement**

# 8 Detailed Description

## 8.1 Overview

The TCAN4420 is a high-speed CAN transceiver that meets the specifications of the ISO 11898-2 (2016) High Speed CAN (Controller Are Network) physical layer standards. It includes many protection features providing device and CAN network robustness. It also allows for the polarity of the CAN pins to be controlled externally by a micro-controller through the use of the polarity switch pin, SW.

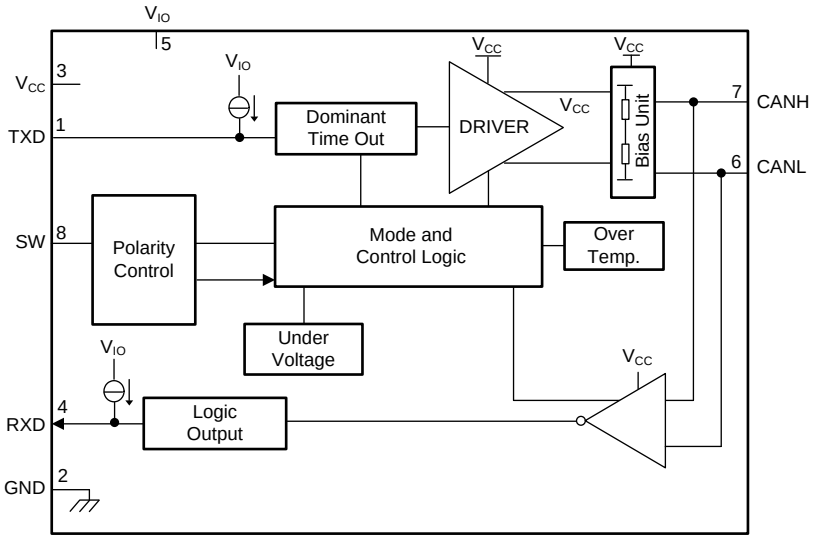
The CAN bus has two logical states during operation: recessive and dominant. See 图 6 and 图 7.

A recessive bus state occurs when the bus is biased to a common mode of $V_{CC}/2$ via the receivers bias unit. Recessive is equivalent to logic high on the TXD pin and is typically a differential voltage on the bus of approximately 0 V.

A dominant bus state occurs when the bus is driven differentially by one or more drivers. The driver produces a current which flows through the termination resistors on the bus and generates a differential voltage. Dominant is equivalent to logic low on the TXD pin and is a differential voltage on the bus greater than the minimum required threshold for a CAN dominant.

The host microprocessor of the CAN node uses the TXD terminal, pin 1, to drive the bus and receives data from the bus via the RXD terminal, pin 4. The TCAN4420 integrates level shifting capabilities into the RXD output via the $V_{IO}$ pin. This feature eliminates the need for an additional level shifter between the host microprocessor and the RXD output of the CAN transceiver.

## 8.2 Functional Block Diagrams






## 8.3 Feature Description

### 8.3.1 TXD Dominant Time Out (DTO)

The TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time out period $t_{TXD\_DTO}$. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on the TXD terminal, thus clearing the TXD DTO condition. The receiver and RXD terminal still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

## Feature Description (接下页)

### 8.3.2 CAN Bus Short Circuit Current Limiting

The TCAN4420 has several protection features that limit the short circuit current when a CAN bus line is shorted. These include CAN driver current limiting (dominant and recessive). During CAN communication the bus switches between dominant and recessive states, thus the short circuit current may be viewed either as the current during each bus state or as a DC average current. For system current and power considerations in the termination resistors and common mode choke ratings the average short circuit current should be used. The percentage dominant is limited by the TXD dominant time out and CAN protocol which has forced state changes and recessive bits such as bit stuffing, control fields, and inter frame space. These ensure there is a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated using 公式 1.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages,
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current.

**注**

The short circuit current and possible fault cases of the network should be taken into consideration when sizing the power ratings of the termination resistance, other network components, and the power supply used to generate $V_{CC}$.

### 8.3.3 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold of 170ºC the device turns off the CAN driver circuitry thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below the thermal shutdown temperature of the device. If the fault condition that caused the thermal shutdown is still present, the temperature may rise again and the device enters thermal shut down again. Prolonged operation with thermal shutdown conditions may affect device reliability. The thermal shutdown circuit includes hysteresis to avoid oscillation of the driver output.

**注**

During thermal shutdown the CAN bus driver is turned off thus no transmission is possible from TXD to the bus. The CAN bus terminals are biased to recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

### 8.3.4 Under Voltage Lockout (UVLO) and Unpowered Device

The $V_{CC}$ and $V_{IO}$ supply terminals have under voltage detection circuitry which places the device in a protected mode if an under voltage fault occurs. This protects the bus during an under voltage event on these terminals. If $V_{IO}$ is under voltage the RXD terminal is tri-stated (high impedance) and the device does not pass any signals from the bus. If $V_{CC}$ supply is lost, or has a brown out that triggers the UVLO, the device transitions to a protected mode. See 表 1.

If $V_{IO}$ drops below $UV_{VIO}$ under voltage detection, the transceiver switches off and disengage from the bus until $V_{IO}$ has recovered.

## Feature Description (接下页)

The device is designed to be an "ideal passive" or “no load” to the CAN bus if the device is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational. Logic terminals also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

**表 1. Under Voltage Lockout Protection**

| $V_{CC}$ | $V_{IO}$ | DEVICE STATE | BUS | RXD |
|---|---|---|---|---|
| > $UV_{VCC}$ | > $UV_{VIO}$ | Normal | Per TXD | Mirrors Bus |
| < $UV_{VCC}$ | > $UV_{VIO}$ | Protected | High Impedance | High (Recessive) |
| > $UV_{VCC}$ | < $UV_{VIO}$ | Protected | High Impedance | High Impedance |
| < $UV_{VCC}$ | < $UV_{VIO}$ | Protected | High Impedance | High Impedance |

**注**

Once an under voltage condition is cleared and the $V_{CC}$ supply has returned to valid level the device typically needs $t_{MODE}$ to transition to normal operation. The host processor should not attempt to send or receive messages until this transition time has expired.

#### *8.3.4.1 $V_{IO}$ Supply PIN*

A separate $V_{IO}$ supply pin is supported on this device. This pin should be connected to the supply voltage of the microcontroller, see 图 17 and 图 18. This sets the signal levels for TXD, RXD and SW pins to the I/O level of the microcontroller.

## 8.4 Device Functional Modes

### 8.4.1 Polarity Configuration

The device supports two polarity configurations on the CAN pins. For a conventional (normal) CAN connection, connect SW pin to GND. Allow for a time interval equal to $t_{MODE}$ after changing the SW pin, before reading the bus or the RXD pin. To support a reverse connection of the CAN pins, connect the SW pin to $V_{IO}$. This approach enables compatibility with existing boards that already use this pin (pin 8) to be connected to GND for normal operation. See 表 2.

**表 2. Polarity Configurations**

| SW Pin | Device Polarity | $V_{OD}$(TX) or $V_{ID}$ (RX) |
|---|---|---|
| LOW | Normal | = CANH-CANL |
| HIGH | Reverse | = CANL-CANH |

### 8.4.2 Normal Polarity Mode

This is the normal configuration of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. Normal Mode is enabled when there is a logic low on the SW pin.

### 8.4.3 Reverse Polarity Mode

The TCAN4420 supports a reverse polarity configuration when the SW pin is connected to supply. In this configuration, both the driver and receiver remain fully operational, the key difference being that both $V_{OD}$ and $V_{ID}$ are now defined as the difference between CANL and CANH pins as indicated in 表 2. Also see Table 表 3 and 表 4 for the pin voltage levels in this configuration.

### 8.4.4 Driver and Receiver Function

The digital logic input and output levels for these devices are TTL levels with respect to $V_{IO}$ for compatibility with protocol controllers having 2.8 V to 5 V logic or I/O.

表 3 and 表 4 provide the states of the CAN driver and CAN receiver in each mode.

**表 3. Driver Function Table**

| DEVICE MODE | TXD INPUT(1) | BUS OUTPUTS(2) | | DRIVEN BUS STATE(3) |
|---|---|---|---|---|
| | | CANH | CANL | |
| Normal | L | H | L | Dominant |
| | H or Open | Z | Z | Biased Recessive |
| Reverse | L | L | H | Dominant |
| | H or Open | Z | Z | Biased Recessive |

(1) H = high level, L = low level
(2) H = high level, L = low level, Z = high Z receiver bias
(3) For Bus state and bias see 图 7

**表 4. Receiver Function Table**

| DEVICE MODE | CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$ | BUS STATE | RXD TERMINAL(1) |
|---|---|---|---|
| Normal: $V_{ID} = V_{CANH} - V_{CANL}$<br>Reverse: $V_{ID} = V_{CANL} - V_{CANH}$ | $V_{ID} \geq 0.9$ V | Dominant | L |
| | 0.5 V < $V_{ID}$ < 0.9 V | Undefined | Undefined |
| | $V_{ID} \leq 0.5$ V | Recessive | H |

(1) H = high level, L = low level

### 8.4.5 Floating Terminals

The TCAN4420 has internal pull ups and pull downs on critical terminals to place the device into known states if the terminal floats. See 表 5 for details on terminal bias conditions

**表 5. Terminal Bias**

| TERMINAL | PULL UP or PULL DOWN | COMMENT |
|---|---|---|
| TXD | Pull up | Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering |
| SW | Pull down | Weakly biases SW terminal towards GND to use the default (normal) polarity configuration |

**注**

The internal bias should not be relied upon as only termination, especially in noisy environments but should be considered a failsafe protection. Special care needs to be taken when the device is used with MCUs which implement open drain outputs. TXD is weakly internally pulled up. The TXD pull up strength and CAN bit timing require special consideration when this device is used with an open drain TXD output on the microprocessor CAN controller. An adequate external pull up resistor must be used to ensure that the TXD output of the microprocessor maintains adequate bit timing input to the CAN transceiver.

# 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the data link layer portion of the CAN protocol. Below are typical application configurations for both 5 V and 3.3 V microprocessor applications. The bus termination is shown for illustrative purposes.

## 9.2 Typical Application

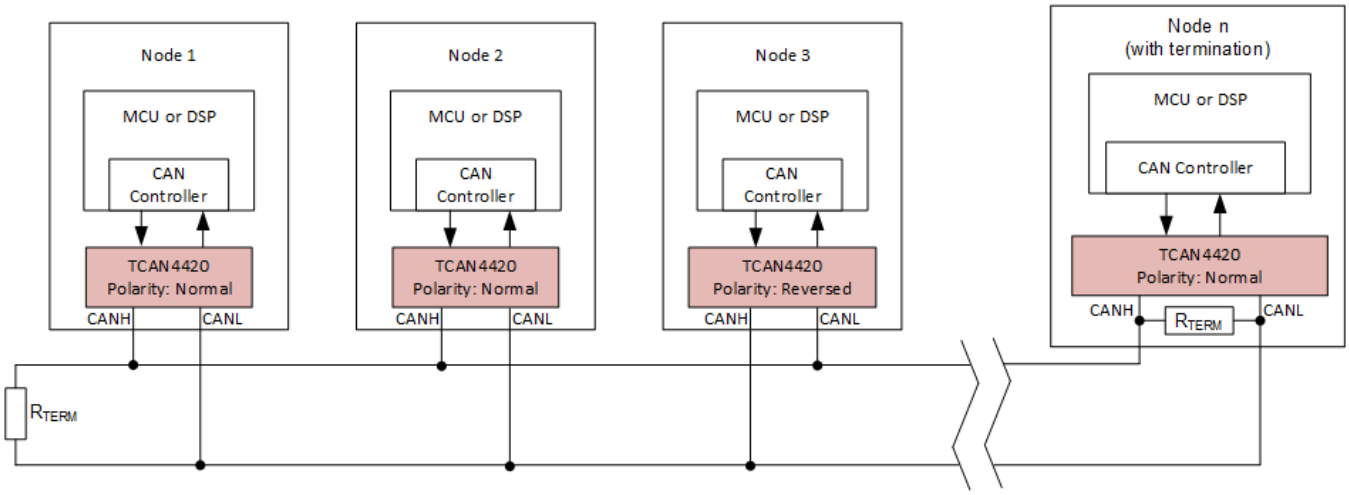



**图 15. Typical CAN Bus Application**

### 9.2.1 Design Requirements

#### *9.2.1.1 Bus Loading, Length and Number of Nodes*

A typical CAN application can have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes require a transceiver with high input impedance such as the TCAN4420 transceiver.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In ISO 11898-2 the driver differential output is specified with a 60-Ω bus load where the differential output must be greater than 1.5 V. The TCAN4420 is specified to meet the 1.5 V requirement across this load and is specified to meet 1.3-V differential output at 50-Ω bus load. The differential input resistance of this family of transceiver is a minimum of 20 kΩ. If 67 of these transceivers are in parallel on a bus, this is equivalent to an 300-Ω differential load in parallel with the 60 Ω bus termination which gives a total bus load of 50 Ω. Therefore, this family theoretically supports over 67 transceivers on a single bus segment with margin to the 0.9-V minimum differential input voltage requirement at each receiving node. However, for network design, margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is much lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes on the bus, and significantly lowered data rate.

## Typical Application (接下页)

This flexibility in network design is one of its key strengths allowing for these system level network extensions and additional standards to build on the typical CAN bus length parameters. However, when using this flexibility the network system designer must take the responsibility of good network design to ensure robust network operation.

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 CAN Termination*

The ISO 11898 standard specifies the interconnect to be a twisted-pair cable (shielded or unshielded) with 120-Ω characteristic impedance ($Z_O$). Resistors equal to the characteristic impedance of the line must be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines, stubs, connecting nodes to the bus must be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus

Termination may be a single 120-Ω resistor at the end of the bus either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used, see 图 16. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages.

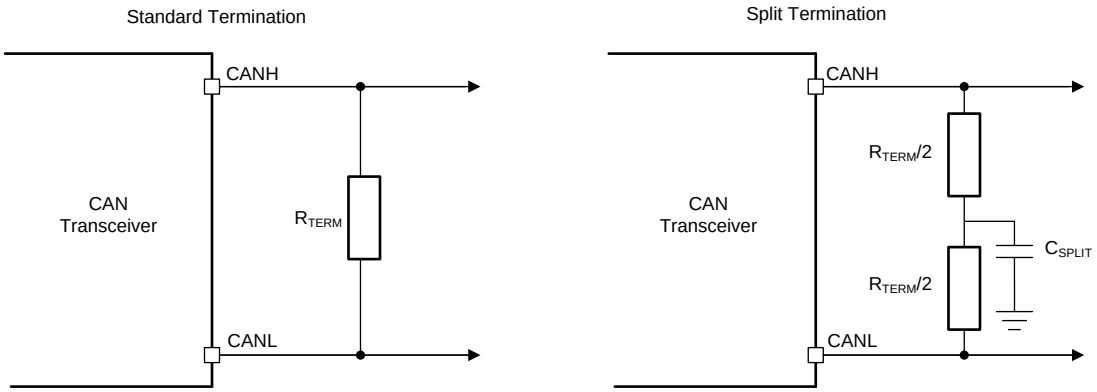



**图 16. CAN Bus Termination Concepts**

The TCAN4420 transceiver supports both 5-V only applications and applications where level shifting is needed for a 3.3-V microcontroller. See 图 17 and 图 18 for application examples.

## Typical Application（接下页）

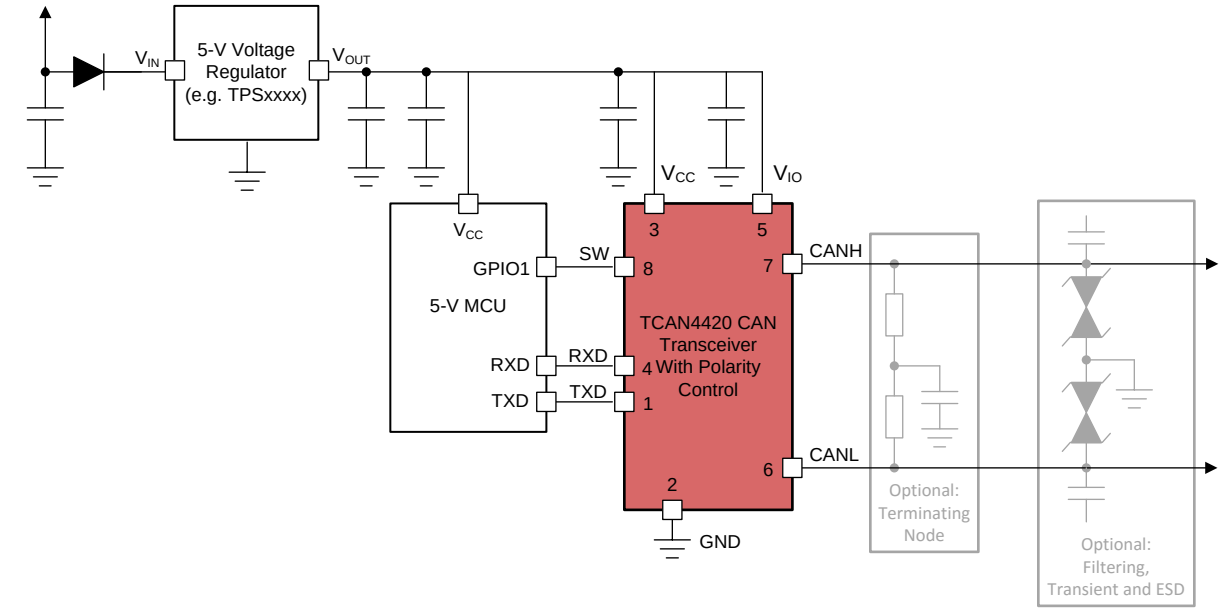





**图 17. Typical CAN Bus Application Using TCAN4420 with 5 V µC**

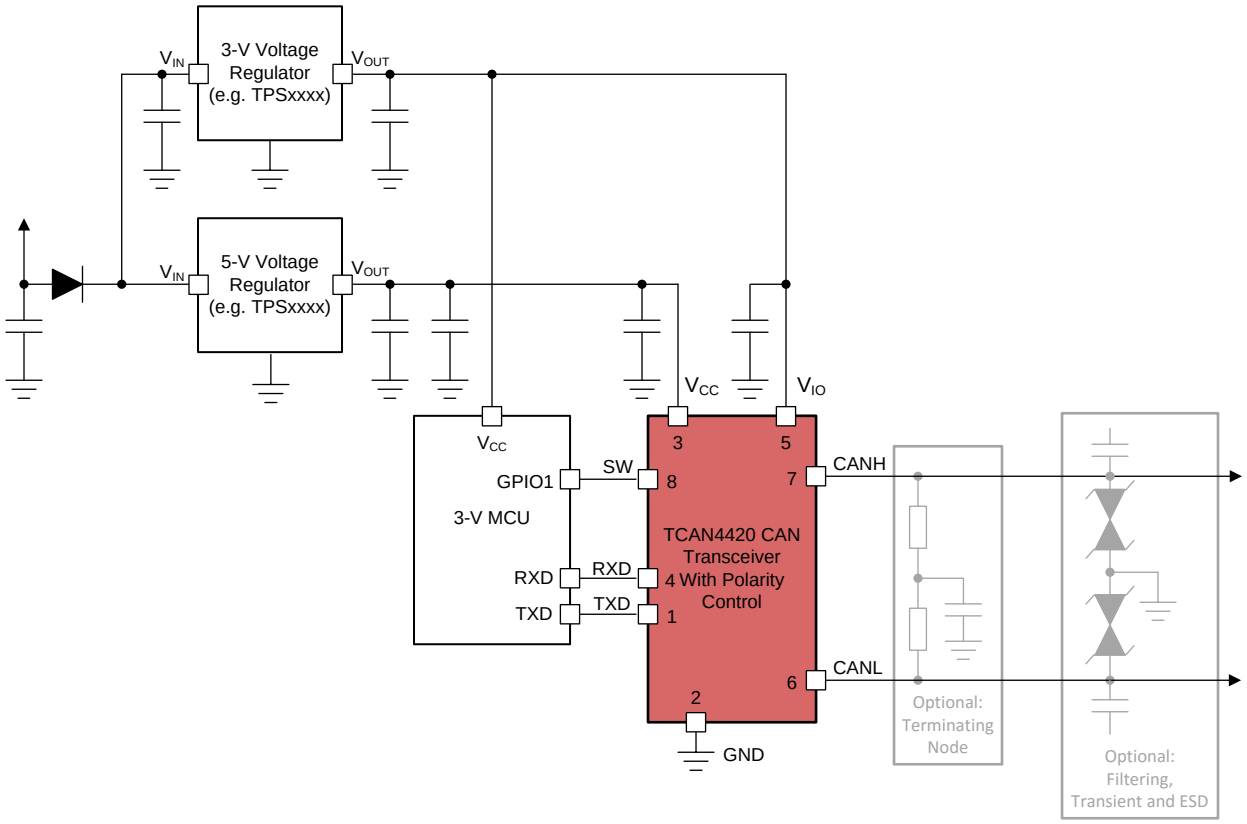





**图 18. Typical CAN Application Using TCAN4420 with 3.3 V µC**

## Typical Application (接下页)

### 9.2.3 Application Curves

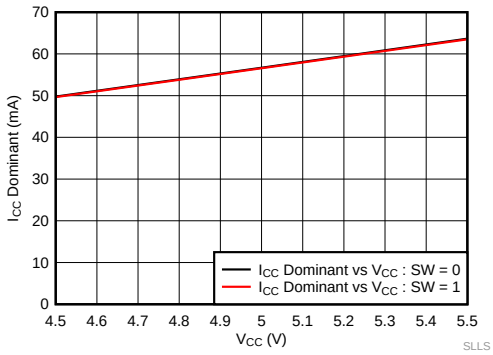



**图 19. $I_{CC}$ Dominant Current over $V_{CC}$ Supply Voltage**

## 10 Power Supply Recommendations

The TCAN4420 device is designed to operate with a main $V_{CC}$ input voltage supply range between 4.5 V and 5.5 V. The device also has an IO level shifting supply input, $V_{IO}$, designed for a range between 2.8 V and 5.5 V. To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

# 11 Layout

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

## 11.1 Layout Guidelines

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from propagating onto the board. In this layout example a transient voltage suppression (TVS) device, D1, has been used for added protection. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C3 and C4. Additionally (not shown) a series common mode choke (CMC) can be placed on the CANH and CANL lines between the TCAN4420 transceiver and connector J1.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply ($V_{CC}$) and ground planes to provide low inductance.

**注**

High-frequency currents follows the path of least impedance and not the path of least resistance.

- Use at least two vias for supply ($V_{CC}$) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass capacitors should be placed as close as possible to the supply terminals of transceiver, examples are C1 on the $V_{CC}$ supply and C5 on the $V_{IO}$ supply.
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R6 and R7, with the center or split tap of the termination connected to ground via capacitor C2. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines, serial resistors may be used. Examples are R2, R3, and R4. These are not required.
- Pin 1: R1 is shown optionally for the TXD input of the device. If an open drain host processor is used, this is mandatory to ensure the bit timing into the device is met.
- Pin 5: A bypass capacitor should be placed as close to the pin as possible (example C5). A voltage must be applied to the $V_{IO}$ for normal operation.
- Pin 8: is shows the SW terminal with R4 and R5 as optional resistors. The SW terminal can also be tied to an IO for soft polarity configuration.

## 11.2 Layout Example

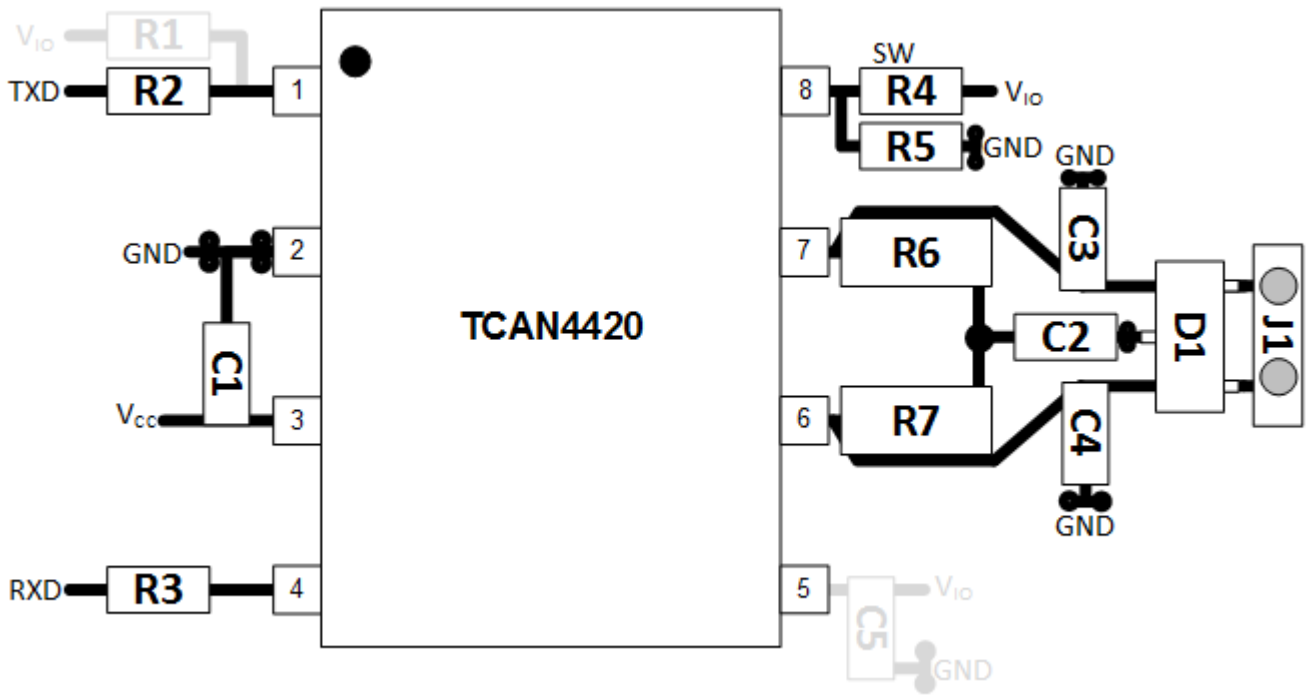



图 20. Example Layout

# 12 器件和文档支持

## 12.1 器件支持

该器件将遵循以下 CAN 标准。本系统规格涵盖了所需的核心内容；但是，应为这些标准提供参考，并指出和探讨所有分歧之处。本文档应提供所需的全部基本内容。但是，由于详细的 CAN 协议范围不在此物理层（收发器）规格范围之内，这些额外的资源对全面了解 CAN（包括协议）非常有帮助。

### 12.1.1 器件命名规则

CAN 收发器物理层标准：

- ISO11898-2 高速媒介访问单元（原高速 CAN 收发器标准）
- 具有低功耗模式的 ISO11898-5 高速媒介访问单元（取代了 ISO11898-2 标准规范中的若干电气规格，并增加了在低功耗模式下通过总线实现原始唤醒功能）。

一致性测试要求：

- A Comprehensible Guide to Controller Area Network", Wilfried Voss, Copperhill Media Corporation
- "CAN System Engineering: From Theory to Practical Applications", 2nd Edition, 2013; Dr. Wolfhard Lawrenz, Springer.

## 12.2 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 12.3 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

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**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

## 12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 机械、封装和可订购信息

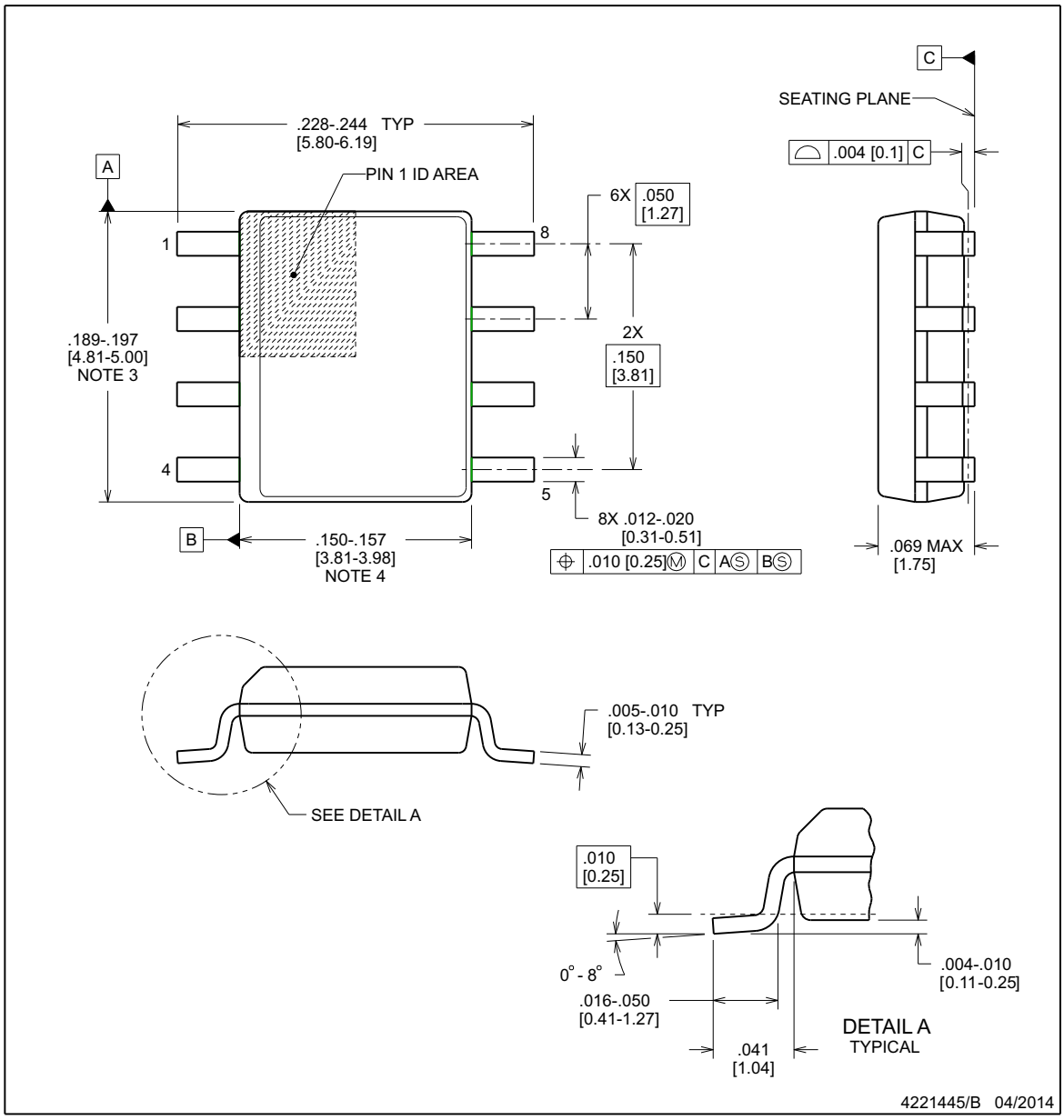
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

# PACKAGE OUTLINE

## D0008B

## SOIC - 1.75 mm max height

SOIC




NOTES:

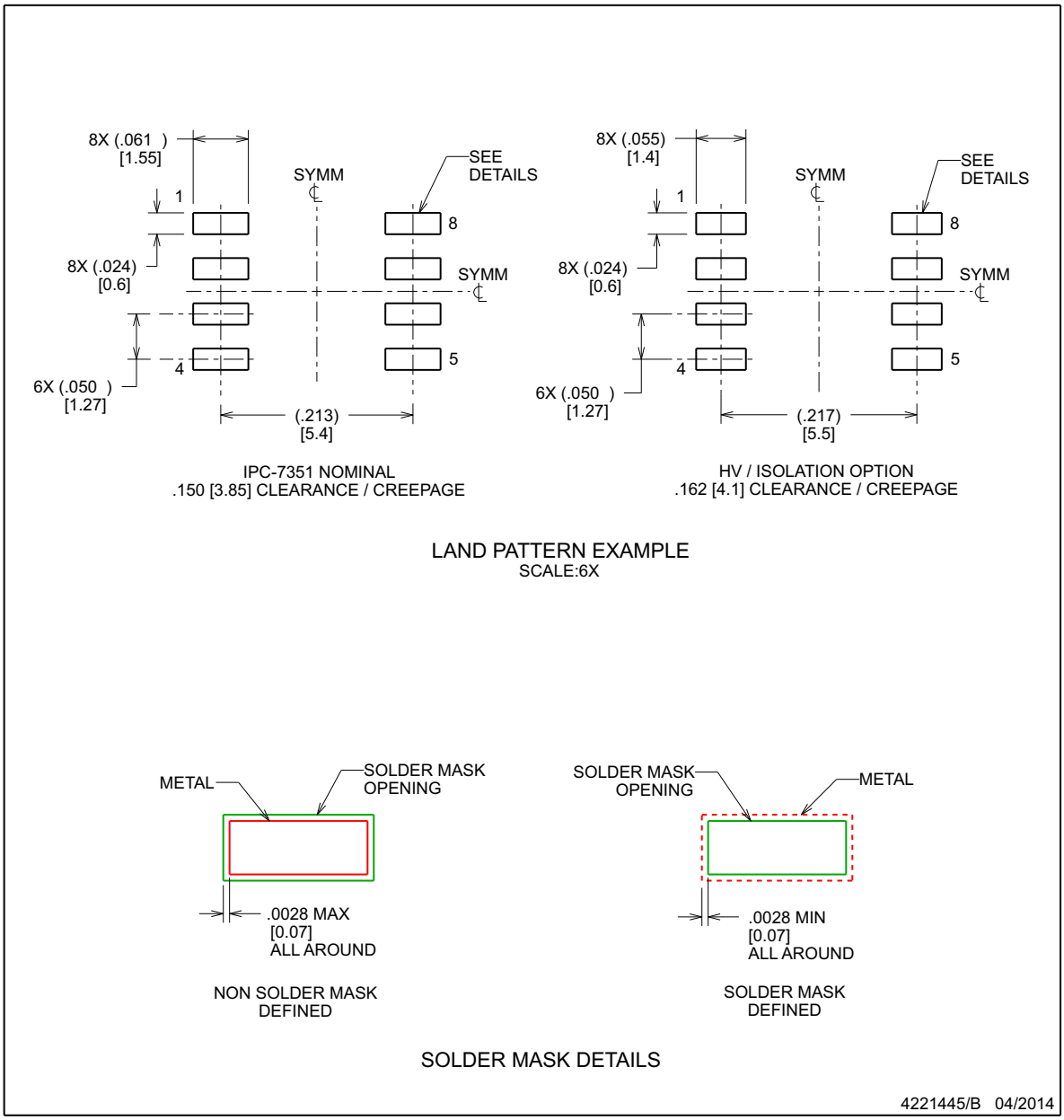
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

## D0008B

### SOIC - 1.75 mm max height

SOIC



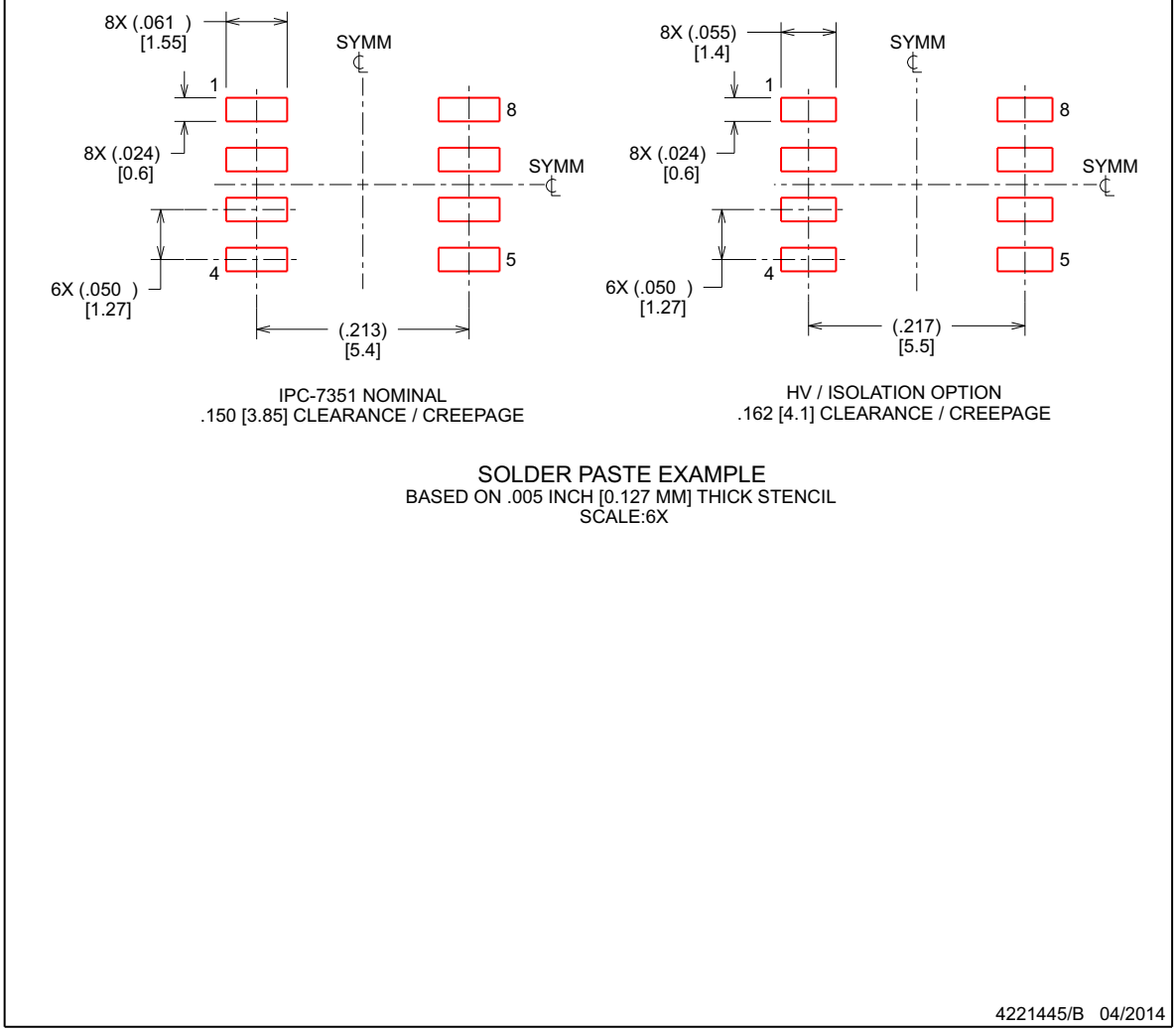

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**D0008B** — **SOIC - 1.75 mm max height**

SOIC




NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TCAN4420DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4420 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

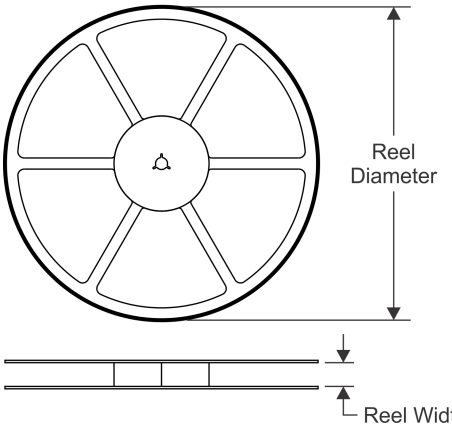
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

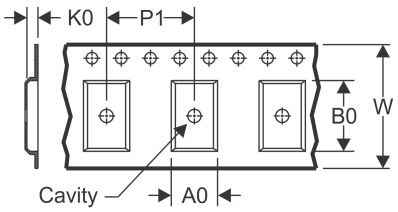
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

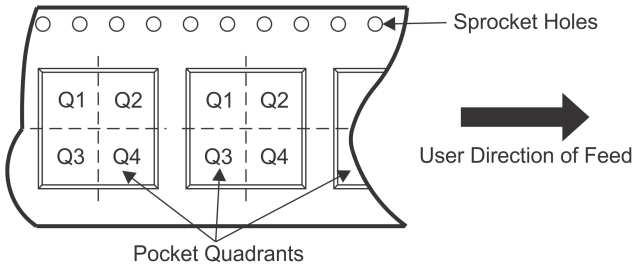



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

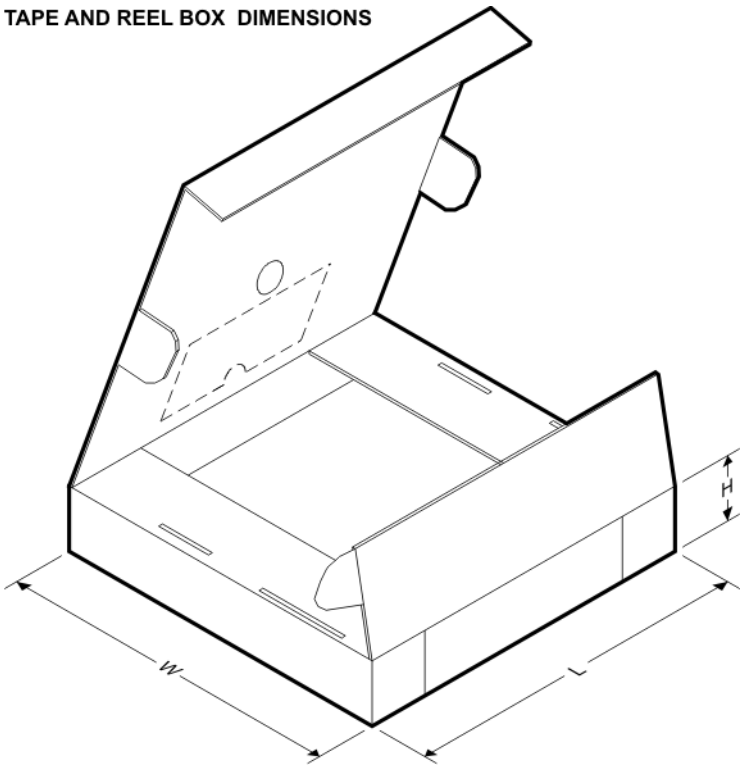
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TCAN4420DR | SOIC | D | 8 | 2500 | 330.0 | 15.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TCAN4420DR | SOIC | D | 8 | 2500 | 336.6 | 336.6 | 41.3 |

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