TLV742P 200mA 小尺寸低压降线性稳压器

1 特性

- 输入电压范围：2V 至 5.5V
- 可提供 0.85V 至 5V 范围（以 50mV 为增量）内的固定输出电压组合(1)
- 典型精度为 0.5%
- 高 PSRR：
  - 1MHz 时为 55dB
- 启用时的 I_Q：25μA
- 禁用时的 I_Q：1μA
- 有源输出放电
- 热关断保护和过流保护
- 封装：
  - 1mm × 1mm DQN (X2SON)

2 应用

- 销售终端
- 摄像头和机器视觉模块
- 游戏和玩具
- 楼宇自动化和视频监控
- 电视和机顶盒

3 说明

TLV742P 系列低压降线性稳压器 (LDO) 经过优化，能够通过支持宽输出电压范围提供出色的性能。这些 LDO 可将单节锂离子电池的输入至输出电压直接调节为低至 0.85V。如果此器件用于对直流/直流转换器输出进行后期调节，则其在 1MHz 下的 55dB 高 PSRR 可抑制纹波，从而提供低噪声且良好调节的稳定 V_{OUT}。

TLV742P 具备有源输出放电特性，有助于在系统处于禁用状态、待机模式或睡眠模式时确保输出保持低电平。此外，该器件的过流保护功能可在输出短路的情况下保护器件，并且其热关断功能可防止过热。

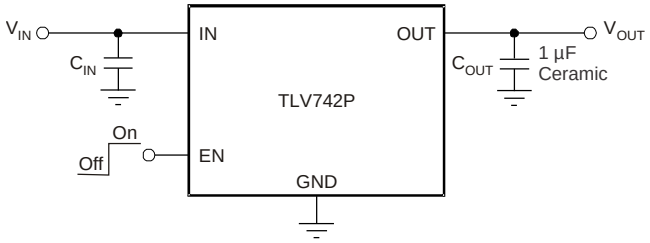
TLV742P 系列稳压器采用 1mm × 1mm X2SON 封装，因此可最大限度减少 PCB 面积。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV742P	X2SON (4)	1.00mm x 1.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用电路



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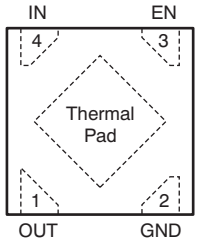
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2017 年 9 月	*	初始发行版。

5 Pin Configuration and Functions

DQN Package
4-Pin X2SON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. For TLV742P, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
GND	2	—	Ground pin
IN	4	I	Input pin. For good transient performance, place a small 1-μF ceramic capacitor from this pin to ground. See *Input and Output Capacitor Requirements* for more details.
OUT	1	O	Regulated output voltage pin. A small 1-μF ceramic capacitor is required from this pin to ground to ensure stability. See *Input and Output Capacitor Requirements* for more details.
Thermal pad	—	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6	V
	EN	–0.3	6	V
	OUT	–0.3	6	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Operating junction, T_J		–55	150	°C
Storage, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to GND pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)(1)	±2000	V
		Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature range	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV742P DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	152	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	117.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	117	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	99.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

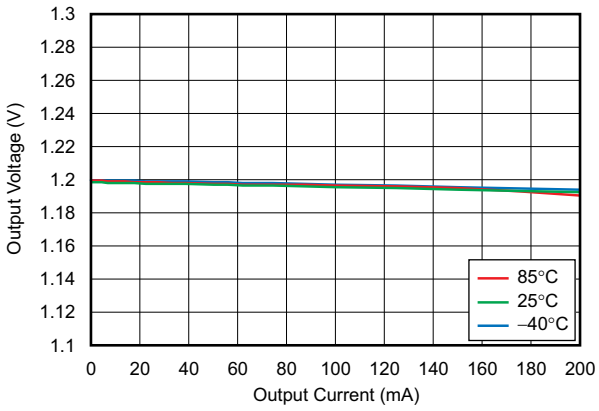
at V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 0.47 µF, and T_J = –40°C to +85°C. Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2		5.5	V
V_{OUT}	Output voltage range				0.85		5	V
	DC output accuracy					0.5%		
		V_{OUT} ≥ 0.85 V			–1.5%		1.5%	
$\Delta V_{O(\Delta VI)}$	Line regulation					1	5	mV
$\Delta V_{O(\Delta IO)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA				10	20	mV
$V_{(DO)}$	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$	2 V < V_{OUT} ≤ 2.4 V	I_{OUT} = 30 mA		65		mV
				I_{OUT} = 150 mA		325	360	mV
			2.4 V < V_{OUT} ≤ 2.8 V	I_{OUT} = 30 mA		50		mV
				I_{OUT} = 150 mA		250	300	mV
			2.8 V < V_{OUT} ≤ 3.3 V	I_{OUT} = 30 mA		45		mV
				I_{OUT} = 150 mA		220	270	mV
			3.3 V < V_{OUT} ≤ 5 V	I_{OUT} = 30 mA		40		mV
				I_{OUT} = 150 mA		200	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$			240	300	450	mA
$I_{(GND)}$	Ground pin current	I_{OUT} = 0 mA				25	50	µA
$I_{(EN)}$	EN pin current	V_{EN} = 5.5 V				0.01		µA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V 2 V ≤ V_{IN} ≤ 4.5 V				1		µA
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)				0		0.4	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)				0.9		V_{IN}	V
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V V_{OUT} = 2.8 V I_{OUT} = 30 mA		f = 100 Hz		70		dB
				f = 10 kHz		55		
				f = 1 MHz		55		
V_n	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V V_{OUT} = 1.8 V I_{OUT} = 10 mA				45		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1 µF I_{OUT} = 150 mA				100		µs
$R_{PULLDOWN}$	Pulldown resistance (TLV742P only)					120		Ω
T_J	Operating junction temperature				–40		125	°C

(1) Start-up time = time from EN assertion to 0.98 × V_{OUT}.

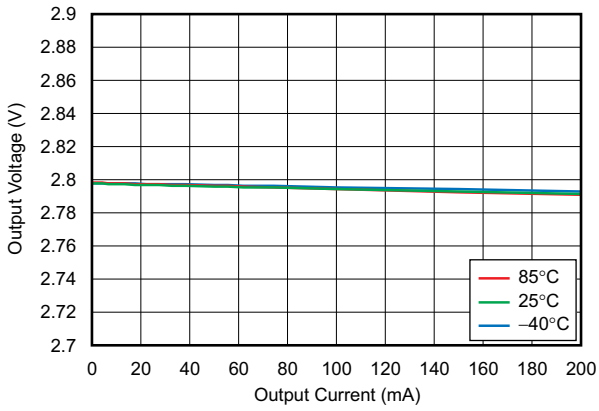
6.6 Typical Characteristics

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



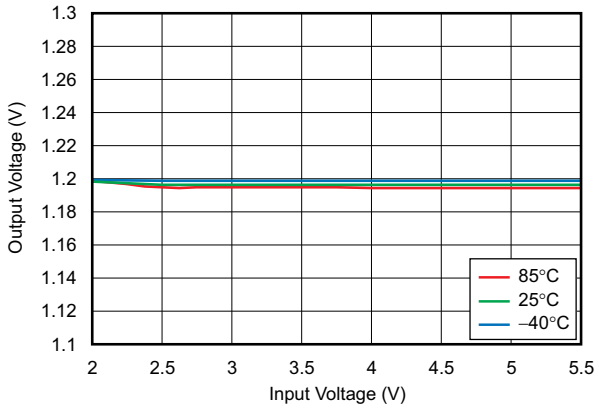
V_{OUT} = 1.2 V

图 1. Load Regulation



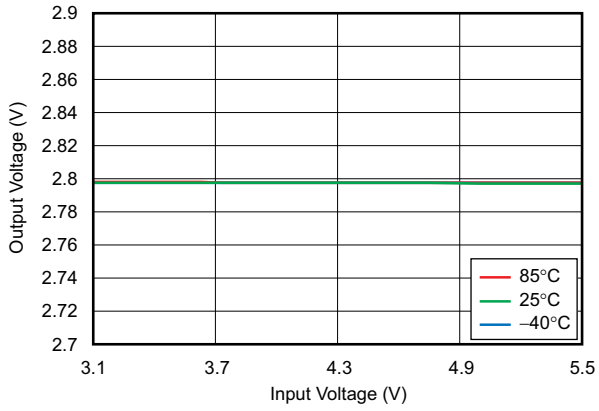
V_{OUT} = 2.8 V

图 2. Load Regulation



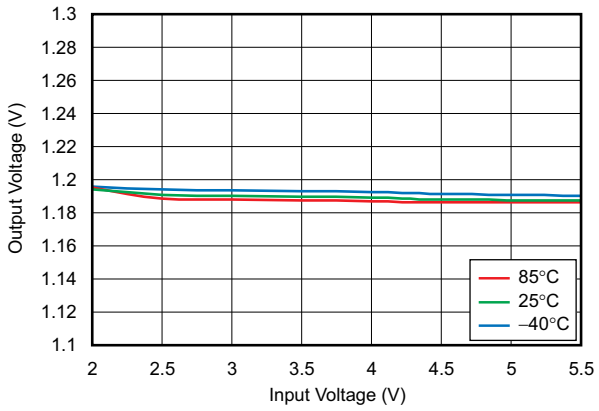
V_{OUT} = 1.2 V, I_{OUT} = 10 mA

图 3. Line Regulation



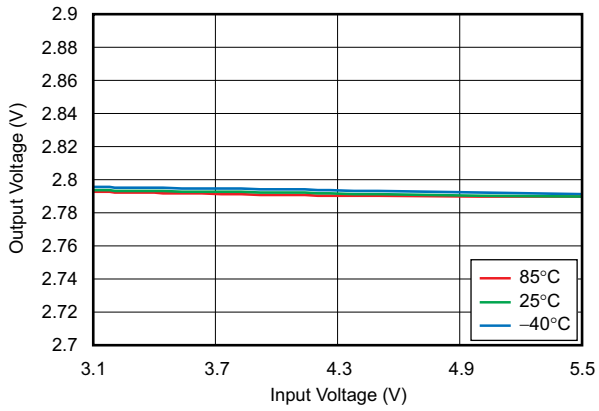
V_{OUT} = 2.8 V, I_{OUT} = 10 mA

图 4. Line Regulation



V_{OUT} = 1.2 V, I_{OUT} = 150 mA

图 5. Line Regulation

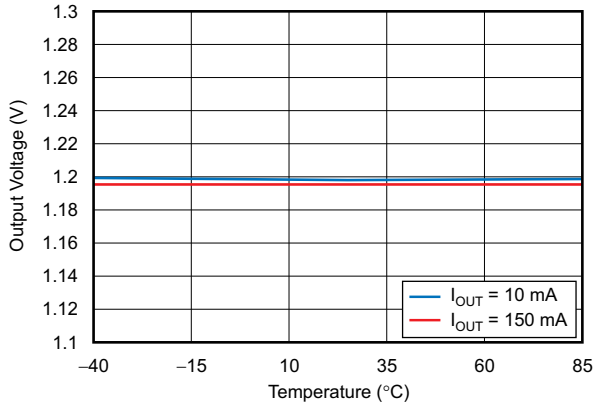


V_{OUT} = 2.8 V, I_{OUT} = 150 mA

图 6. Line Regulation

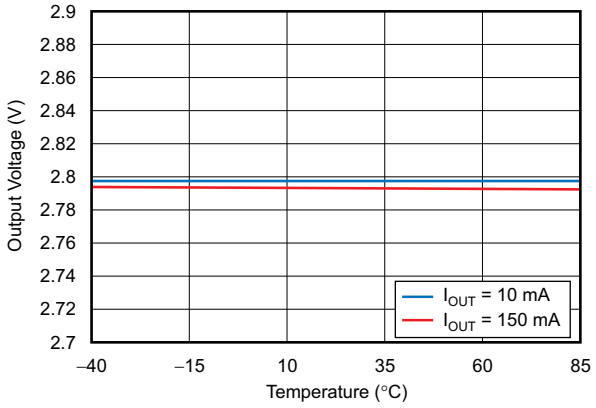
Typical Characteristics (接下页)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



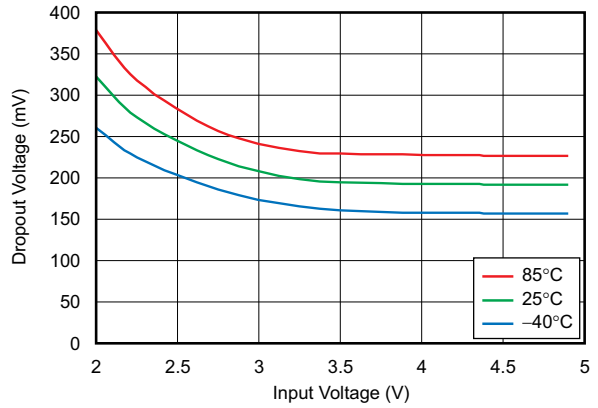
V_{OUT} = 1.2 V

图 7. Output Voltage vs Temperature



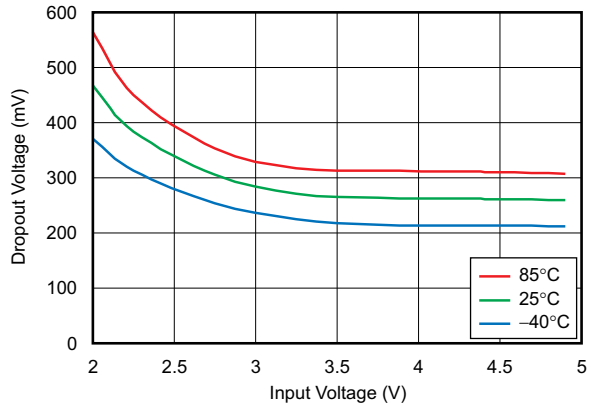
V_{OUT} = 2.8 V

图 8. Output Voltage vs Temperature



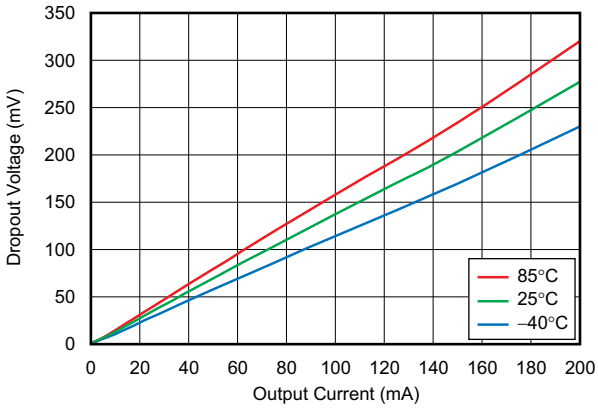
I_{OUT} = 150 mA

图 9. Dropout Voltage vs Input Voltage



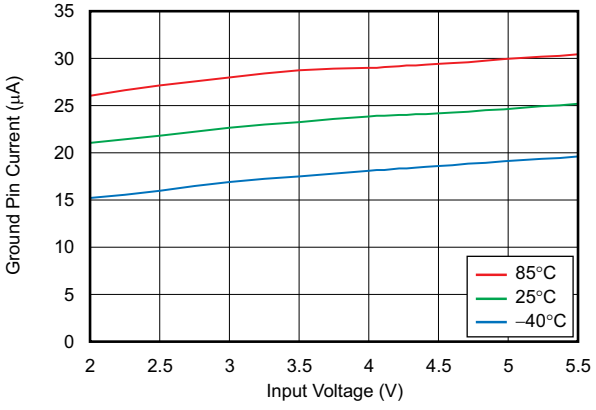
I_{OUT} = 200 mA

图 10. Dropout Voltage vs Input Voltage



V_{OUT} = 2.8 V

图 11. Dropout Voltage vs Output Current

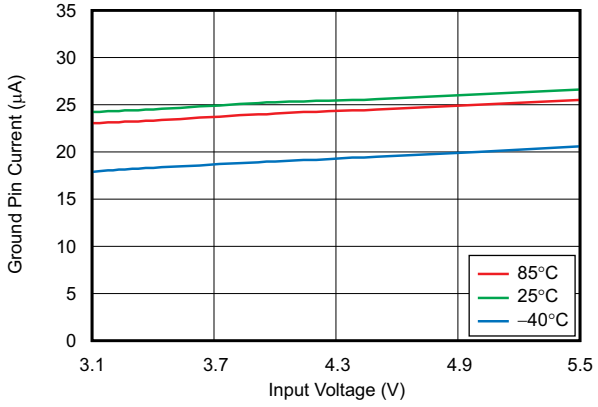


V_{OUT} = 1.2 V, I_{OUT} = 0 mA

图 12. Ground Pin Current vs Input Voltage

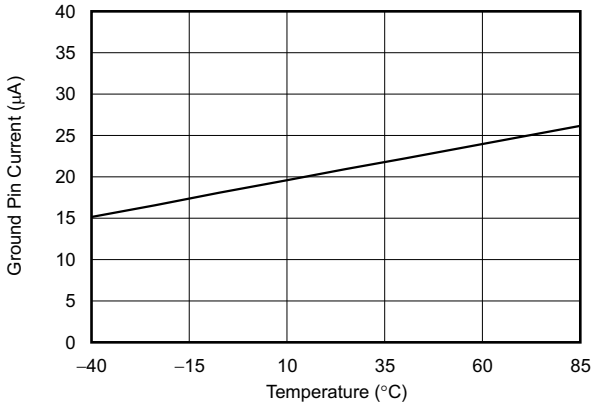
Typical Characteristics (接下页)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



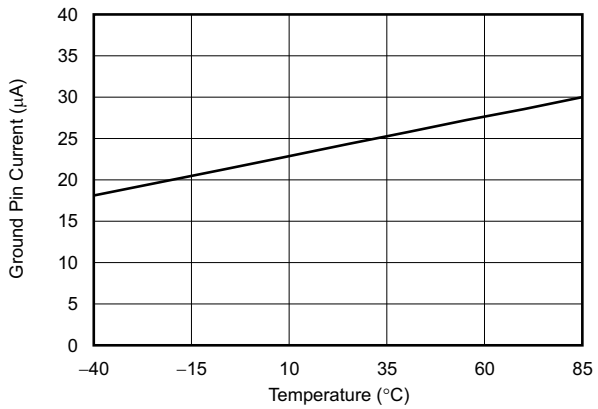
V_{OUT} = 2.8 V, I_{OUT} = 0 mA

图 13. Ground Pin Current vs Input Voltage



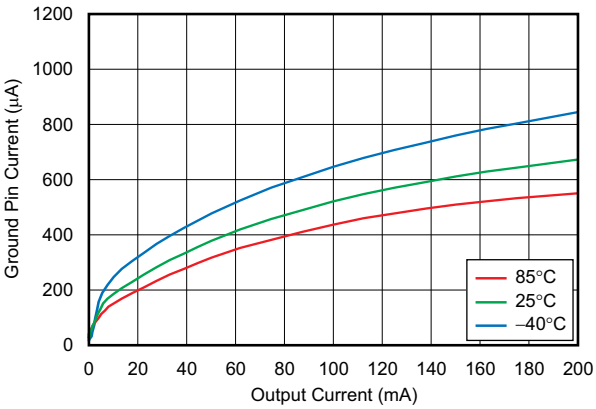
V_{OUT} = 1.2 V, I_{OUT} = 0 mA

图 14. Ground Pin Current vs Temperature



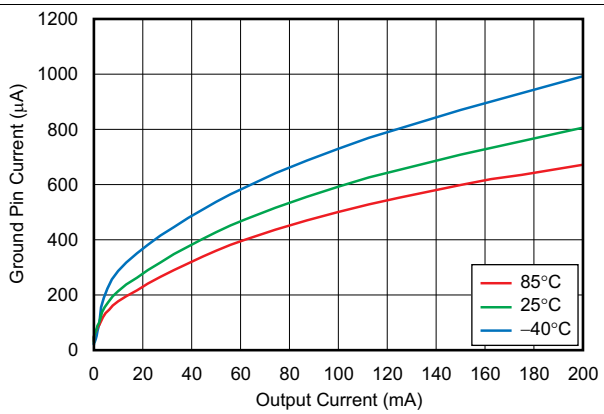
V_{OUT} = 2.8 V, I_{OUT} = 0 mA

图 15. Ground Pin Current vs Temperature



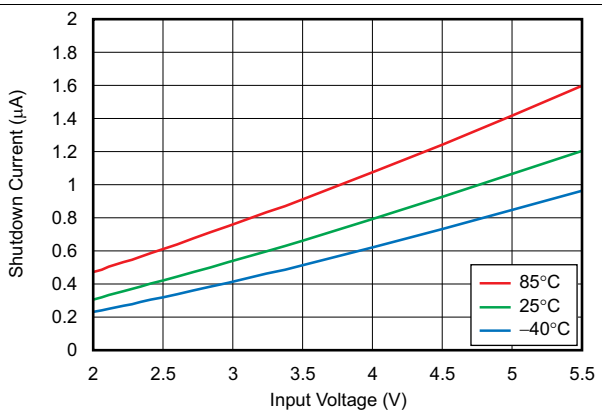
V_{OUT} = 1.2 V

图 16. Ground Pin Current vs Output Current



V_{OUT} = 2.8 V

图 17. Ground Pin Current vs Output Current

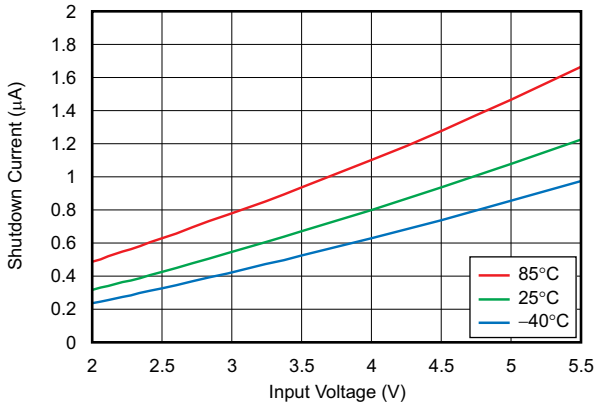


V_{OUT} = 1.2 V

图 18. Shutdown Current vs Input Voltage

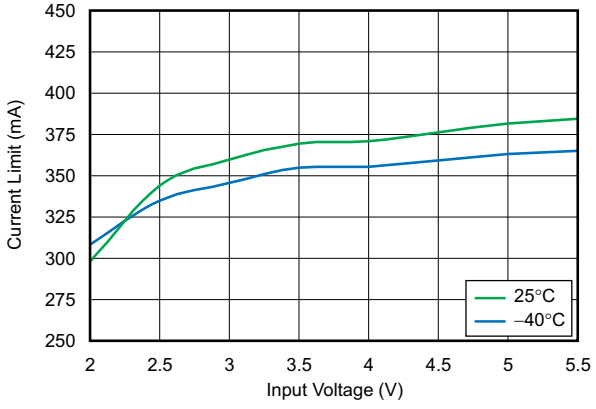
Typical Characteristics (接下页)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



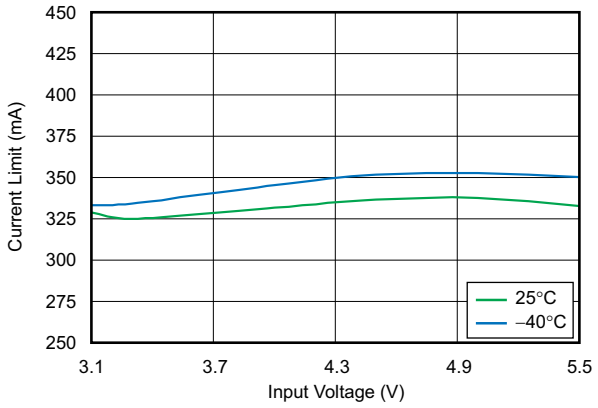
V_{OUT} = 2.8 V

图 19. Shutdown Current vs Input Voltage



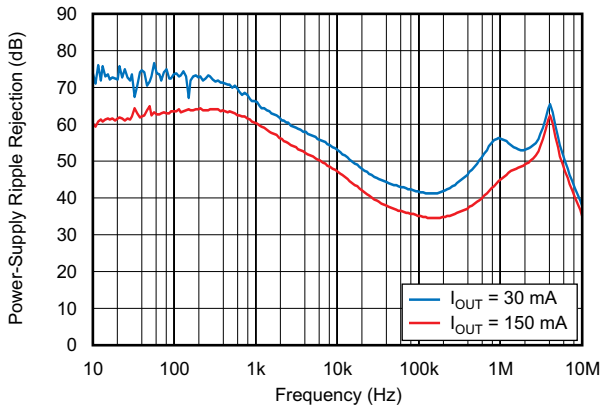
V_{OUT} = 1.2 V

图 20. Current Limit vs Input Voltage



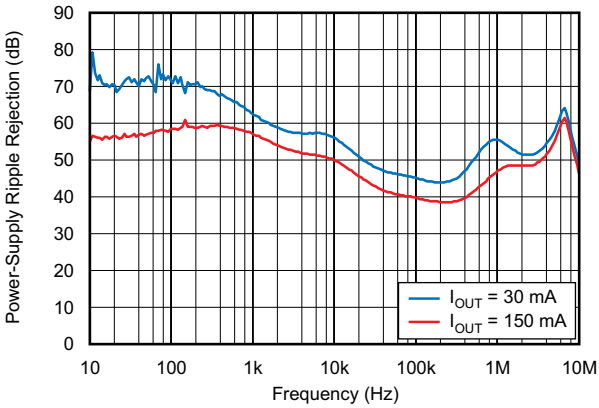
V_{OUT} = 2.8 V

图 21. Current Limit vs Input Voltage



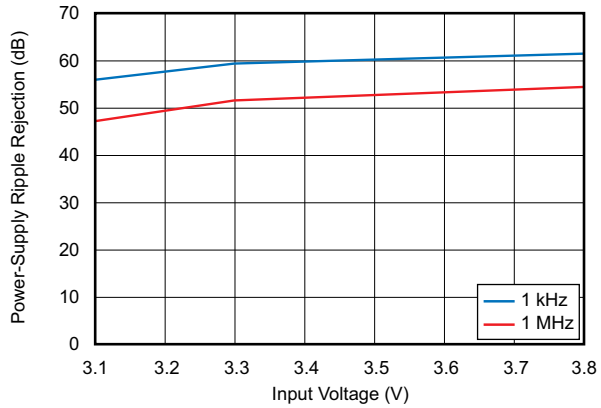
V_{OUT} = 1.2 V

图 22. Power-Supply Ripple Rejection vs Frequency



V_{OUT} = 2.8 V

图 23. Power-Supply Ripple Rejection vs Frequency

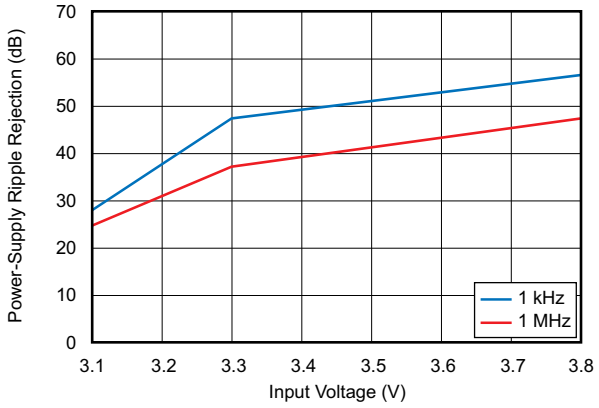


V_{OUT} = 2.8 V, I_{OUT} = 30 mA

图 24. Power-Supply Ripple Rejection vs Input Voltage

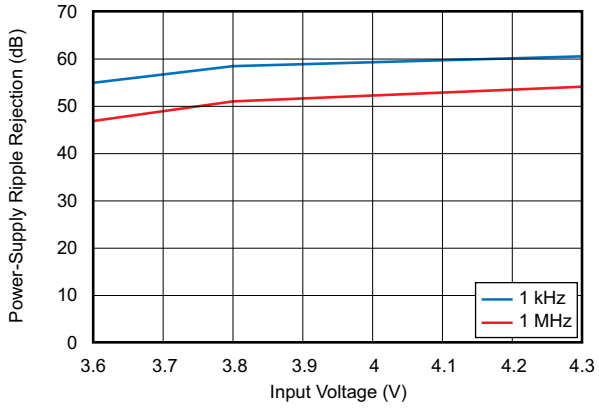
Typical Characteristics (接下页)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



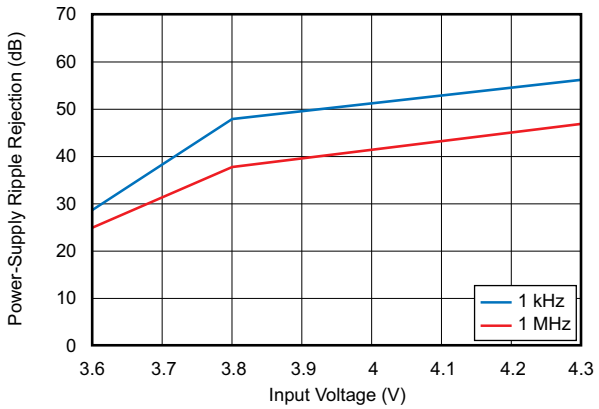
V_{OUT} = 2.8 V, I_{OUT} = 150 mA

图 25. Power-Supply Ripple Rejection vs Input Voltage



V_{OUT} = 3.3 V, I_{OUT} = 30 mA

图 26. Power-Supply Ripple Rejection vs Input Voltage



V_{OUT} = 3.3 V, I_{OUT} = 150 mA

图 27. Power-Supply Ripple Rejection vs Input Voltage

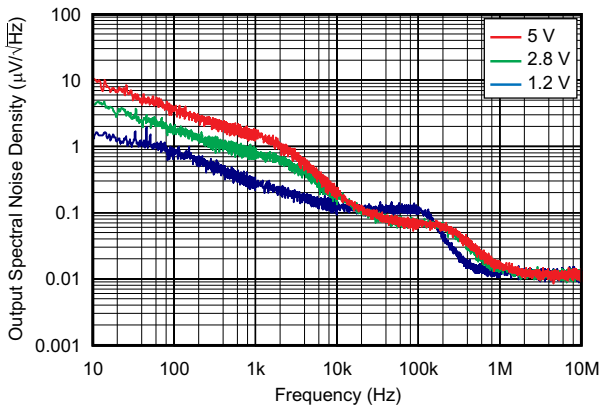
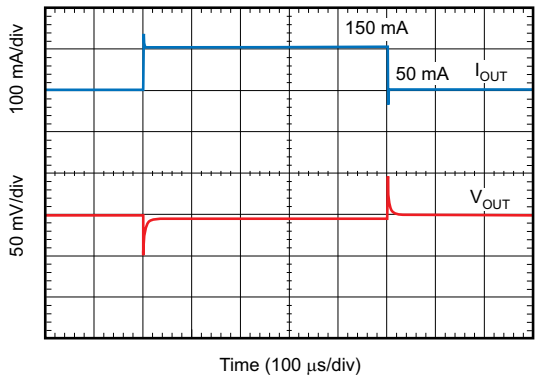
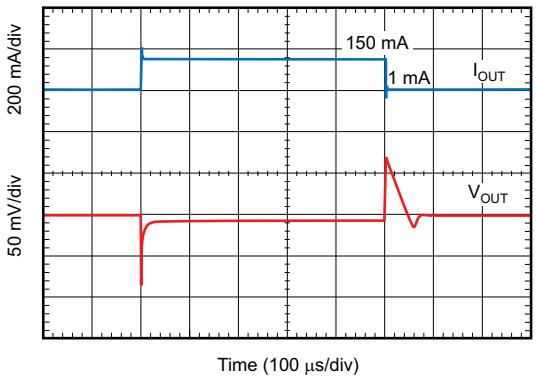


图 28. Output Spectral Noise Density vs Frequency



V_{OUT} = 1.2 V

图 29. Load Transient Response

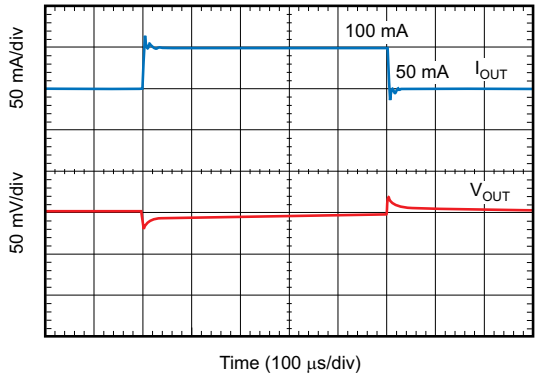


V_{OUT} = 1.2 V

图 30. Load Transient Response

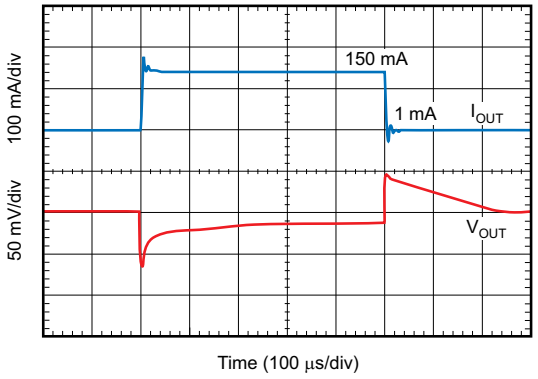
Typical Characteristics (接下页)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



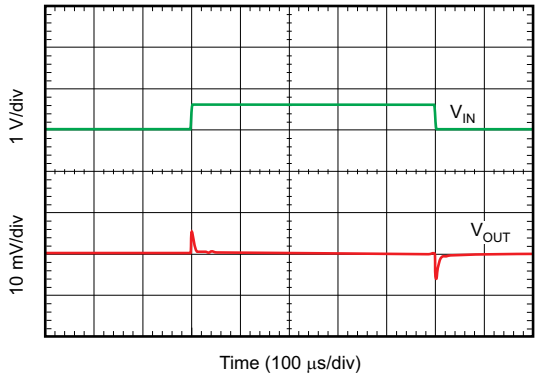
V_{OUT} = 2.8 V

图 31. Load Transient Response



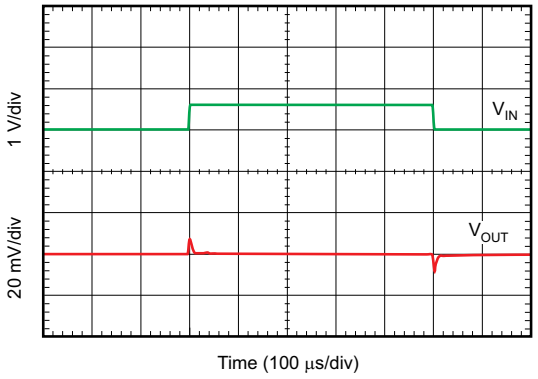
V_{OUT} = 2.8 V

图 32. Load Transient Response



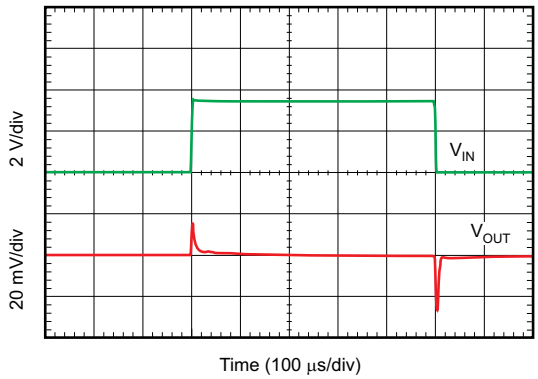
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

图 33. Line Transient Response



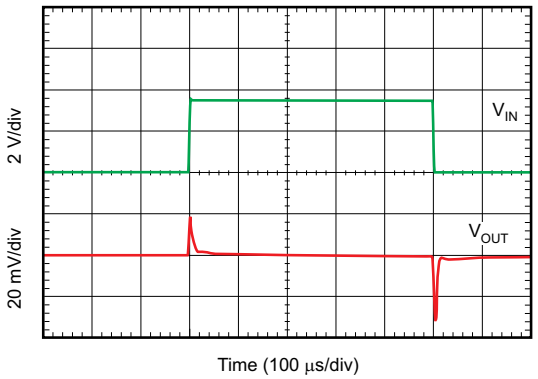
V_{OUT} = 1.2 V, I_{OUT} = 200 mA

图 34. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 150 mA

图 35. Line Transient Response

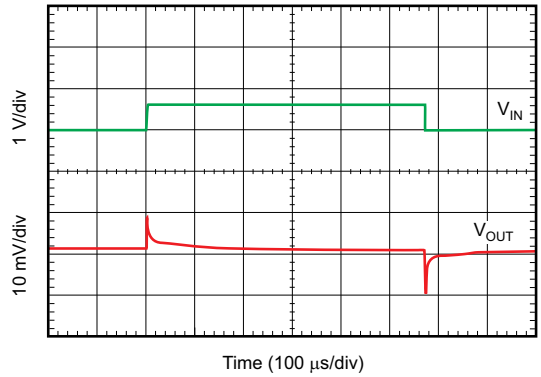


V_{OUT} = 1.2 V, I_{OUT} = 200 mA

图 36. Line Transient Response

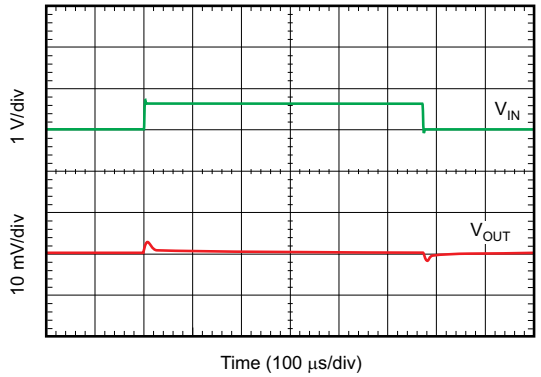
Typical Characteristics (接下页)

at T_J = –40°C to +85°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF
Typical values are at T_J = 25°C, (unless otherwise noted)



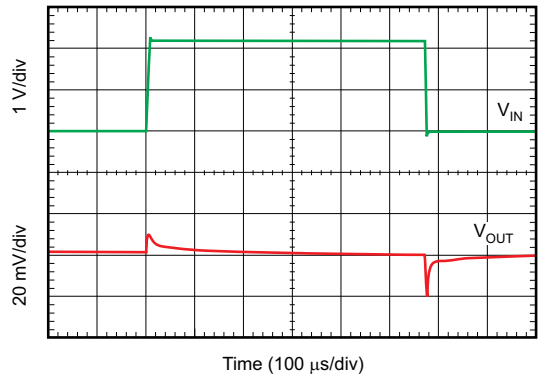
V_{OUT} = 2.8 V, I_{OUT} = 150 mA

图 37. Line Transient Response



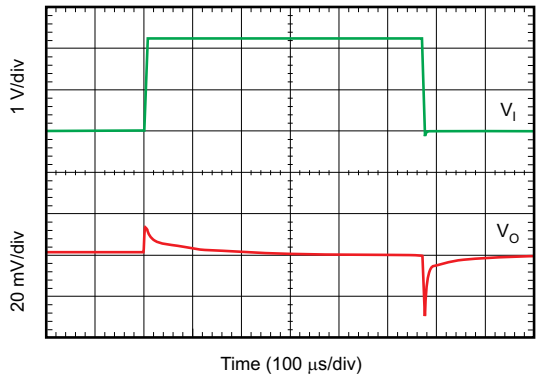
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

图 38. Line Transient Response



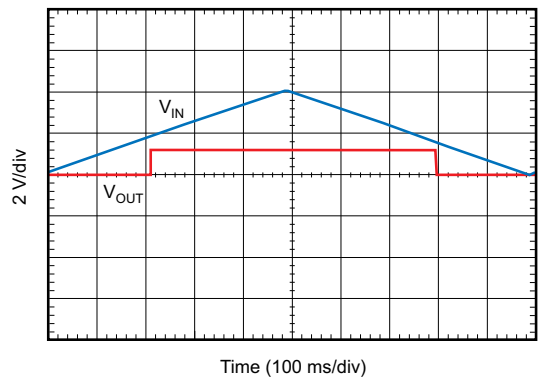
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

图 39. Line Transient Response



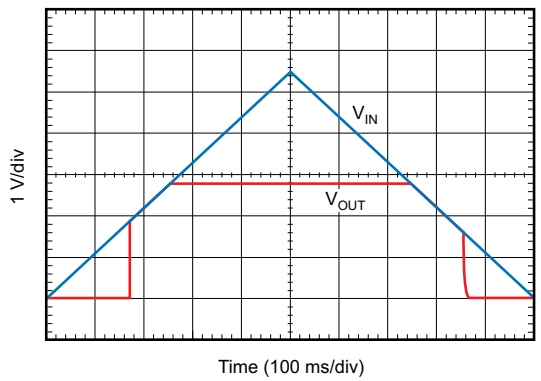
V_{OUT} = 2.8 V, I_{OUT} = 200 mA

图 40. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 30 mA

图 41. V_{IN} Ramp Up, Ramp Down Response



V_{OUT} = 2.8 V, I_{OUT} = 30 mA

图 42. V_{IN} Ramp Up, Ramp Down Response

7 Detailed Description

7.1 Overview

The TLV742P device belongs to a family of LDOs. This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics [combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom] make this device ideal for portable RF applications.

7.2 Functional Block Diagrams

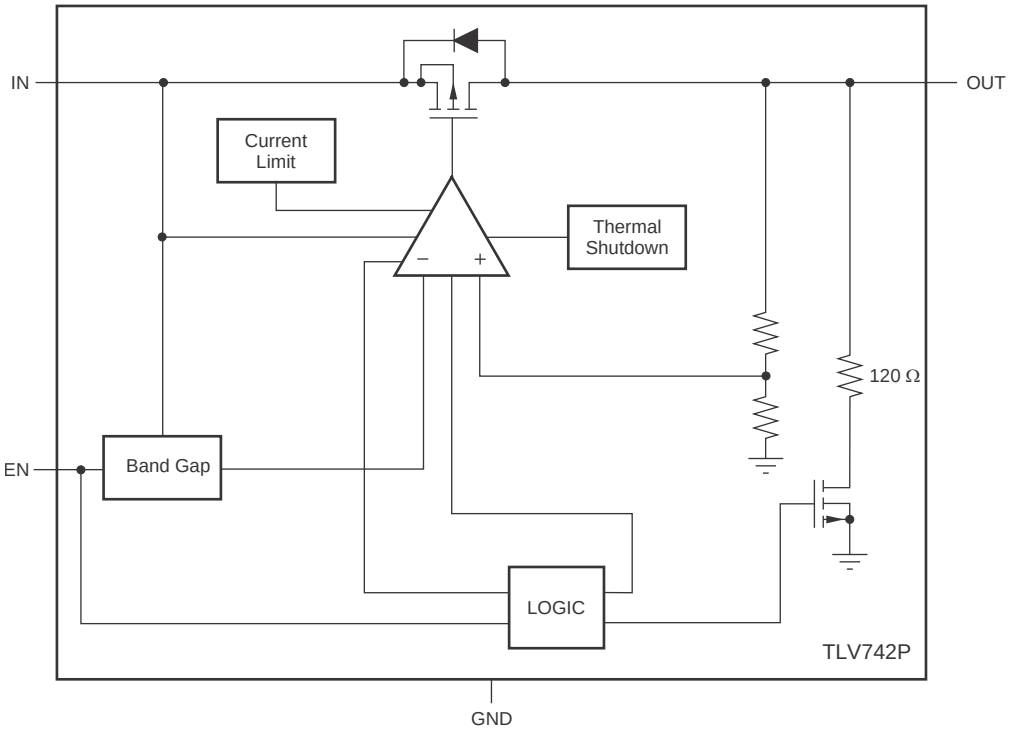


图 43. TLV742P Block Diagram

7.3 Feature Description

This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device is –40°C to +125°C.

7.3.1 Internal Current Limit

The internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{CL} \times R_L$. The PMOS pass transistor dissipates (V_{IN} – V_{OUT}) × I_{LIMIT} until thermal shutdown is triggered and the device turns off. When the device cools, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see *Thermal Information* for more details.

The PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (接下页)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at the EN pin goes above 0.9 V. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV742P version has internal active pulldown circuitry that discharges the output with a time constant as given by 公式 1:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

7.4 Device Functional Modes

The TLV742P series is specified over the recommended operating conditions (see *Recommended Operating Conditions*). The specifications may not be met when exposed to conditions outside of the recommended operating range.

To turn on the regulator, the EN pin must be driven over 0.9 V. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device typically reduces to 1 µA.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV742P is a LDO with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers current limit and thermal protection. The operating junction temperature of this device series is –40°C to +125°C.

8.2 Typical Application

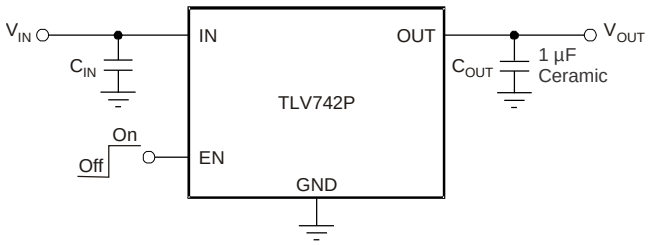


图 44. Typical Application Circuit

8.2.1 Design Requirements

Provide an input supply with adequate headroom to meet minimum V_{IN} requirements (as listed in 表 1), compensate for the GND pin current, and to power the load.

表 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V to 3.6 V
Output voltage	1.2 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Generally, 1-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV742P is designed to be stable with an effective capacitance of 0.1 µF or larger at the output. As a result, the device is stable with capacitors of other dielectric types if the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking bias voltage and temperature derating into consideration. In addition to using less expensive dielectrics, this stability with 0.1-µF effective capacitance enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions is less than 0.1 µF. Maximum ESR must be less than 200 mΩ.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be required if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2-Ω, a 0.1-µF input capacitor may be required to ensure stability.

8.2.2.2 Dropout Voltage

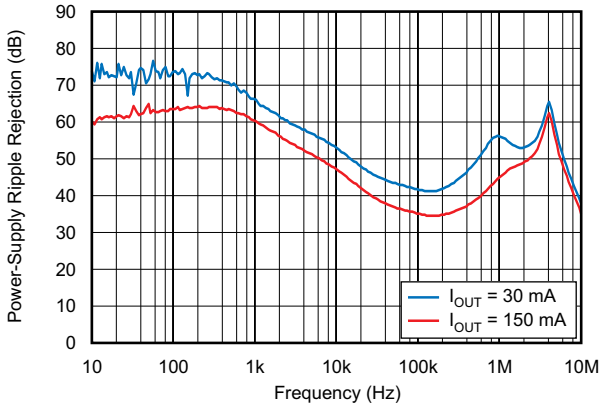
The TLV742P series of LDOs use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device functions similar to a resistor in dropout.

PSRR and transient response degrade when (V_{IN} – V_{OUT}) approaches dropout.

8.2.2.3 Transient Response

Increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves



V_{OUT} = 1.2 V

图 45. Power-Supply Ripple Rejection vs Frequency

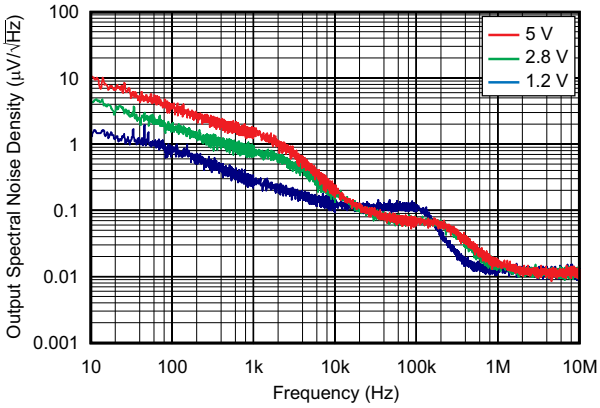
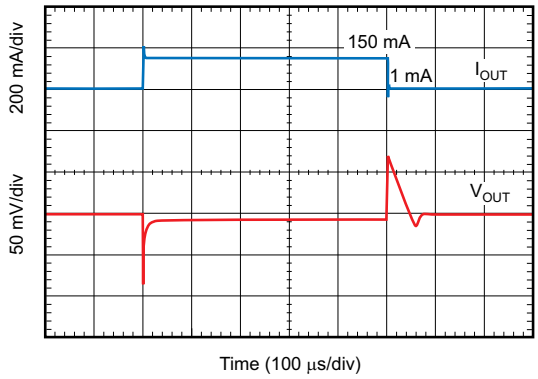
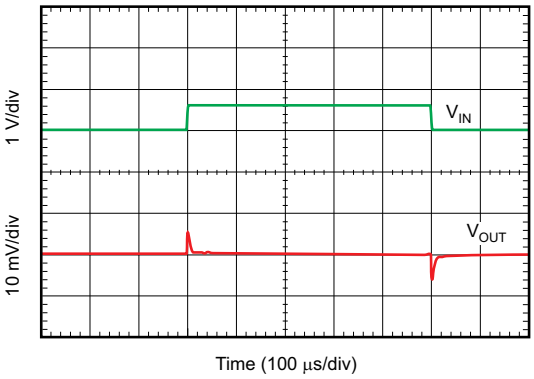


图 46. Output Spectral Noise Density vs Frequency



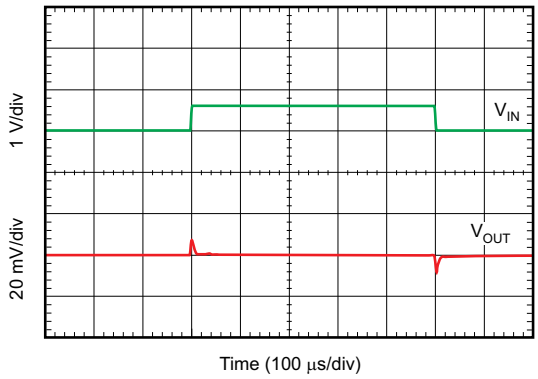
V_{OUT} = 1.2 V

图 47. Load Transient Response



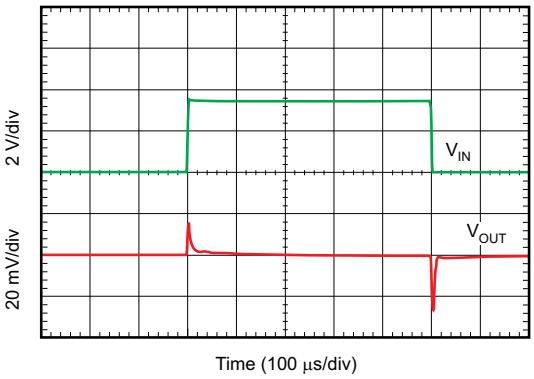
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

图 48. Line Transient Response



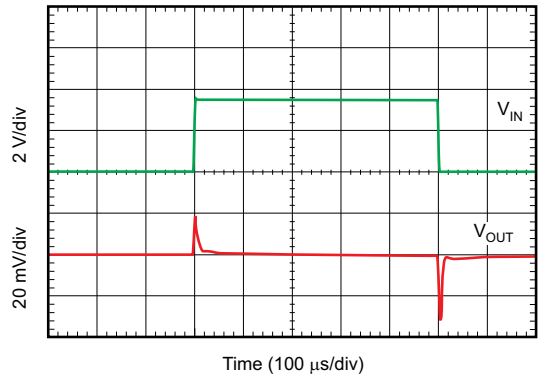
V_{OUT} = 1.2 V, I_{OUT} = 200 mA

图 49. Line Transient Response



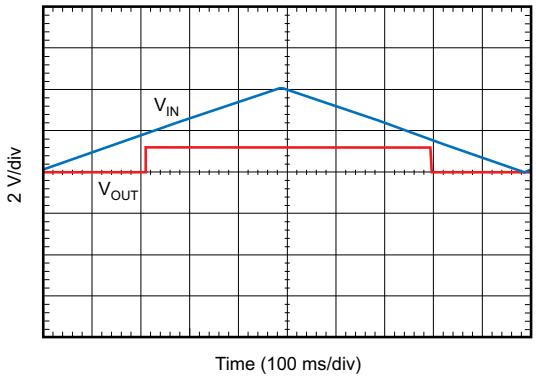
V_{OUT} = 1.2 V, I_{OUT} = 150 mA

图 50. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 200 mA

图 51. Line Transient Response



V_{OUT} = 1.2 V, I_{OUT} = 30 mA

图 52. V_{IN} Ramp Up, Ramp Down Response

8.3 Do's and Don'ts

Place at least one 1-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Connect a 1-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator for improved transient performance.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2 V and 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well-regulated (see 图 33 through 图 40). If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Place input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device, as shown in 图 53. Connect the ground connection for the output capacitor directly to the GND pin of the device. High ESR capacitors can degrade PSRR performance.

10.1.2 Package Mounting

Solder pad footprint recommendations are available from the TI website at www.ti.com. The recommended land pattern for the DQN (X2SON-4) package is provided in the *机械、封装和可订购信息* section.

10.2 Layout Example

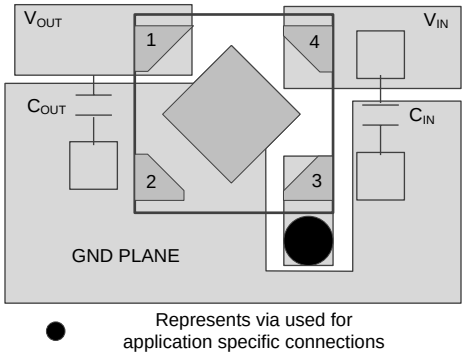


图 53. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enables again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, which protects the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the LDO is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the LDO into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for JEDEC low- and high-K boards are shown in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers improves heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in 公式 2.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

我们提供了一款评估模块 (EVM)，可与 TLV742P 配套使用，帮助评估初始电路性能。 *TLV70728EVM-612* 详细介绍了 TLV70728EVM-612 的设计套件和评估模块。

可通过德州仪器 (TI) 网站上的 TLV742P 产品文件夹申请获取该 EVM，也可以直接从 TI 网上商店购买。

11.1.2 器件命名规则

订购信息(1)

产品	V_{OUT}(2)
TLV742**xx(x)***Pyyyz*	**XX(X)** 是标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，18 = 1.8V，285 = 2.85V）。 **P** 为可选项；P 表示器件具有一个带有源输出放电功能的 LDO 稳压器。 **YYY** 为封装标识符。 **Z** 为封装数量。***R*** 表示卷（3000 片），***T*** 表示带（250 片）。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹，此文件夹位于www.ti.com.cn内。
(2) 可提供 0.85V 至 5V 范围内的输出电压（以 50mV 为单位增量）。请与厂方联系以了解详细信息和可用性。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV74211PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8H	Samples
TLV74212PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8G	Samples
TLV74215PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8F	Samples
TLV74218PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8E	Samples
TLV74225PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CS	Samples
TLV74227PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8D	Samples
TLV74228PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8C	Samples
TLV74229PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8B	Samples
TLV74230PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT	Samples
TLV74233PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7Z	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

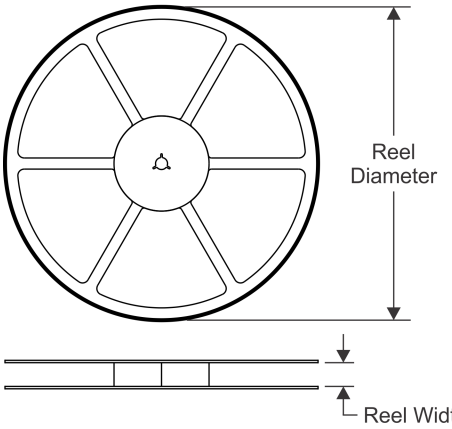
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

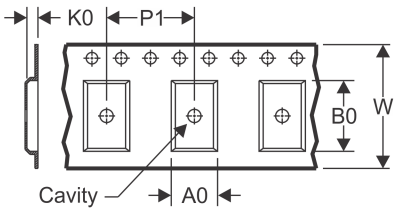
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

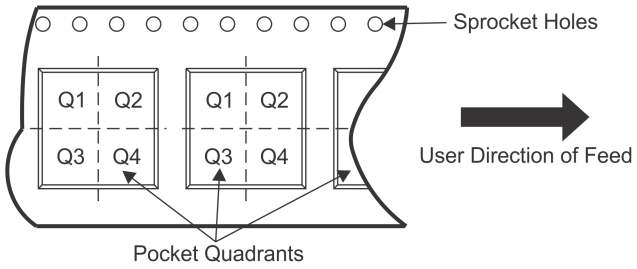


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

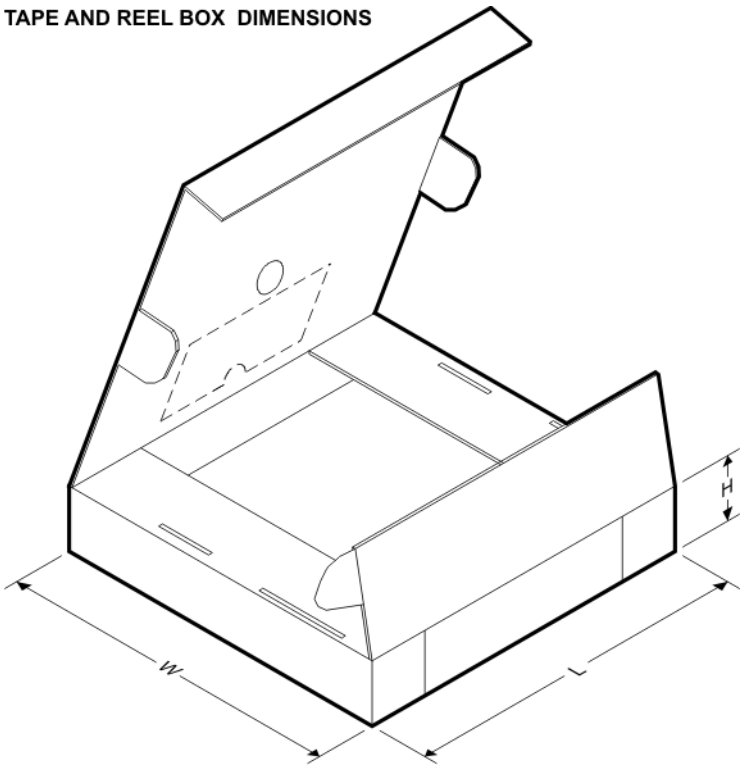
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74211PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74212PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74215PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74218PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74225PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74227PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74228PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74229PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74230PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2
TLV74233PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.53	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74211PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74212PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74215PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74218PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74225PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74227PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74228PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74229PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74230PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3
TLV74233PDQNR	X2SON	DQN	4	3000	203.2	196.8	33.3

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

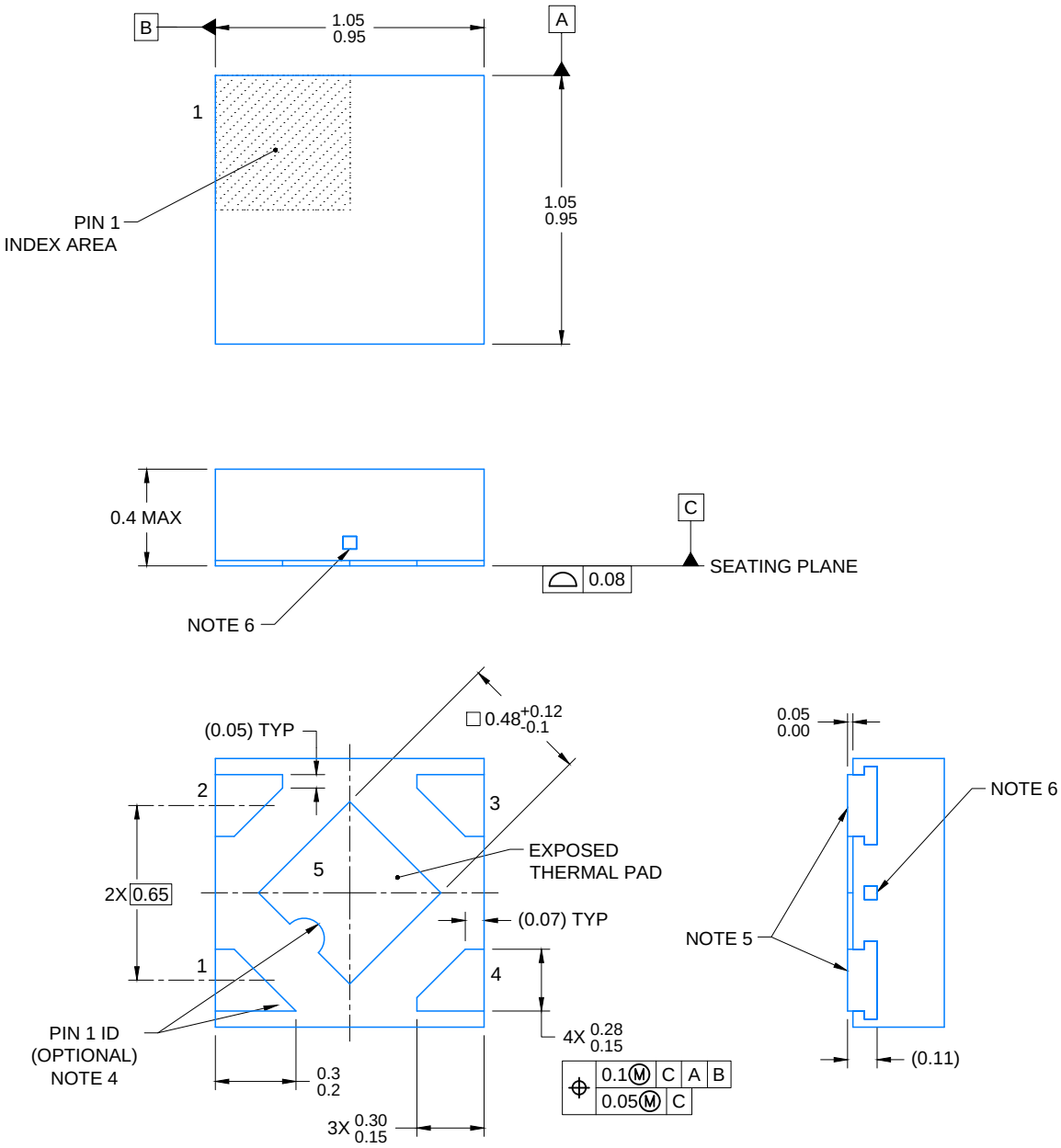
4210367/F

PACKAGE OUTLINE

DQN0004A

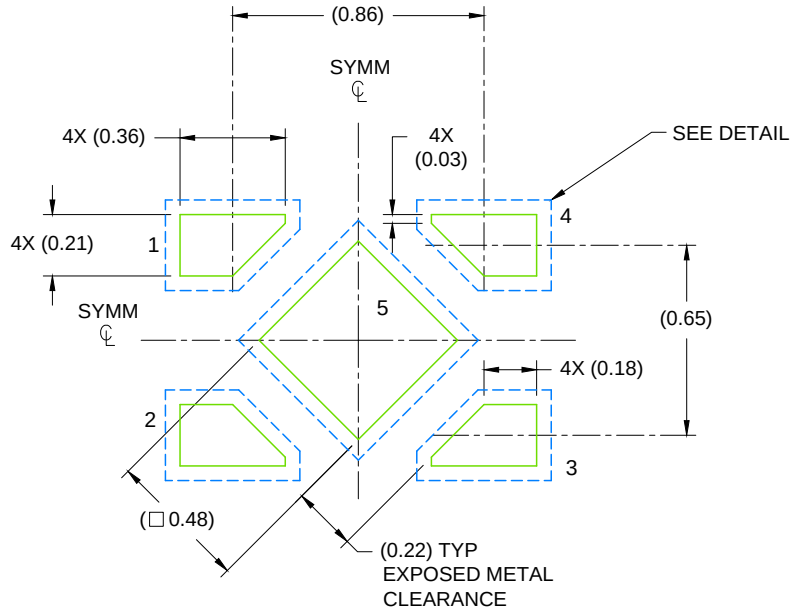
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



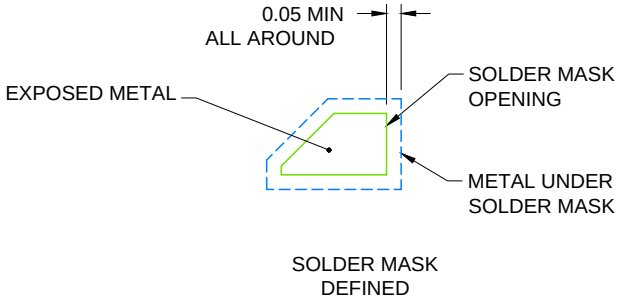
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X



SOLDER MASK DETAIL

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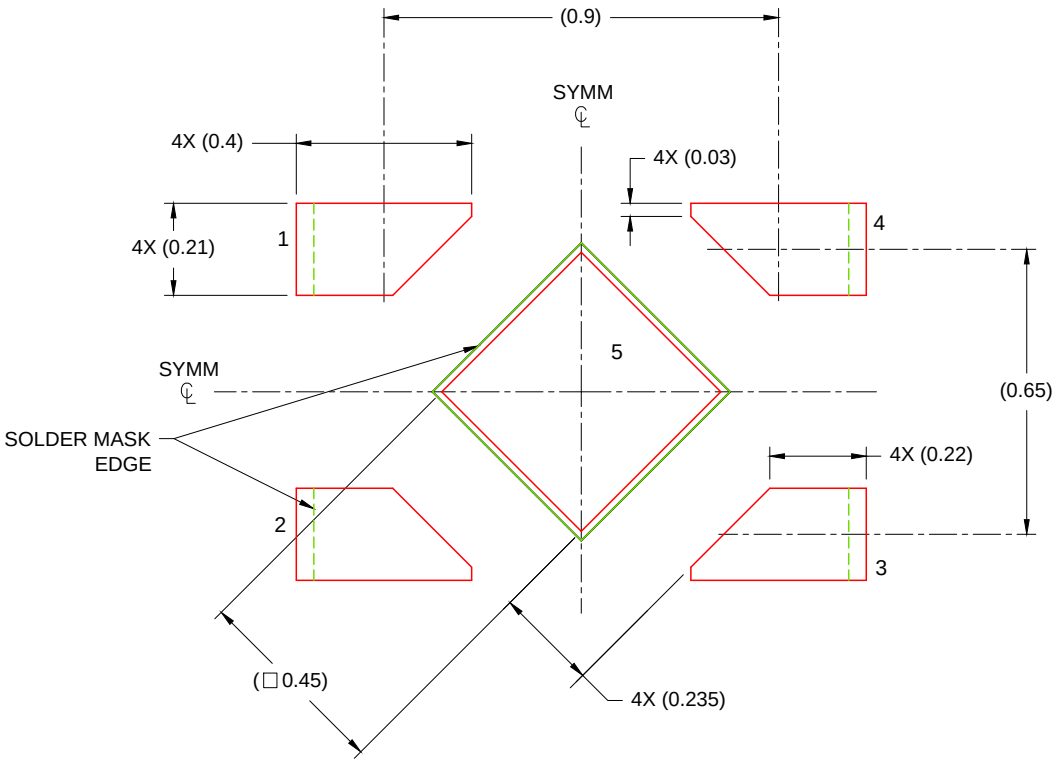
NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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