采用小型 0402 封装的 TMP63 100kΩ 线性热敏电阻

1 特性

- 具有
  正温度系数 (PTC) 的硅基热敏电阻
- 与非线性热敏电阻相比，线性热敏电阻随温度变化
  - 可简化电阻/温度转换方法
  - 可降低查找表内存要求
  - 无需线性化电路或多点校准
  - 可降低在宽温度范围内的精度
- 在 25°C 下具有 100kΩ 标称电阻 (R25)
- 在整个温度范围内具有稳定的灵敏度
  - 6400ppm/°C TCR (25°C)
  - 在整个温度范围内具有 0.2% 的典型 TCR 容差（-40°C 至 125°C）
- 宽工作温度范围：
  - –40°C 至 125°C
- 快速热响应时间：
  - 对于 DEC 封装为 0.6秒
- 长寿命和稳健性能
  - 与由于自加热而尽可能降低误差的传统 NTC 相比，具有超低功耗
  - 内置失效防护，能够在发生短路故障时提供保护
  - 在高温和高湿度环境下测试后可实现 <1% 的最大漂移
- 提供的封装选项：
  - X1SON（DEC/0402 封装尺寸）

2 应用

- 温度测量与监测
- 热补偿
- 热保护（带有比较器）

3 说明

TMP63 小型硅线性热敏电阻用于温度测量、保护、补偿和控制系统。与传统 NTC 热敏电阻相比，TMP63 器件可在整个温度范围内提供增强的线性和一致的灵敏度。

TMP63 器件具有稳健的性能，这得益于它对环境变化的抗扰能力和内置的高温下失效防护行为。此器件目前可采用兼容 0402 尺寸的 2 引脚表面贴装 X1SON 封装、。

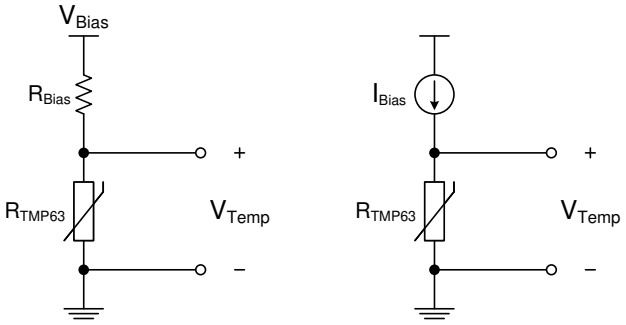
器件信息(1)

器件型号	封装	封装尺寸（标称值）
TMP63	X1SON (2)	0.60mm x 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

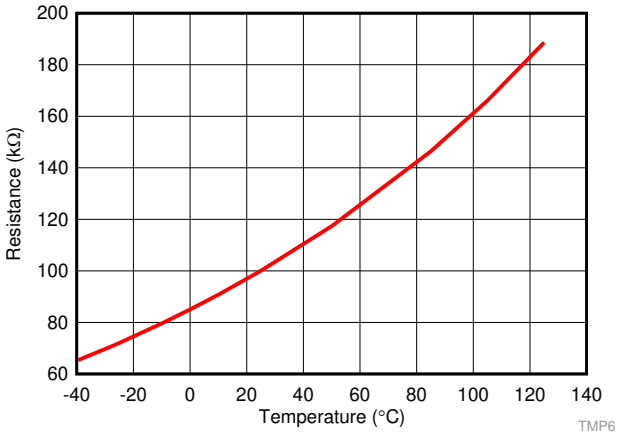
ADVANCE INFORMATION

典型实施电路



$$V_{Temp} = \frac{V_{Bias} * R_{TMP63}}{R_{Bias} + R_{TMP63}} \qquad V_{Temp} = I_{Bias} * R_{TMP63}$$

典型电阻与环境温度间的关系



目录

ADVANCE INFORMATION

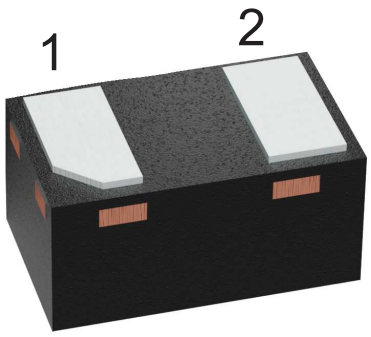
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	版本	注释
2019 年 10 月	*	最初发布版本。

5 Pin Configuration and Functions

DEC Package
2-Pin X1SON
Top View (Angled)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	X1SON (DEC)		
–	1	—	Thermistor (–) and (+) terminals. For proper operation, ensure a positive bias where the + terminal is at a higher voltage potential than the – terminal.
+	2		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage across the device		+6	V
Junction temperature (T_J)	–40	+150	°C
Current through the device		+450	µA
Storage temperature (T_{stg})	–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) per JESD22-A114 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{Sns}	Voltage Across Pins 2 (+) and 1 (–)	0		5.5	V
I_{Sns}	Current passing through the device	0		400	µA
T_A	Operating free-air temperature (specified performance) (X1SON/DEC Package)	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMP63 DEC (X1SON) 2 PINS	Units
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2) (3)	443.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	195.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	254.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	254.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction to ambient thermal resistance ($R\theta_{JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(3) Changes in output due to self heating can be computed by multiplying the internal dissipation by the thermal resistance.

ADVANCE INFORMATION

6.5 Electrical Characteristics

T_A = -40°C - 125°C, I_{Sns} = 20 μA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{25}	Thermistor Resistance at 25°C	T_A = 25°C		100		kΩ
R_{TOL}	Resistance Tolerance	T_A = 25°C	–1		+1	%
		T_A = 0°C - 70°C	–1		+1	
		T_A = -40°C - 125°C	–1.5		+1.5	
TCR_{-35}	Temperature Coefficient of Resistance	T1 = -40°C, T2 = -30°C		+6220		ppm/°C
TCR_{25}		T1 = 20°C, T2 = 30°C		+6400		
TCR_{85}		T1 = 80°C, T2 = 90°C		+5910		
TCR_{-35} %	Temperature Coefficient of Resistance Tolerance	T1 = -40°C, T2 = -30°C		±0.4		%
TCR_{25} %		T1 = 20°C, T2 = 30°C		±0.2		
TCR_{85} %		T1 = 80°C, T2 = 90°C		±0.3		
ΔR	Sensor Long Term Drift (Reliability)	96 hours continuous operation,RH=85%, T_A = 130°C, V_{Bias} = 5.5V	0.1		+0.8	%
		600 hours continuous operation, T_A = 150°C, V_{Bias} = 5.5V	0.1		+1	
$t_{RES\ (stirred\ liquid)}$	Thermal response to 63%	T1=25°C in Still Air to T2=125°C in Stirred Liquid		0.6		s
$t_{RES\ (still\ air)}$	Thermal response to 63%	T1=25°C to T2=70°C in Still Air		3.2		s

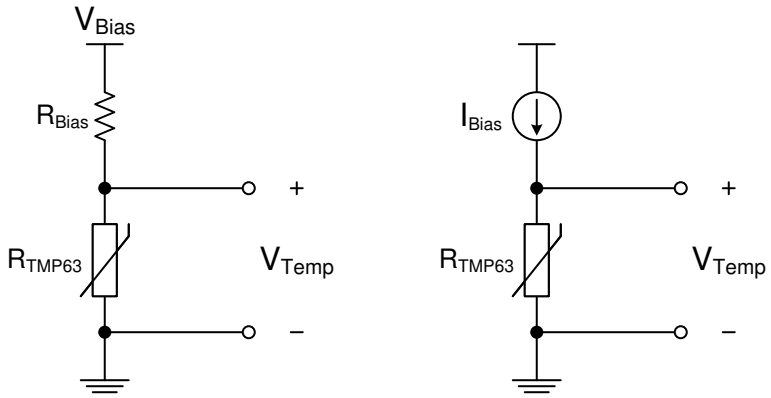
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The TMP63 series of silicon linear thermistors has a linear positive temperature coefficient (PTC) that results in a uniform and consistent temperature coefficient resistance (TCR) across a wide operating temperature range.

7.2 Functional Block Diagram



$$V_{Temp} = \frac{V_{Bias} * R_{TMP63}}{R_{Bias} + R_{TMP63}} \qquad V_{Temp} = I_{Bias} * R_{TMP63}$$

图 1. Typical Implementation Circuits

7.3 Feature Description

The TMP63 has good linear behaviour across the whole temperature range, but a small non-linearity can be observed as well as supply dependence. To fabricate the TMP63, the engineer can use a special silicon process where the device key characteristics—the temperature coefficient resistance (TCR) and nominal resistance (R25)—are controlled by the doping level and active region area. Note that the TMP63 has an active area and a substrate due to the polarized terminals of the device. The positive terminal should be connected to the highest potential, while the negative terminal (which is tied to the substrate internally) should be connected to the lowest potential. 公式 1 can help the user approximate the TCR.

表 1 and 表 2 show the typical resistance, resistance spread, and maximum expected error across temperature using a direct ideal bias current or an ideal voltage bias in a divider circuit. The tables provided are for specific applications. 表 1 is for constant current applications supplying 20 µA of constant current. 表 2 is for a circuit having a bias voltage of 2.5 V supplying a resistor divider consisting of a top resistor of 100 kΩ with the TMP63 on the bottom. These tables are not to be used if operating either circuit under different currents, bias voltages or different Resistor values. New tables will be required based on your specific design.

$$\text{TCR (ppm/°C)} = (R_{T2} - R_{T1}) / ((T_2 - T_1) \times R_{(T2+T1)/2}) \quad (1)$$

Below are the definitions of the key terms used throughout this document:

- I_{Sns}: Current flowing through the TMP63.
- V_{Sns}: Voltage across the two TMP63 terminals.
- I_{Bias}: Current supplied by the biasing circuit.
- V_{Bias}: Voltage supplied by the biasing circuit.
- V_{Temp}: Output voltage that corresponds to the measured temperature. Note that this is different from V_{Sns}. In the use case of a voltage divider circuit with the TMP63 in the high side, V_{Temp} is taken across R_{Bias}.

ADVANCE INFORMATION

Feature Description (接下页)

表 1. TMP63 Transfer Table Using an Ideal I_{Bias} of 20 µA (1) [DEC Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(2)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(3)(2) (°C)
	MIN	TYP	MAX		
–40	64426	65407	66388	416	2.36
–35	66526	67539	68552	436	2.32
–30	68723	69769	70816	456	2.30
–25	71012	72093	73175	474	2.28
–20	73391	74509	75626	492	2.27
–15	75857	77012	78168	509	2.27
–10	78408	79602	80796	526	2.27
–5	81042	82276	83510	543	2.27
0	84181	85032	85882	559	1.52
5	86989	87868	88747	575	1.53
10	89876	90784	91692	591	1.54
15	92840	93778	94716	607	1.55
20	95882	96850	97819	622	1.56
25	99000	100000	101000	638	1.57
30	102196	103228	104260	653	1.58
35	105469	106534	107599	669	1.59
40	108820	109919	111018	685	1.60
45	112250	113383	114517	701	1.62
50	115760	116929	118098	717	1.63
55	119352	120557	121763	734	1.64
60	123028	124270	125513	751	1.65
65	126790	128070	129351	769	1.67
70	130640	131960	133279	787	1.68
75	133902	135941	137980	806	2.53
80	137918	140018	142119	825	2.55
85	142031	144194	146357	845	2.56
90	146246	148473	150700	866	2.57
95	150566	152859	155151	888	2.58
100	154995	157355	159716	911	2.59
105	159539	161968	164398	934	2.60
110	164201	166702	169202	959	2.61
115	168988	171562	174135	985	2.61
120	173906	176554	179202	1012	2.62
125	178959	181684	184409	1040	2.62

(1) Changing the specified current will require a new 4th order polynomial to create a resistance table for your design
(2) Table defined based on 4th order equation: $R(\Omega) = 85031.7 + 559.26 * T + 1.6114 * T^4 - (1.79E\text{-}3) * T^3 + (2.07E\text{-}5) * T^4$
(3) Assuming ideal current source

ADVANCE INFORMATION

表 2. TMP63 Transfer Table Using a Voltage Divider With an Ideal V_{Bias} of 2.5 V(1)and R_{Bias} of 100 kΩ With ±0.01% Tolerance(1)[DEC Package]

TEMPERATURE (°C)	RESISTANCE (Ω)(2)			ΔR/ΔT (Ω/°C)	TEMPERATURE ERROR(3) (°C)
	MIN	TYP	MAX		
–40	64032	65007	65982	424	2.30
–35	66154	67162	68169	438	2.30
–30	68348	69389	70430	453	2.30
–25	70614	71689	72764	467	2.30
–20	72952	74062	75173	482	2.30
–15	75362	76510	77658	497	2.31
–10	77846	79032	80217	512	2.32
–5	80404	81628	82853	527	2.32
0	83457	84300	85143	542	1.56
5	86177	87047	87918	557	1.56
10	88972	89871	90770	572	1.57
15	91844	92772	93699	588	1.58
20	94792	95750	96707	603	1.59
25	97818	98806	99794	619	1.60
30	100921	101940	102960	635	1.61
35	104102	105154	106205	651	1.62
40	107363	108447	109532	667	1.63
45	110703	111821	112939	683	1.64
50	114124	115276	116429	699	1.65
55	117625	118813	120001	716	1.66
60	121209	122433	123657	732	1.67
65	124874	126136	127397	749	1.68
70	128623	129923	131222	766	1.70
75	131787	133794	135801	783	2.56
80	135685	137752	139818	800	2.58
85	139668	141795	143922	817	2.60
90	143737	145926	148115	835	2.62
95	147893	150145	152398	853	2.64
100	152137	154454	156770	871	2.66
105	156469	158852	161234	889	2.68
110	160890	163340	165790	907	2.70
115	165402	167921	170440	925	2.72
120	170005	172594	175183	944	2.74
125	174700	177361	180021	963	2.76

(1) Changing the specified voltage or resistance will require a new 4th order polynomial to create a resistance table for your design.
(2) Table defined based on 4th order equation: $R(\Omega) = 84229.91 + 541.907 * T + 1.515 * T^3 + (6.84E\text{-}4) * T^3 + (1.29E\text{-}6) * T^4$
(3) Assuming ideal voltage source, 100 kΩ with ±0.01% R_{Bias}

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the *Recommended Operating Conditions*.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP63 is a positive temperature coefficient (PTC) linear silicon thermistor. The device behaves like a temperature-dependent resistor, and may be configured in a variety of ways to monitor temperature based on the system-level requirements. The TMP63 has a nominal resistance at 25°C (R25) of 100 kΩ, a maximum operating voltage of 5.5 V (V_{Sns}), and maximum supply current of 400 µA (I_{Sns}). This device may be used in a variety of applications to monitor temperature close to a heat source with the very small DEC package option compatible with the typical 0402 (inch) footprint. Some of the factors that influence the total measurement error include the ADC resolution (if applicable), the tolerance of the bias current or voltage, the tolerance of the bias resistance in the case of a voltage divider configuration, and the location of the sensor with respect to the heat source.

8.2 Typical Application

8.2.1 Thermistor Biasing Circuits

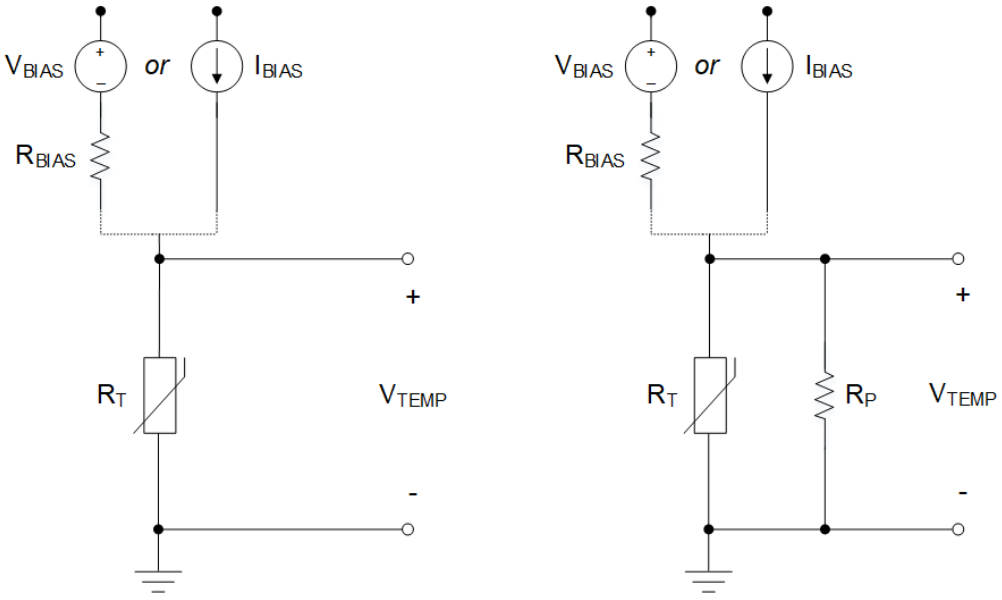


Figure 2. Biasing Circuit Implementations With Linear Thermistor (Left) vs. Non-Linear Thermistor (Right)

8.2.1.1 Design Requirements

Existing thermistors, in general, have a non-linear temperature vs. resistance curve. To linearize the thermistor response, the engineer can use a voltage linearization circuit with a voltage divider configuration, or a resistance linearization circuit by adding another resistance in parallel with the thermistor, R_P. Figure 2 highlights the two implementations where R_T is the thermistor resistance. To generate an output voltage across the thermistor, the engineer can use a voltage divider circuit with the thermistor placed at either the high side (close to supply) or low side (close to ground), depending on the desired voltage response (negative or positive). Alternatively, the resistor can be biased directly using a precision current source (yielding the highest accuracy and voltage gain).

ADVANCE INFORMATION

Typical Application (continued)

It is common to use a voltage divider with thermistors because of its simple implementation and lower cost. The TMP63, on the other hand, has a linear positive temperature coefficient (PTC) of resistance such that the voltage measured across it increases linearly with temperature. As such, the need for linearization circuits is no longer a requirement, and a simple current source or a voltage divider circuit can be used to generate the temperature voltage.

This output voltage can be interpreted using a comparator against a voltage reference to trigger a temperature trip point that is either tied directly to an ADC to monitor temperature across a wider range or used as feedback input for an active feedback control circuit.

The voltage across the TMP63 can be translated to temperature using either a lookup table method (LUT) or a fitting polynomial, V(T), as described in Equation 2. The temperature voltage must first be digitized using an ADC. The necessary resolution of this ADC is dependent on the biasing method used. Additionally, for best accuracy, the bias voltage (V_{BIAS}) should be tied to the reference voltage of the ADC to create a measurement where the difference in tolerance between the bias voltage and the reference voltage cancels out. The engineer can also implement a low-pass filter to reject system level noise, and the user should place the filter as close to the ADC input as possible.

8.2.1.2 Detailed Design Procedure

The resistive circuit divider method produces an output voltage (V_{TEMP}) scaled according to the bias voltage (V_{BIAS}). When V_{BIAS} is also used as the reference voltage of the ADC, any fluctuations or tolerance error due to the voltage supply will be canceled and will not affect the temperature accuracy. This type of configuration is shown in Figure 3. Equation 2 describes the output voltage (V_{TEMP}) based on the variable resistance of the TMP63 (R_{TMP63}) and bias resistor (R_{BIAS}). The ADC code that corresponds to that output voltage, ADC full-scale range, and ADC resolution is given in Equation 3.

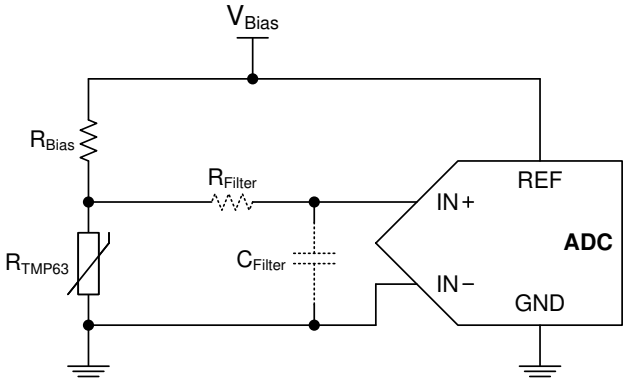


Figure 3. TMP63 Voltage Divider With an ADC

$$V_{Temp} = V_{Bias} * \left(\frac{R_{TMP63}}{R_{Bias} + R_{TMP63}}\right) \quad (2)$$

$$ADC\ Code = \left(\frac{V_{Temp}}{FSR}\right) * 2^n \quad (3)$$

where

- FSR is the full-scale range of the ADC, which is the voltage at REF to GND (V_{REF})
- n is the resolution of the ADC

Equation 4 shows whenever $V_{REF} = V_{BIAS}$, V_{BIAS} cancels out.

$$ADC\ Code = \left(\frac{V_{Bias} * \left(\frac{R_{TMP63}}{R_{Bias} + R_{TMP63}}\right)}{V_{Bias}}\right) * 2^n = \left(\frac{R_{TMP63}}{R_{Bias} + R_{TMP63}}\right) * 2^n \quad (4)$$

ADVANCE INFORMATION

Typical Application (continued)

The engineer can use a polynomial equation or a LUT to extract the temperature reading based on the ADC code read in the microcontroller.

The cancellation of V_{BIAS} is one benefit to using a voltage-divider (ratiometric approach), but the sensitivity of the output voltage of the divider circuit cannot increase much. Therefore, not all of the ADC codes will be used due to the small voltage output range compared to the FSR. This application is very common, however, and is simple to implement.

The engineer can use a current source-based circuit, like the one shown in Figure 4, to have better control over the sensitivity of the output voltage and achieve higher accuracy. In this case, the output voltage is simply V = I × R. For example, if a current source of 40 µA is used with the TMP63, the output voltage will span approximately 5.5 V and will have a gain up to 40 mV/°C. Having control over the voltage range and sensitivity allows for full utilization of the ADC codes and full-scale range. Based on the bias current, the temperature voltage is shown in Figure 5. Similar to the ratiometric approach above, if the ADC has a built-in current source that shares the same bias as the reference voltage of the ADC, the tolerance of the supply current cancels out. In this case, a precision ADC is not required. This method yields the best accuracy, but can increase the system implementation cost.

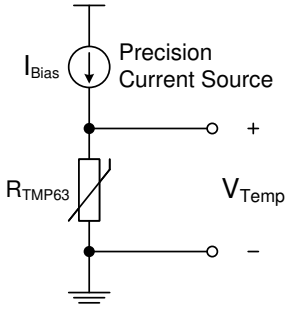


Figure 4. TMP63 Biasing Circuit With Current Source

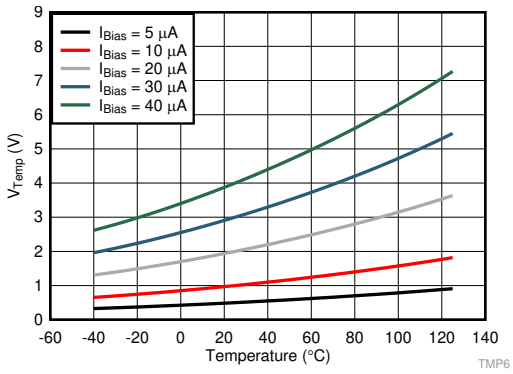


Figure 5. TMP63 Temperature Voltage With Varying Current Sources

In comparison to the non-linear NTC thermistor in a voltage divider, the TMP63 has an enhanced linear output characteristic. The two voltage divider circuits with and without a linearization parallel resistor, R_P, are shown in Figure 6. Consider an example where V_{BIAS} = 5 V, R_{BIAS} = 10 kΩ, and a parallel resistor (R_P) is used with the NTC thermistor (R_{NTC}) to linearize the output voltage with an additional 10-kΩ resistor. The TMP63 produces a linear curve across the entire temperature range while the NTC curve is only linear across a small temperature region. When the parallel resistor (R_P) is added to the NTC circuit, the added resistor makes the curve much more linear but greatly affects the output voltage range.

ADVANCE INFORMATION

Typical Application (continued)

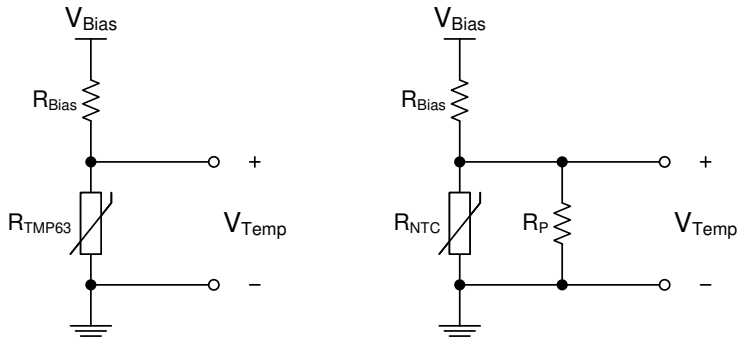


Figure 6. TMP63 vs. NTC With Linearization Resistor (R_P) Voltage Divider Circuits

8.2.1.2.1 Thermal Protection With Comparator

The engineer can use the TMP63, a voltage reference, and a comparator to program the thermal protection. As shown in Figure 7, the output of the comparator will remain low until the voltage of the thermistor divider, with R_{BIAS} and R_{TMP63}, rises above the threshold voltage set by R_1 and R_2. When the output goes high, the comparator signals an overtemperature warning signal. The engineer can also program the hysteresis to prevent the output from continuously toggling around the temperature threshold when the output returns low. Either a comparator with built-in hysteresis or feedback resistors may be used.

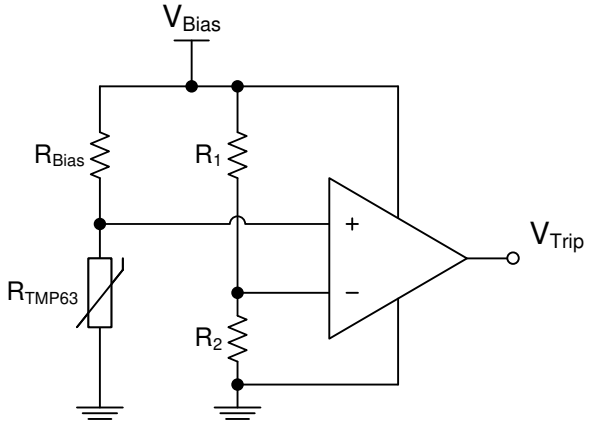


Figure 7. Temperature Switch Using TMP63 Voltage Divider and a Comparator

8.2.1.2.2 Thermal Foldback

One application that uses the output voltage of the TMP63 in an active control circuit is thermal foldback. This is performed to reduce, or fold back, the current driving a string of LEDs, for example. At high temperatures, the LEDs begin to heat up due to environmental conditions and self heating. Thus, at a certain temperature threshold based on the LED's safe operating area, the driving current must be reduced to cool down the LEDs and prevent thermal runaway. The TMP63 voltage output increases with temperature when the output is in the lower position of the voltage divider and can provide a response used to fold back the current. Typically, the current is held at a specified level until a high temperature is reached, known as the knee point, where the current must be rapidly reduced. To better control the temperature/voltage sensitivity of the TMP63, a rail-to-rail operational amplifier is used. In the example shown in Figure 8, the temperature “knee” where the foldback begins is set by the reference voltage (2.5 V) at the positive input, and the feedback resistors set the response of the foldback curve. The foldback knee point may be chosen based on the output of the voltage divider and the corresponding temperature from Equation 5 (like 110°C, for example). A buffer is used in-between the voltage divider with R_{TMP63} and the input to the op amp to prevent loading and variations in V_{TEMP}.

ADVANCE INFORMATION

Typical Application (continued)

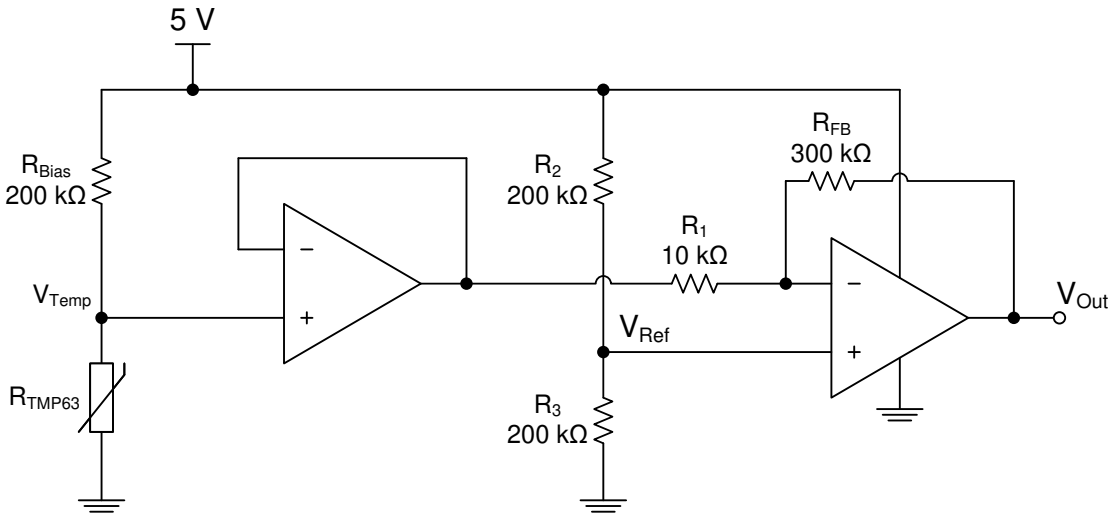


Figure 8. Thermal Foldback Using TMP63 Voltage Divider and a Rail-to-Rail Op Amp

The op amp will remain high as long as the voltage output is below V_{Ref}. When the temperature goes above 110°C, then the output will swing low to the 0-V rail of the op amp. The rate at which the foldback occurs is dependent on the feedback network, R_{FB} and R_1, which varies the gain of the op amp, G, given by Equation 6. This in return controls the voltage/temperature sensitivity of the circuit. This voltage output is fed into a LED driver IC that will adjust output current accordingly. The final output voltage used for thermal foldback is V_{OUT}, and is given in Equation 7. In this example where the knee point is set at 110°C, the output voltage curve is as shown in Figure 9.

$$V_{Temp} = V_{Bias} * \left(\frac{R_{TMP63}}{R_{Bias} + R_{TMP63}} \right) \quad (5)$$

$$G = \frac{R_{FB}}{R_1} \quad (6)$$

$$V_{Out} = -G * V_{Temp} + (1 + G) * V_{Ref} \quad (7)$$

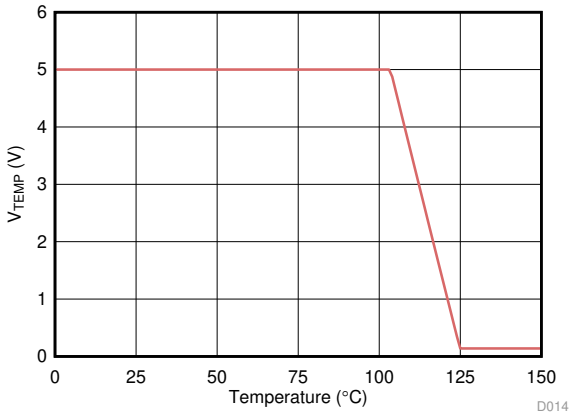


Figure 9. Thermal Foldback Voltage Output Curve

ADVANCE INFORMATION

9 Power Supply Recommendations

The maximum recommended operating voltage of the TMP63 is 5.5 V (V_{Sns}), and the maximum current through the device is 400 µA (I_{Sns}).

10 Layout

10.1 Layout Guidelines

The layout of the TMP63 is similar to that of a passive component. If the device is biased with a current source, the positive pin 2 is connected to the source, while the negative pin 1 is connected to ground. If the circuit is biased with a voltage source, and the device is placed on the lower side of the resistor divider, V– is connected to ground, and V+ is connected to the output (V_{TEMP}). If the device is placed on the upper side of the divider, V+ is connected to the voltage source and V– is connected to the output voltage (V_{TEMP}). Figure 10 shows the device layout.

10.2 Layout Example

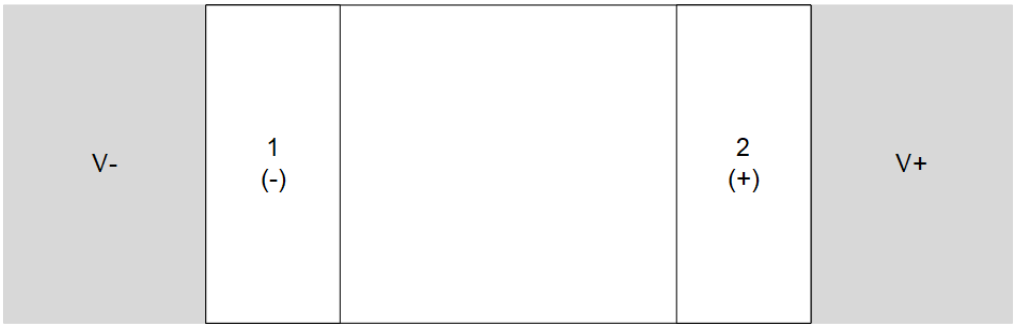


Figure 10. Recommended Layout: DEC Package

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP6331DECR	ACTIVE	X1SON	DEC	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC	Samples
TMP6331DECT	ACTIVE	X1SON	DEC	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC	Samples
TMP6331DYAR	ACTIVE	SOT-5X3	DYA	2	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	1HG	Samples
TMP6331DYAT	ACTIVE	SOT-5X3	DYA	2	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	1HG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

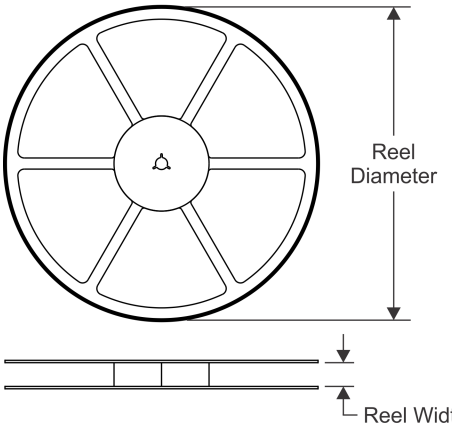
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

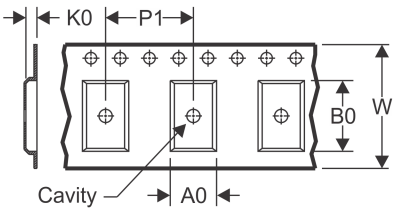
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

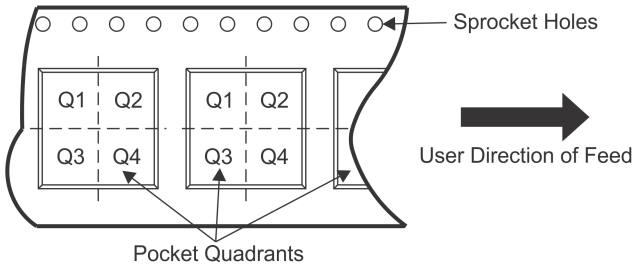


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

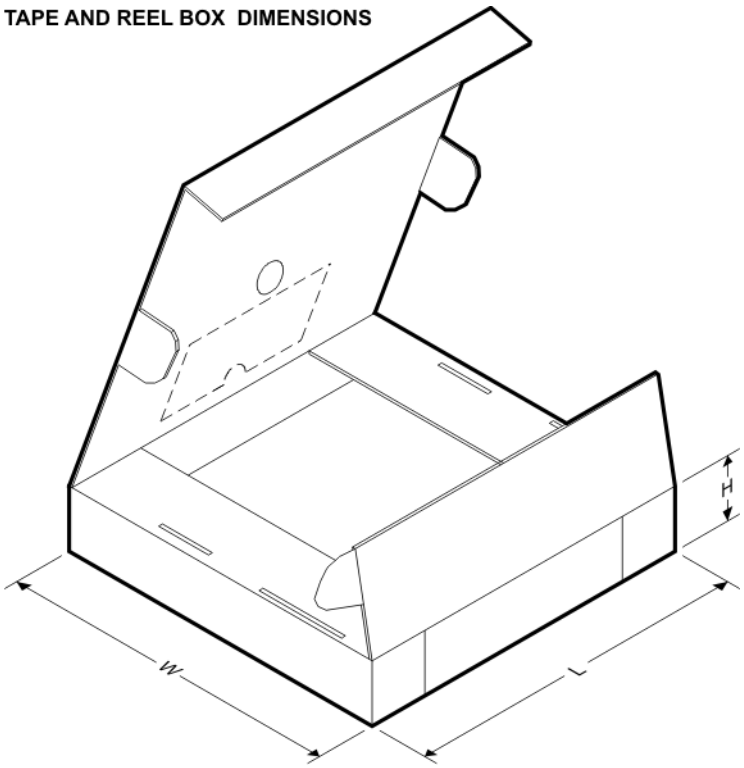
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP6331DECR	X1SON	DEC	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TMP6331DECT	X1SON	DEC	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

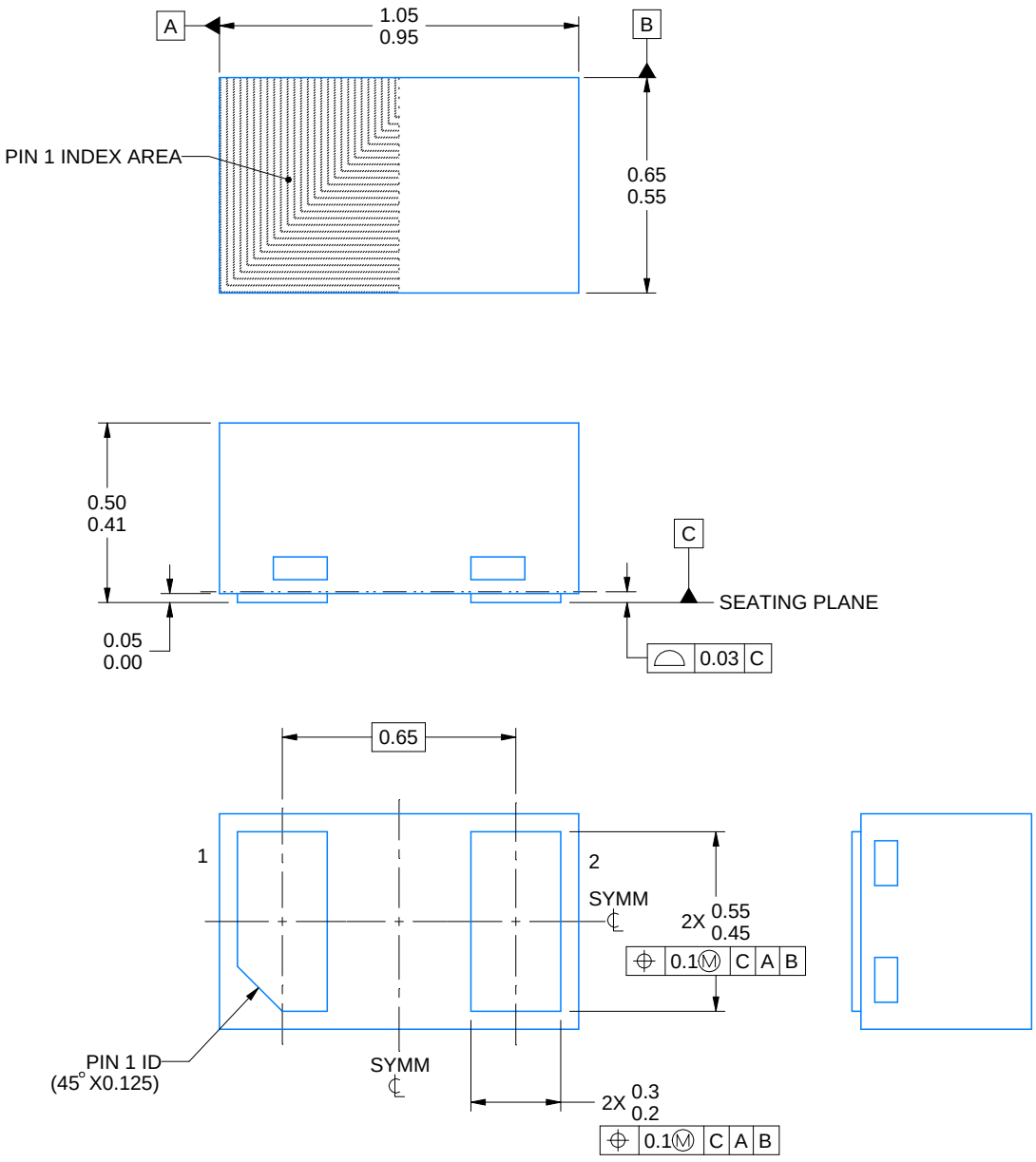
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP6331DECR	X1SON	DEC	2	10000	205.0	200.0	33.0
TMP6331DECT	X1SON	DEC	2	250	205.0	200.0	33.0

PACKAGE OUTLINE

DEC0002A

X1SON - 0.5 mm max height

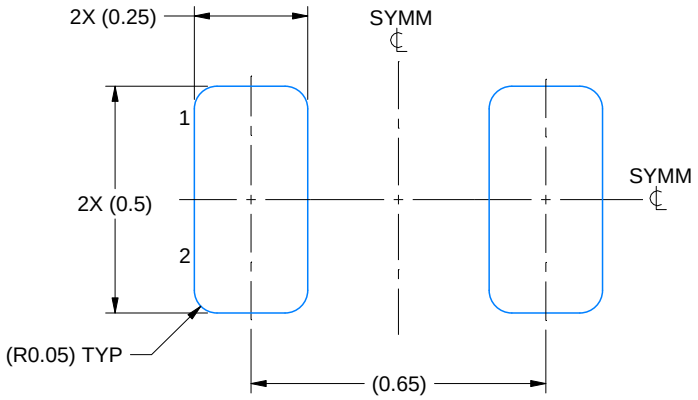
PLASTIC SMALL OUTLINE - NO LEAD



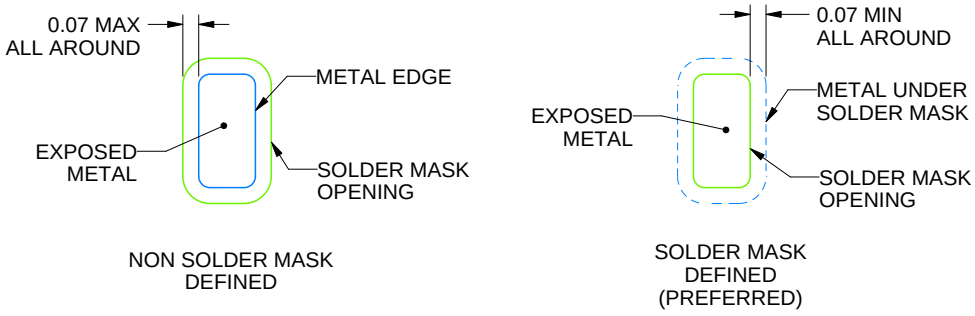
4224506/A 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

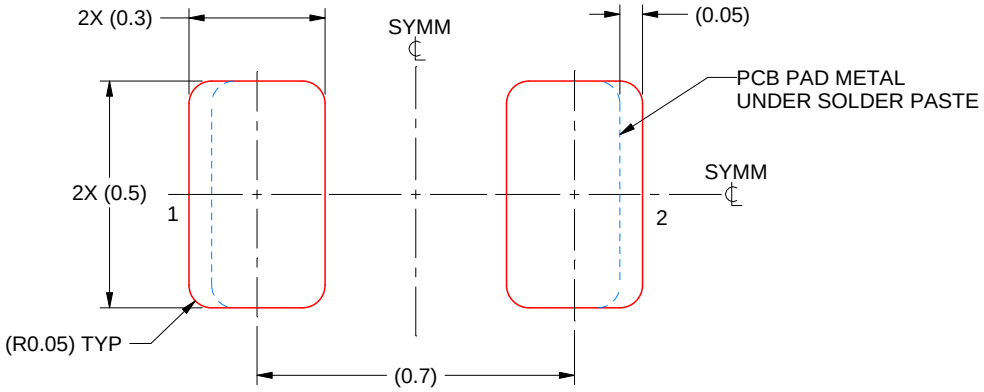


SOLDER MASK DETAILS

4224506/A 08/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224506/A 08/2018

NOTES: (continued)

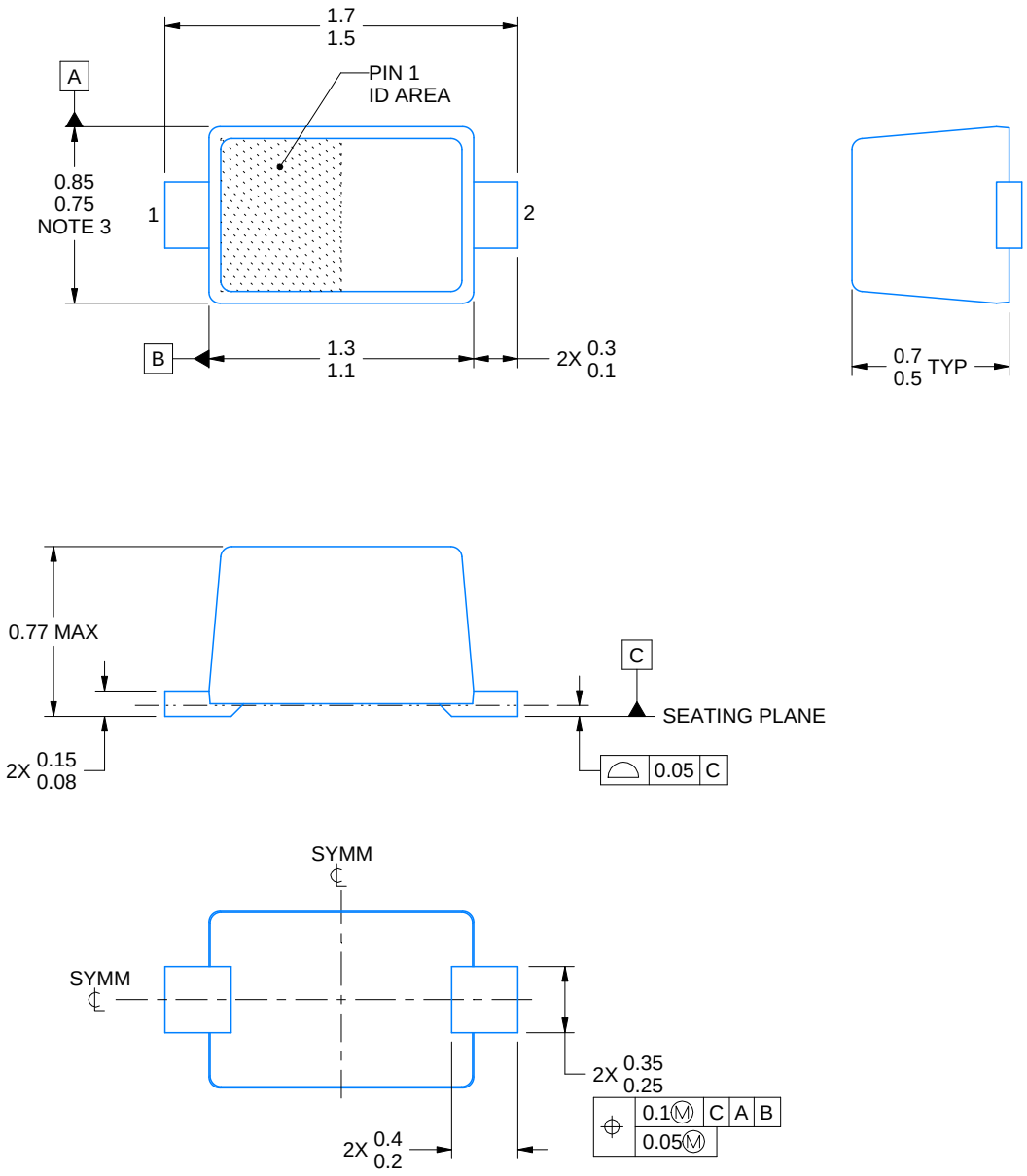
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

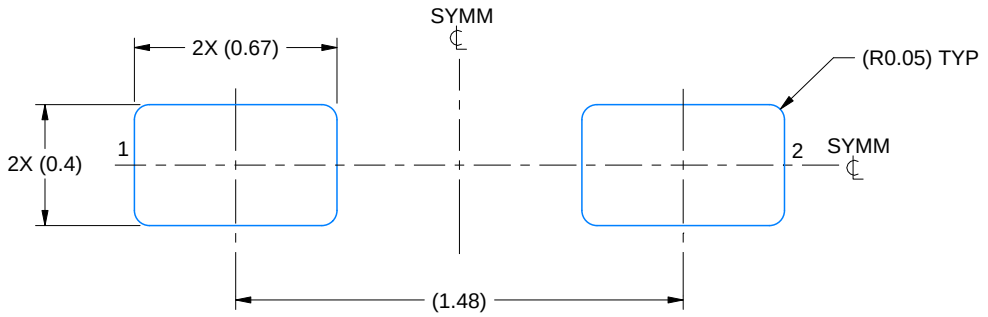
PLASTIC SMALL OUTLINE



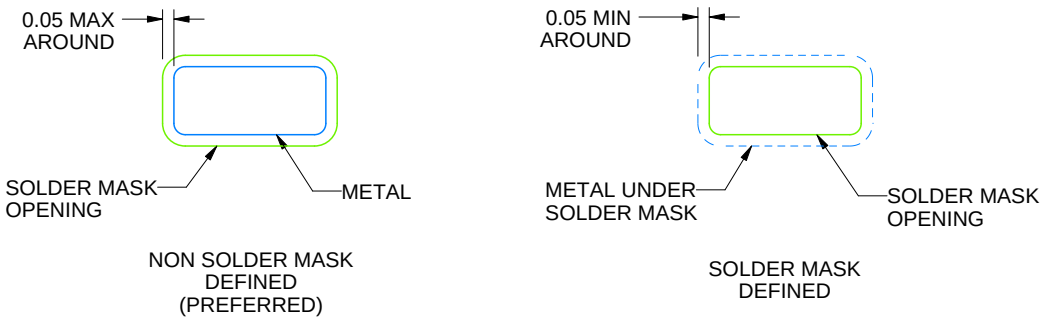
4224978/B 09/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X



SOLDERMASK DETAILS

4224978/B 09/2021

NOTES: (continued)

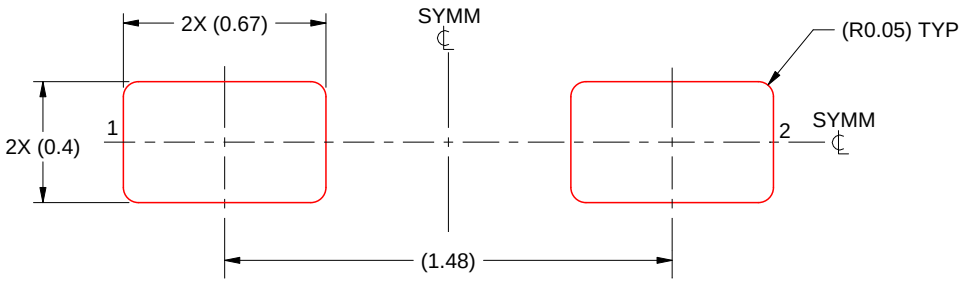
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/B 09/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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