

适用于 USB Type-C 和 HDMI 2.0 的 TPD4E02B04-Q1 4 通道 ESD 保护二极管

1 特性

- 符合 AEC-Q101
- IEC 61000-4-2 4 级 ESD 保护
 - $\pm 12\text{kV}$ 接触放电
 - $\pm 15\text{kV}$ 气隙放电
- ISO 10605 (330pF , 330Ω) ESD 保护
 - $\pm 10\text{kV}$ 接触放电
 - $\pm 10\text{kV}$ 气隙放电
- IEC 61000-4-4 瞬态放电 (EFT) 保护
 - 80A (5/50ns)
- IEC 61000-4-5 浪涌保护
 - 2A (8/20 μs)
- IO 电容:
 - 0.25pF (典型值)
- 直流击穿电压: 5.5V (最小值)
- 超低泄漏电流: 10nA (最大值)
- 低 ESD 钳位电压: 8.8V (5A TLP)
- 支持速率高达 10Gbps 的高速接口
- 工业温度范围: -40°C 至 $+125^\circ\text{C}$
- 简易直通布线封装

2 应用

- 终端设备
 - 音响主机
 - 后座娱乐系统
 - 远程信息处理
 - USB 集线器
 - 仪表组
 - 车身控制模块
 - 媒体接口
- 接口
 - USB Type-C
 - USB 3.1 第 2 代
 - 高清多媒体接口 (HDMI) 2.0/1.4
 - USB 3.0
 - DisplayPort 1.3
 - 10/100/1000Mbps 以太网

3 说明

TPD4E02B04-Q1 是一种经过汽车认证的双向 TVS ESD 保护二极管阵列，用于 USB Type-C 和 HDMI 2.0 电路保护。TPD4E02B04-Q1 的额定 ESD 冲击消散值高达 10kV ，符合 ISO

10605 (330pF , 330Ω) ESD 标准。TPD4E02B04 的额定 ESD 冲击消散值也达到了 IEC 61000-4-2 国际标准 (4 级) 中规定的最高水平。

该器件的每个通道均具有一个 0.25pF IO 电容，适用于保护速率高达 10Gbps 的高速接口 (例如第 2 代 USB 3.1)。低动态电阻和低钳位电压确保系统级抗瞬变事件保护。

TPD4E02B04-Q1 采用符合行业标准的 USON-10 (DQA) 封装。该封装采用直通布线，其引脚间距为 0.5mm ，能够简化实现并缩短设计时间。

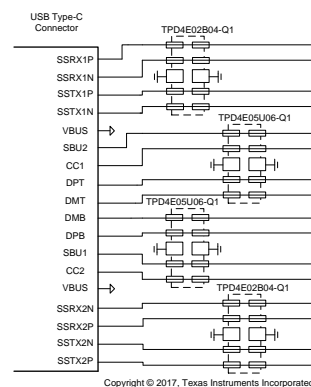
该器件还具有未经过汽车认证的型号：[TPD4E02B04](#)。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPD4E02B04-Q1	USON (10)	2.50mm x 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图



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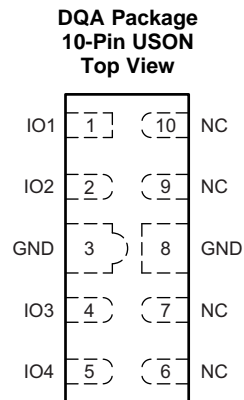
4 修订历史记录

Changes from Original (June 2017) to Revision A

Page

•	首次公开发布数据表	1
•	已更改 将 ISO 气隙额定值更改成了 10kV	1
•	已更改 将接触额定值更改成了 10kV	1
•	已更改 将接口以太网更改成了 10/100/1000Mbps	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground
GND	8		
IO1	1	I/O	ESD protected channel
IO2	2		
IO3	4		
IO4	5		
NC	6	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	7		
NC	9		
NC	10		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power ($t_p - 8/20 \mu\text{s}$) at 25°C		17	W
	IEC 61000-4-5 Ccurrent ($t_p - 8/20 \mu\text{s}$) at 25°C		2	A
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—AEC Specification

		VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2500
		Charged-device model (CDM), per AEC Q100-011	±1000

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

		VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±12000
		IEC 61000-4-2 air-gap discharge	±15000

6.4 ESD Ratings—ISO Specification

		VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge	ISO 10605 330 pF, 330 Ω , IO	±10000
		Contact discharge	±10000
		Air-gap discharge	±10000

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	-3.6	3.6	V
T_A	Operating free-air temperature	-40	125	°C

6.6 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD4E02B04-Q1	UNIT
		DQA (USON)	
		10 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	348.7	°C/W
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	214.1	°C/W
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	270.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	81.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	270.7	°C/W
$R_{\theta\text{JC(bot)}}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 10 nA	-3.6		3.6	V
V _{BRF}	Breakdown voltage, any IO pin to GND ⁽¹⁾	I _{IO} = 1 mA, T _A = 25°C	5.5	6.4	7.5	V
V _{BRR}	Breakdown voltage, GND to any IO pin ⁽¹⁾	I _{IO} = 1 mA, T _A = 25°C	-5.5	-6.4	-7.5	V
V _{HOLD}	Holding voltage ⁽²⁾	I _{IO} = 1 mA		5.8		V
V _{CLAMP}	Clamping voltage	I _{PP} = 1 A, TLP, from IO to GND		6.6		V
		I _{PP} = 5 A, TLP, from IO to GND		8.8		
		I _{PP} = 1 A, TLP, from GND to IO		6.6		
		I _{PP} = 5 A, TLP, from GND to IO		8.8		
I _{LEAK}	Leakage current, any IO to GND	V _{IO} = ±2.5 V			10	nA
R _{DYN}	Dynamic resistance	IO to GND		0.47		Ω
		GND to IO		0.47		
C _L	Line capacitance	V _{IO} = 0 V, f = 1 MHz, IO to GND, T _A = 25°C		0.25	0.33	pF
ΔC _L	Variation of line capacitance	Delta of capacitance between any two IO pins, V _{IO} = 0 V, f = 1 MHz, T _A = 25°C, GND = 0 V		0.01	0.07	pF
C _{CROSS}	Channel to channel capacitance	Capacitance from one IO to another, V _{IO} = 0 V, f = 1 MHz, GND = 0 V		0.13	0.16	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when 1 mA is applied in the positive-going direction, before the device latches into the snapback state.

(2) V_{HOLD} is defined as the voltage when 1 mA is applied in the negative-going direction, after the device has successfully latched into the snapback state.

6.8 Typical Characteristics

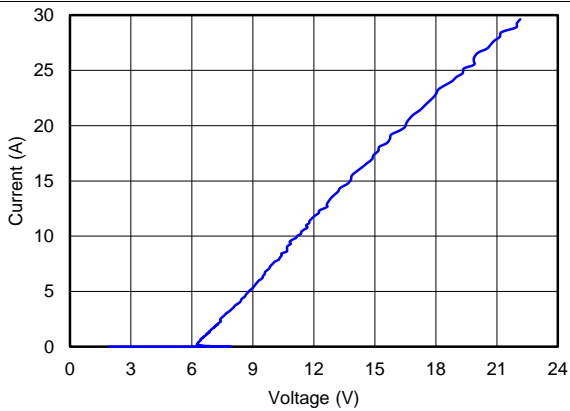


图 1. Positive TLP Curve

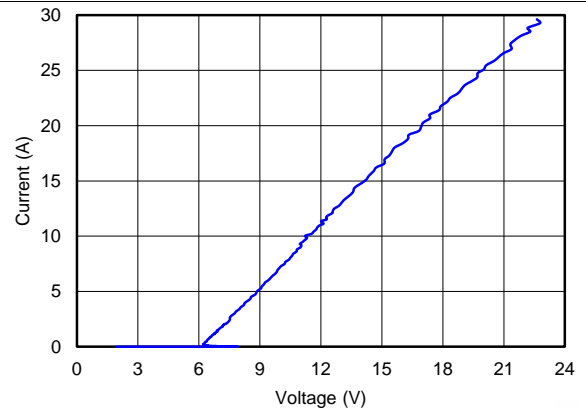


图 2. Negative TLP Curve

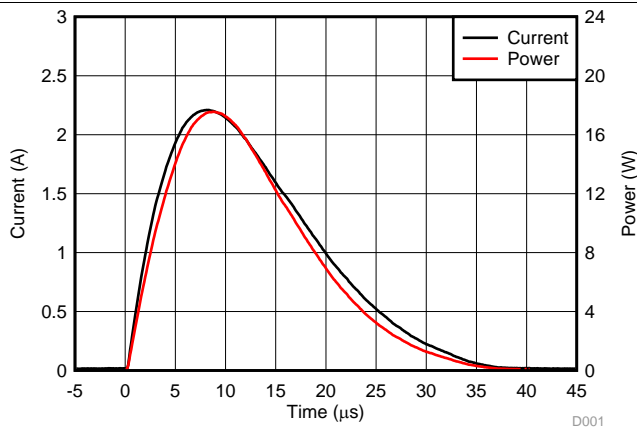


图 3. Surge Curve ($t_p = 8/20 \mu s$), any IO pin to GND

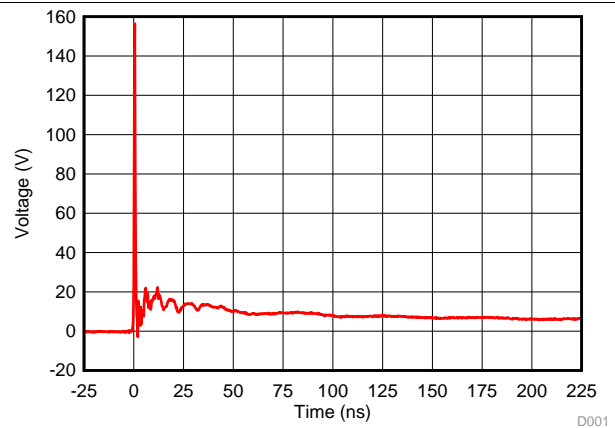


图 4. 8-kV IEC Waveform

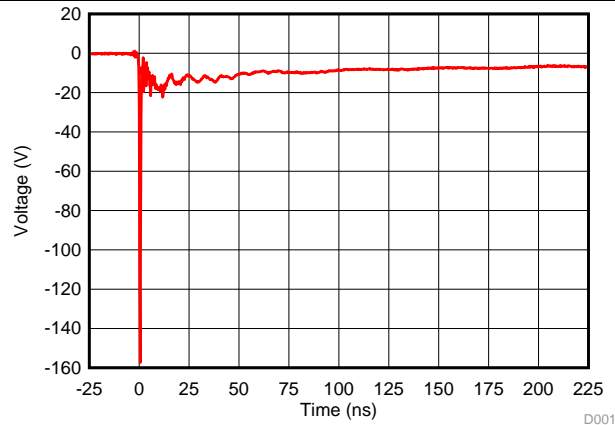


图 5. -8-kV IEC Waveform

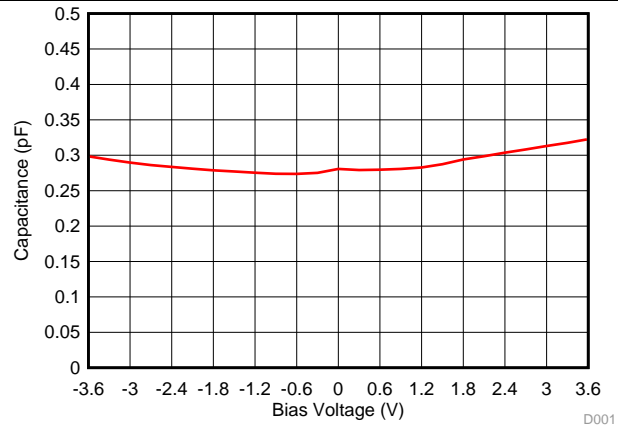
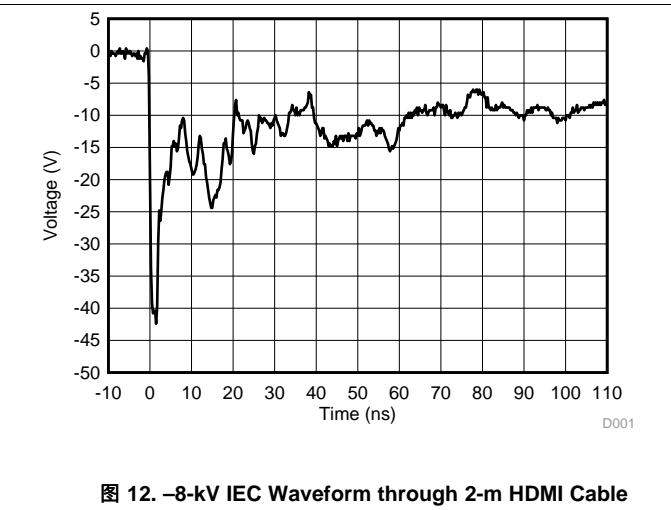
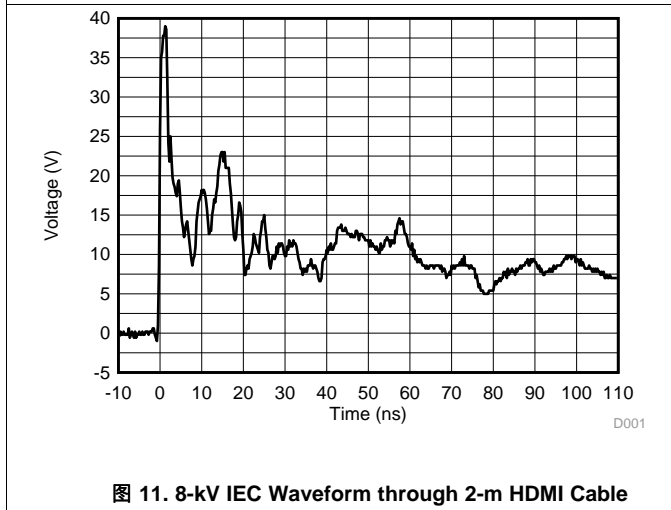
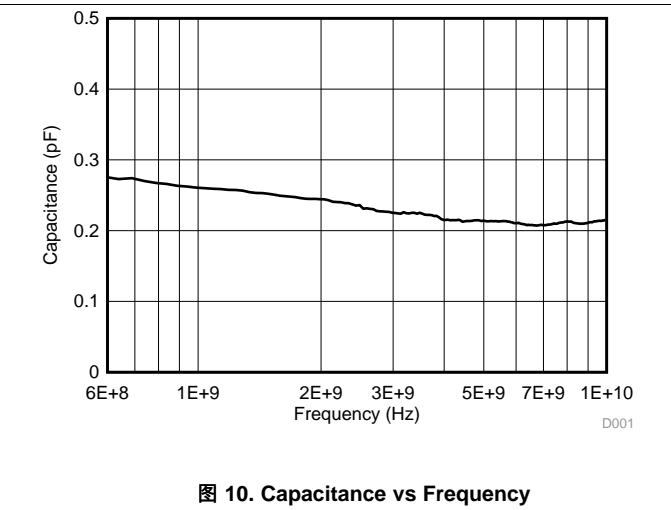
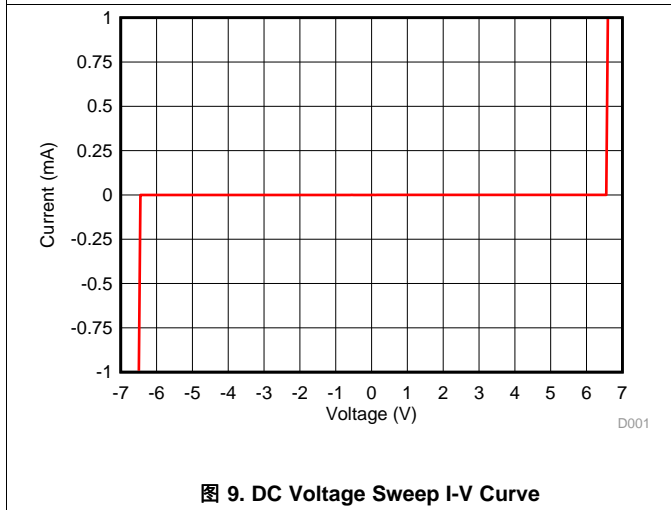
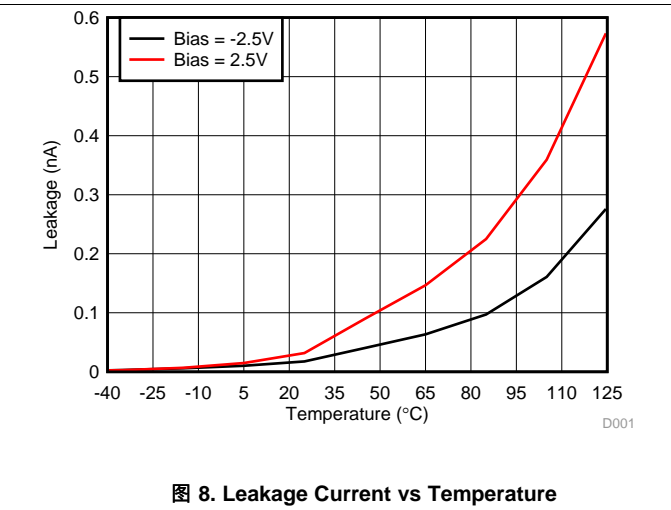
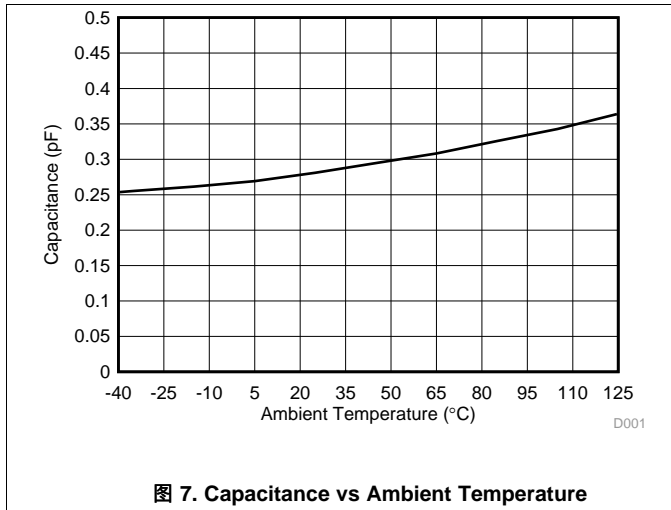


图 6. Capacitance vs Bias Voltage

Typical Characteristics (接下页)



Typical Characteristics (接下页)

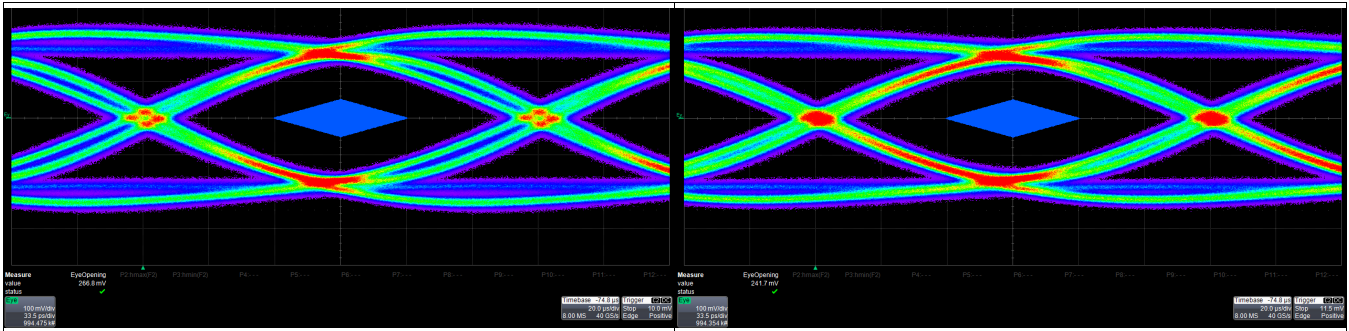


图 13. USB3.0 Eye Diagram (Bare Board)

图 14. USB3.0 Eye Diagram (With TPD4E02B04-Q1)

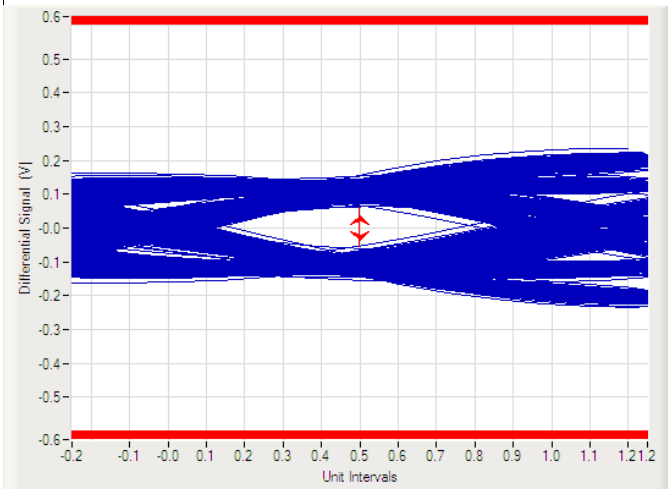


图 15. USB3.1 Gen 2 Eye Diagram (Bare Board)

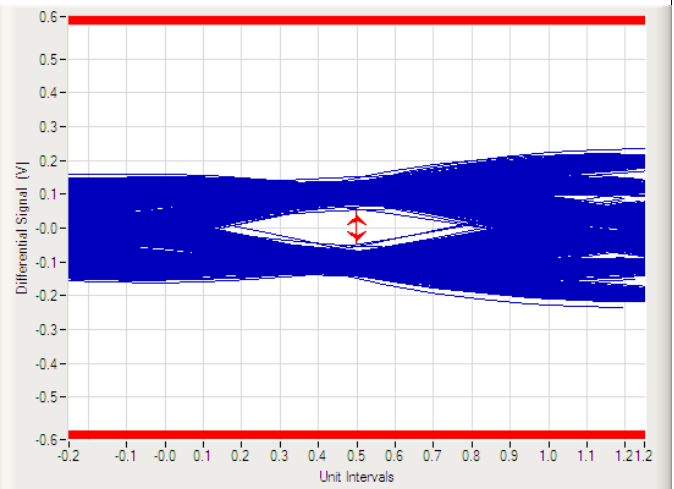


图 16. USB3.1 Gen 2 Eye Diagram (With TPD4E02B04-Q1)

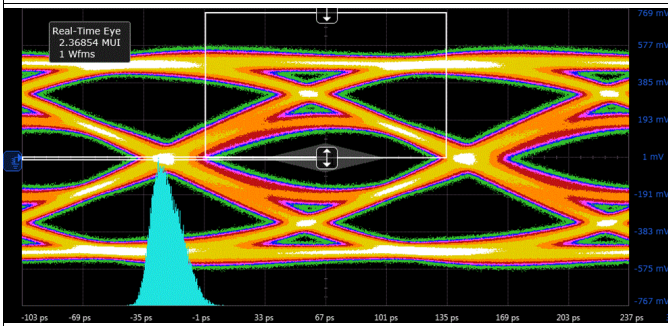


图 17. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

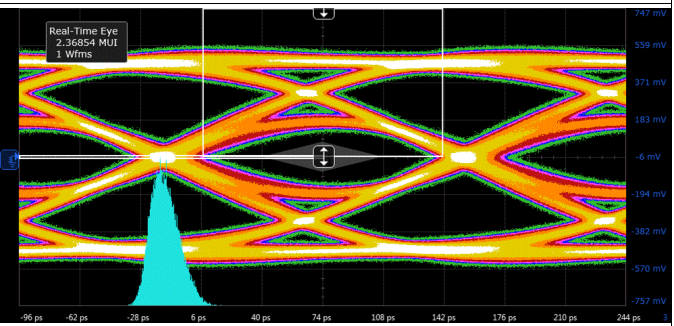


图 18. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD4E02B04-Q1)

Typical Characteristics (接下页)

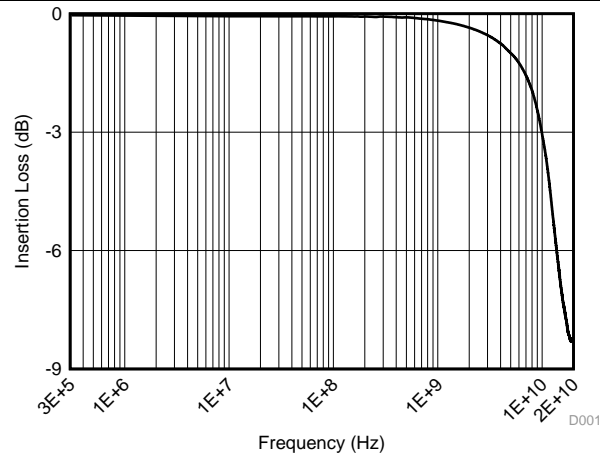


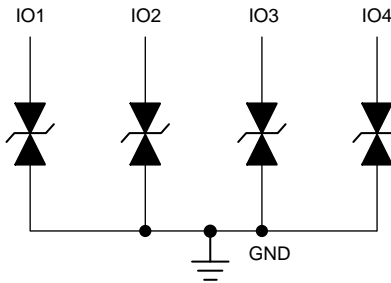
图 19. Differential Insertion Loss

7 Detailed Description

7.1 Overview

The TPD4E02B04-Q1 is an automotive-qualified bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 (Level 4) International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards and is qualified to operate from -40°C to $+125^{\circ}\text{C}$.

7.3.2 ISO 10605 ESD Protection

The I/O pins can withstand ESD events of at least $\pm 10\text{-kV}$ contact and $\pm 10\text{-kV}$ air gap according to the ISO 10605 (330 pF, 330 Ω) standard. The device diverts the current to ground.

7.3.3 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to $\pm 12\text{-kV}$ contact and $\pm 15\text{-kV}$ air gap. An ESD-surge clamp diverts the current to ground.

7.3.4 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50- Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.5 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2 A and 17 W (8/20 μs waveform). An ESD-surge clamp diverts this current to ground.

7.3.6 IO Capacitance

The capacitance between each I/O pin to ground is 0.25 pF (typical). This device supports data rates up to 10 Gbps.

7.3.7 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of $\pm 5.5\text{ V}$. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of $\pm 3.6\text{ V}$.

7.3.8 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of $\pm 2.5\text{ V}$.

Feature Description (接下页)

7.3.9 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.8 V ($I_{PP} = 5$ A).

7.3.10 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 10 Gbps, because of the extremely low IO capacitance.

7.3.11 Industrial Temperature Range

This device features an industrial operating range of -40°C to $+125^{\circ}\text{C}$.

7.3.12 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD4E02B04-Q1 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR} . During ESD events, voltages as high as ± 15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of the TPD4E02B04-Q1 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

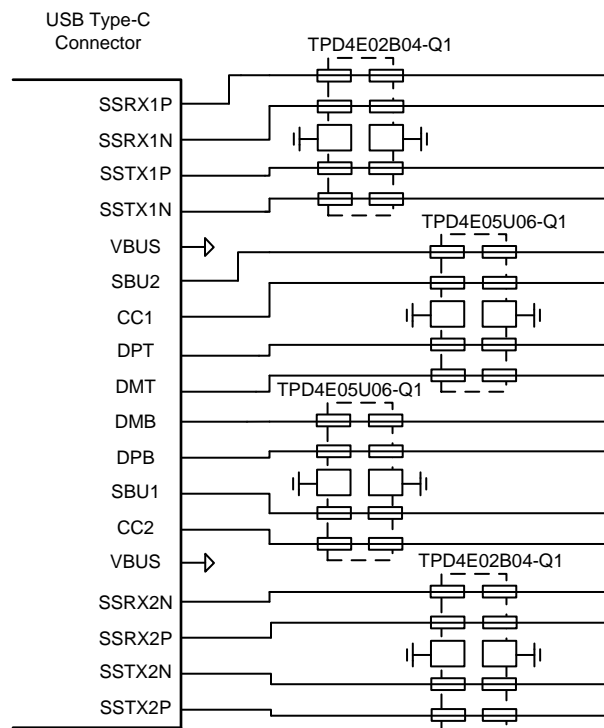
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E02B04-Q1 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

8.2 Typical Application



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图 20. USB 3.1 Gen 2 Type-C ESD Schematic

Typical Application (接下页)

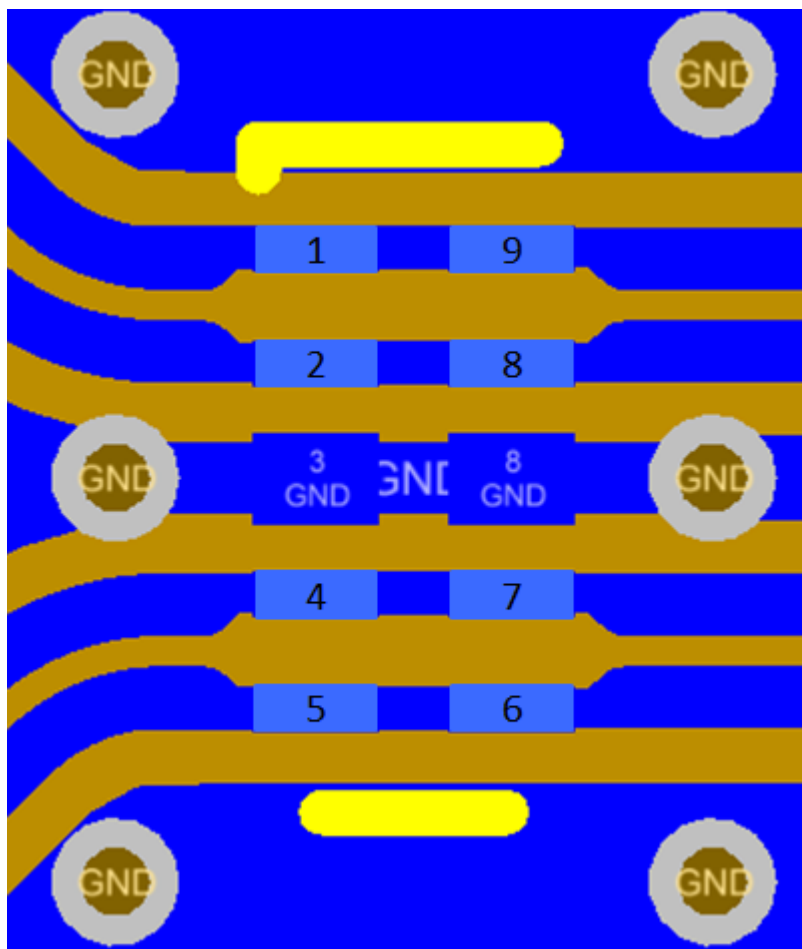


图 21. USB 3.1 Gen 2 SuperSpeed Layout

8.2.1 Design Requirements

For this design example two TPD4E02B04-Q1 devices and two TPD4E05U06 devices are being used in a USB 3.1 Gen 2 Type-C application. This provides a complete ESD protection scheme.

Given the USB 3.1 Gen 2 Type-C application, the parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal Range on SuperSpeed+ Lines	0 V to 3.6 V
Operating Frequency on SuperSpeed+ Lines	5 GHz
Signal Range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating Frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD4E02B04-Q1 supports signal ranges between -3.6 V and 3.6 V, which supports the SuperSpeed+ pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP/DM lines.

8.2.2.2 Operating Frequency

The TPD4E02B04-Q1 has a 0.25 pF (typical) capacitance, which supports the USB3.1 Gen 2 data rates of 10 Gbps. The TPD4E05U06 has a 0.5 pF (typical) capacitance, which easily supports the CC, SBU, and DP/DM data rates.

8.2.3 Application Curves

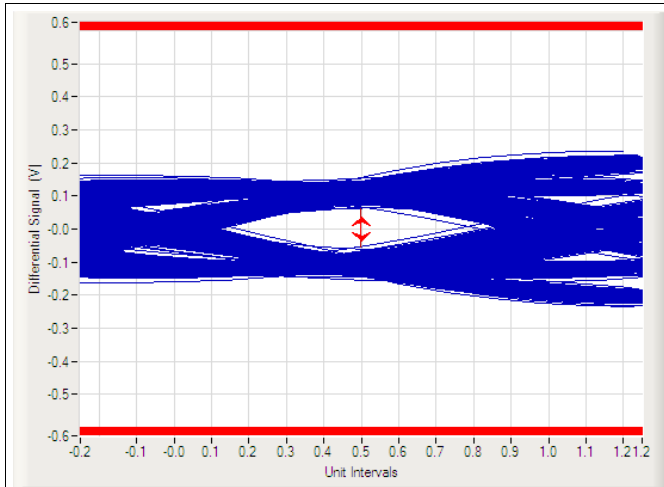


图 22. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

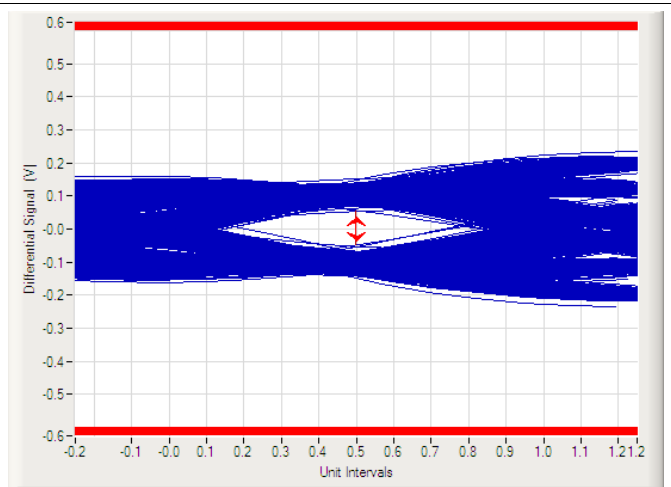


图 23. USB 3.1 Gen 2 10-Gbps Eye Diagram (With TPD4E02B04-Q1)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

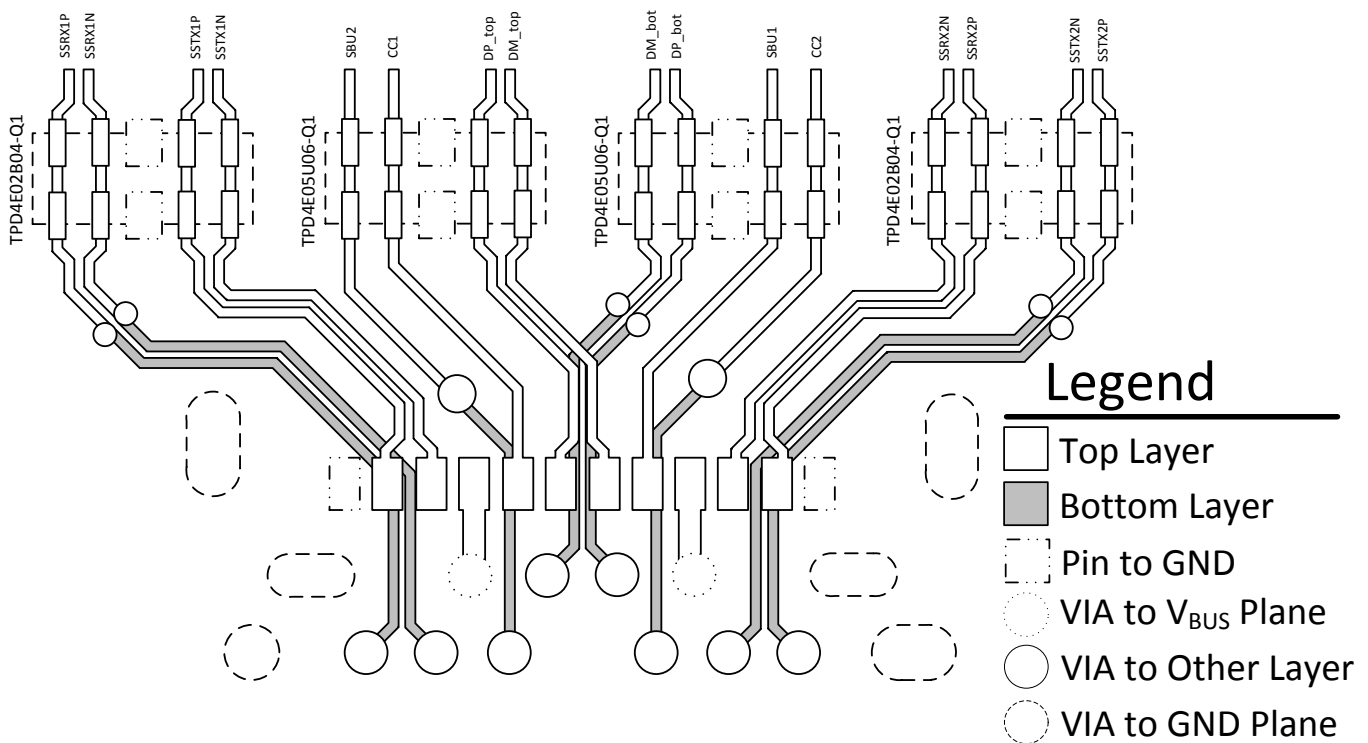







图 24. USB Type-C Mid-Mount, Hybrid Connector with One-Sided ESD Layout

Layout Examples (接下页)

- Legend**
-  Top Layer
 -  Bottom Layer
 -  Pin to GND
 -  VIA to Other Layer
 -  VIA to GND Plane

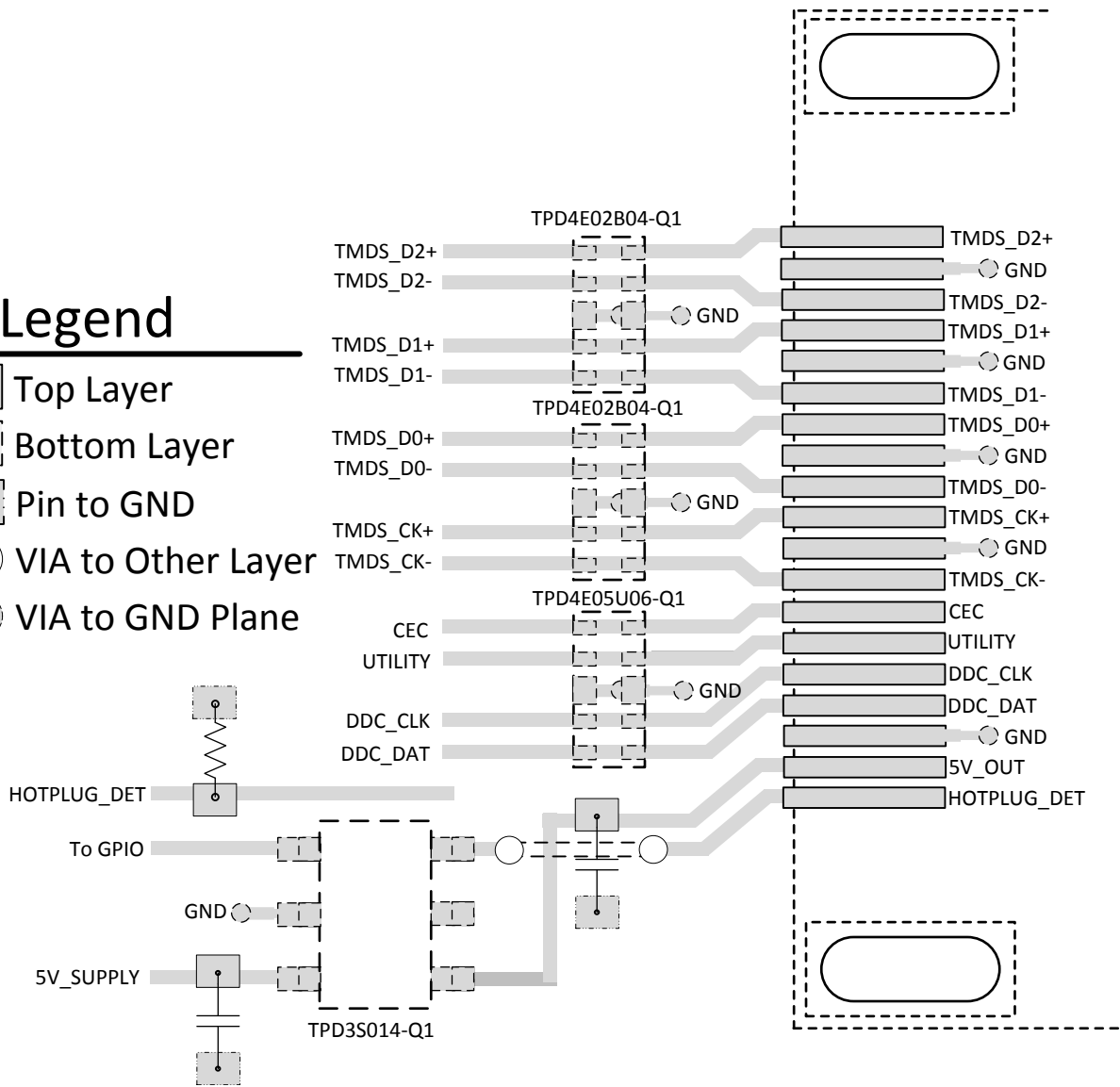


图 25. HDMI2.0 Type-A Transmitter Port Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档:

- 《阅读并理解 ESD 保护数据表》，[SLLA305](#)
- 《ESD 布局布线指南》，[SLVA680](#)
- 《为超高速数据线选择 ESD 二极管》，[SLVA785](#)
- 《TPD4E02B04EVM 用户指南》，[SLVUAH6](#)

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的通知我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.

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11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E02B04QDQARQ1	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E02B04QDQARQ1	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

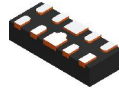
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E02B04QDQARQ1	USON	DQA	10	3000	189.0	185.0	36.0

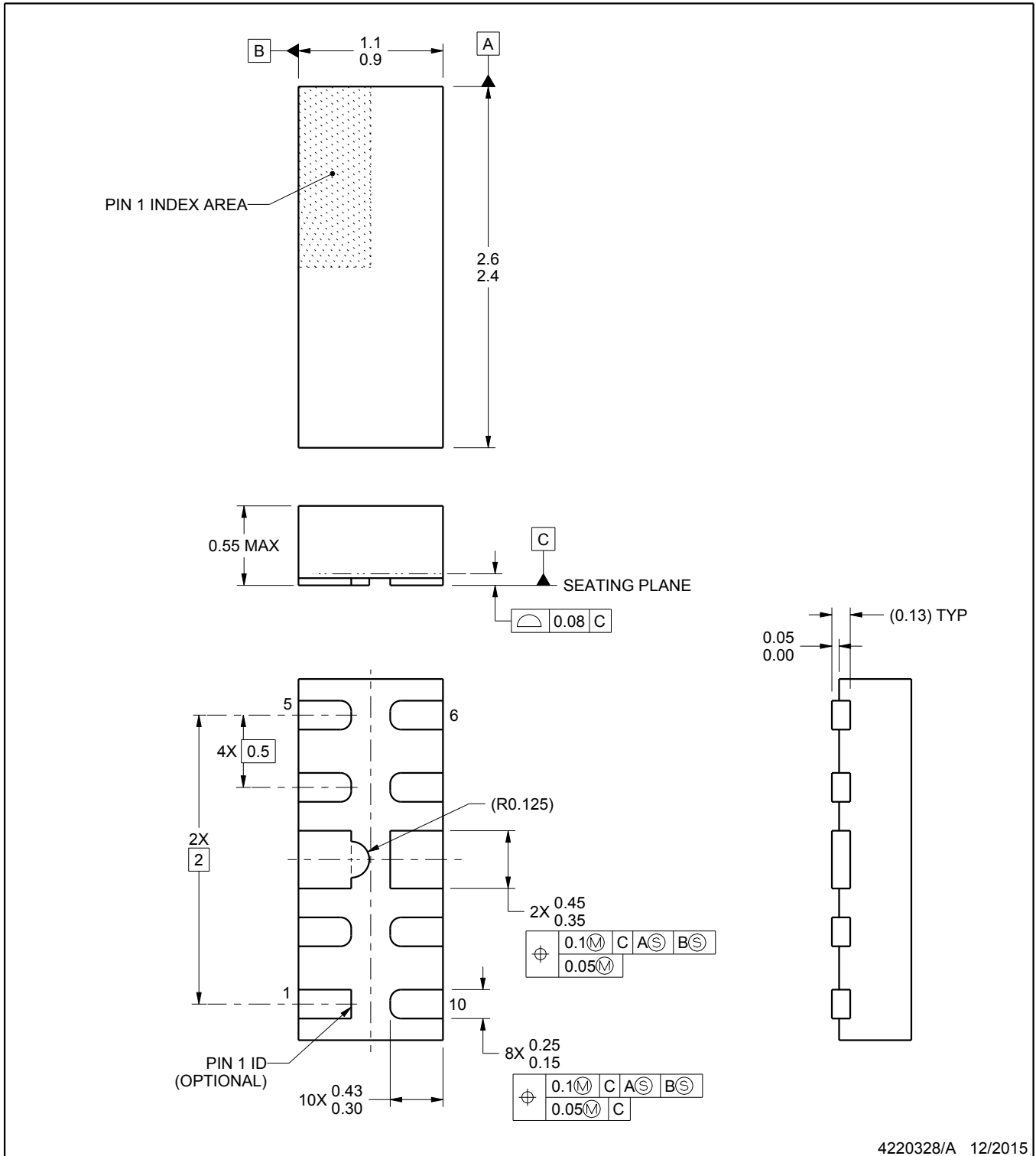
DQA0010A



PACKAGE OUTLINE

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220328/A 12/2015

NOTES:

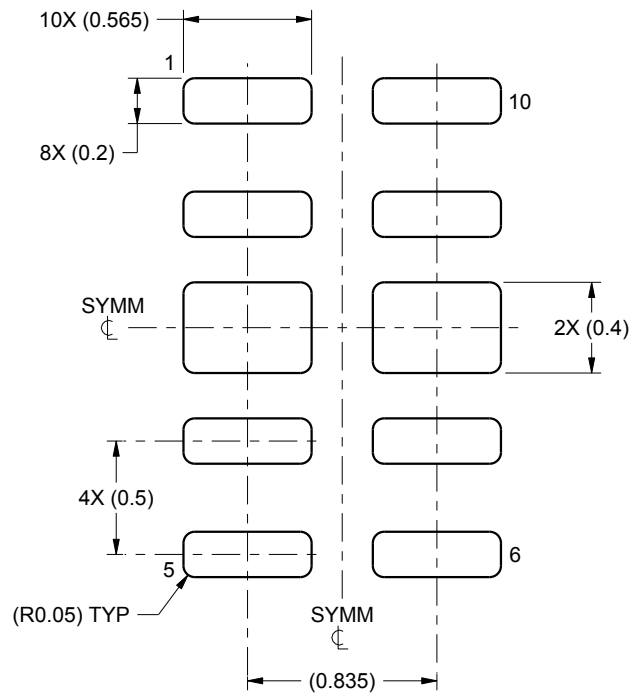
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

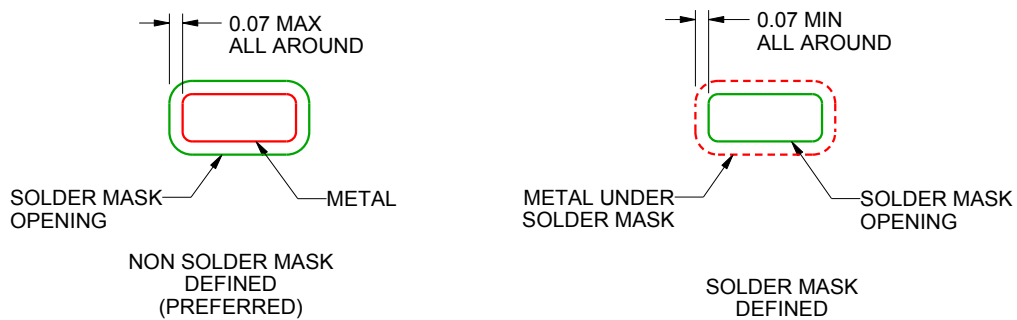
DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

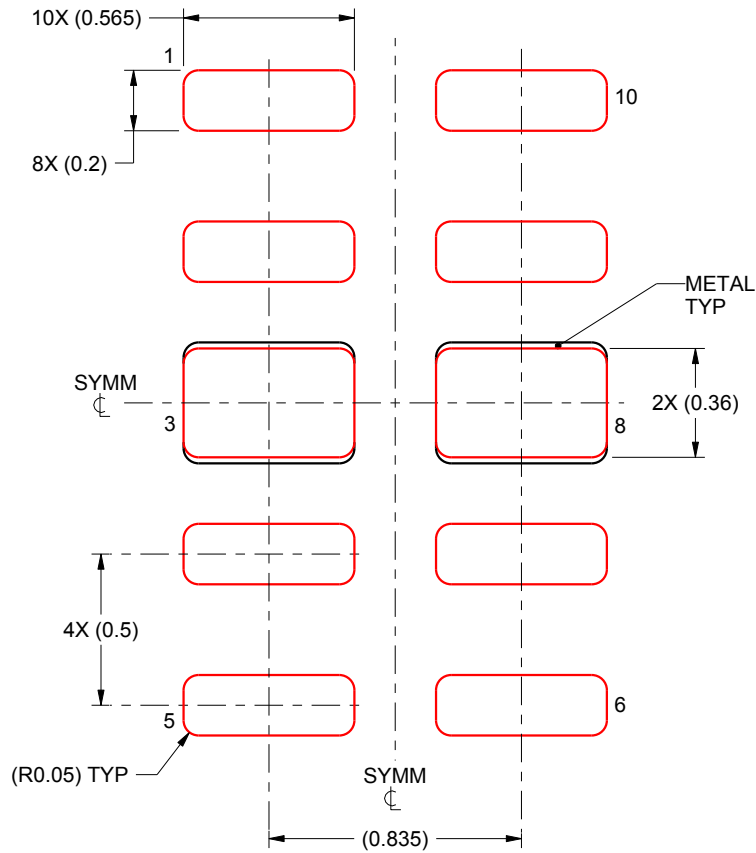
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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