

# 具有电平位移&可调转换率控制的 1.2V-8V, 3A 聚合物薄膜场效应晶体管 (PFET) 高侧负载开关

 查询样品: [TPS27081A](#)

## 特性

- 低导通电阻, 高电流 **PFET**
  - $V_{GS} = -4.5V$  时,  $R_{导通} = 32m\Omega$
  - $V_{GS} = -3.0V$  时,  $R_{导通} = 44m\Omega$
  - $V_{GS} = -1.8V$  时,  $R_{导通} = 82m\Omega$
  - $V_{GS} = -1.5V$  时,  $R_{导通} = 93m\Omega$
  - $V_{GS} = -1.2V$  时,  $R_{导通} = 155m\Omega$
- 通过外部 **R1**, **R2** 和 **C1** 实现的可调打开和关闭转换率控制
- 支持 **1.2V** 到高达 **8V** 的宽范围电源输入
- 用于 **PFET** 控制的集成 **NMOS**
- NMOS** 打开/关闭支持 **1.0V** 至高达 **8.0V** 的宽范围控制逻辑接口
- 完全静电放电 (**ESD**) 保护 (所有引脚)
  - 人体模型 (**HBM**) **2kV**, 充电器件模型 (**CDM**) **500V**
- 待机模式下的超低泄漏电流 (典型值 **100nA**)
- 采用微型 **6** 引脚封装
  - 2.9mm x 2.8mm x 0.75mm** 薄型小外形尺寸晶体管 (**SOT**)-**23** (**DDC**) 封装

## 应用范围

- 高侧负载开关
- 涌入电流控制
- 电源排序和控制
- 待机电源隔离
- 便携式电源开关

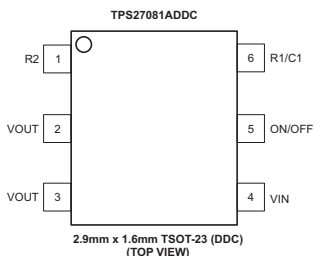


图 1. TPS27081A 封装

## 说明

TPS27081A 是一款高侧负载开关, 此开关在微封装内集成了一个功率 PFET 和一个控制 NMOS。

TPS27081A 在所有引脚上特有业界标准 ESD 保护, 从而提供与其它板载组件更好的 ESD 兼容性。

TPS27081A 可将开/关逻辑信号的电平转换为 VIN 电平, 并且支持低至 1.0V 的 CPU 或 MCU 逻辑以在不需要外部电平位移器的前提下控制更高电压的电源。

通过一个快速开/关逻辑信号来开启大值输出电容器有可能导致过多的涌入电流。为了控制负载涌入电流, 如图 2 所示, 连接一个电阻器 R2。可增加一个外部电容器 C1 来进一步限制涌入电流。要配置 TPS27081A 以获得一个特定的转换率, 请参考应用信息一节。

无需对涌入电流进行控制的待机电源开关应用需要一个单一上拉电阻器 R1。在此类应用中, 将 TPS27081A 引脚 R2 连接至系统接地。

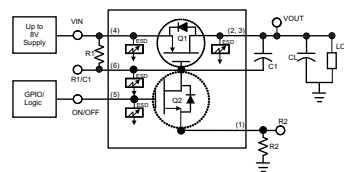


图 2. 简化方框图&amp;应用图

组件表 (典型应用)

组件	说明
R1	电平位移器/上拉电阻器
R2	可选 <sup>(1)</sup>
C1	可选 <sup>(1)</sup>

(1) 负载涌入电流 (转换率) 控制需要此选项



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	PART NUMBER	PACKAGE		TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	TPS27081ADDCR	6-Pin Thin SOT	Reel of 3000	AU_

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) DDC: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>**

Specified at T<sub>J</sub> = –40°C to 105°C unless otherwise noted.

	VALUE		UNIT
	MIN	MAX	
V <sub>INmax</sub> , V <sub>OUTmax</sub>	V <sub>IN</sub> , V <sub>OUT</sub> pin Maximum Voltage with reference to pin R2		V
V <sub>ON/OFF</sub>	ON/OFF Pin max Voltage with respect to Pin R2		V
I <sub>Q1-ON</sub>	Max Continuous Drain Current of Q1 at T <sub>J</sub> = 105°C		3
	Max Pulsed Drain Current of Q1 <sup>(3)</sup> at T <sub>J</sub> = 105°C		9.5
P <sub>D</sub>	Max power dissipation at T <sub>A</sub> = 25°C, T <sub>J</sub> = 150°C	6 Pin - TSOT, θ <sub>JA</sub> = 105°C/W	mW
All pins	ESD Rating – HBM		2000
	ESD Rating – CDM		500
T <sub>A</sub>	Operating free-air ambient temperature range		°C
T <sub>J-max</sub> <sup>(5)</sup>	Operating virtual junction temperature		°C
T <sub>stg</sub>	Storage temperature range		°C

- (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Refer to TI's design support web page at [www.ti.com/thermal](http://www.ti.com/thermal) for improving device thermal performance
- (3) Pulse Width <300us, Duty Cycle <2%
- (4) T<sub>J-max</sub> limits and other related conditions apply. Refer to SOA charts, [Figure 17](#) through [Figure 21](#)
- (5) Operating at the absolute T<sub>J-max</sub> of 150°C can affect reliability – for higher reliability it is recommended to ensure T<sub>J</sub> <105°C

**DISSIPATION RATINGS<sup>(1)(2)(3)</sup>**

BOARD	PACKAGE	θ <sub>JC</sub>	θ <sub>JA</sub> <sup>(4)</sup>	T <sub>A</sub> < 25°C	T <sub>A</sub> = 70°C	T <sub>A</sub> = 85°C	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C
High-K(JEDEC 51-7)	6-Pin Thin SOT (DDC)	43°C/W	105°C/W	1190 mW	760 mW	619 mW	9.55 mW/°C

- (1) Refer to TI's design support web page at [www.ti.com/thermal](http://www.ti.com/thermal) for improving device thermal performance.
- (2) Maximum dissipation values for retaining a maximum allowable device junction temperature of 150°C
- (3) Package thermal data based on a 76x114x1.6mm, 4-layer board with 2-oz Copper on outer layers
- (4) Operating at the absolute T<sub>J-max</sub> of 150°C can affect reliability; T<sub>J</sub> ≤ 105°C is recommended

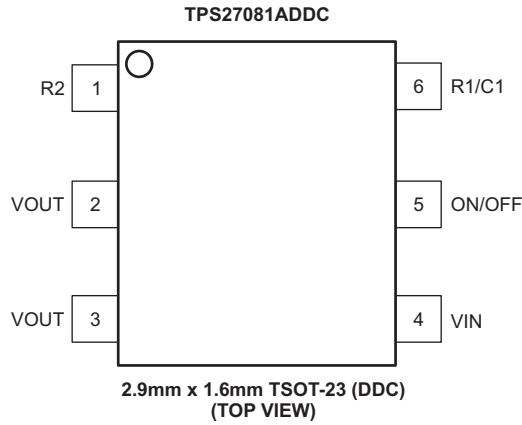
## ELECTRICAL CHARACTERISTICS

Specified over the recommended junction temperature range  $T_J = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$  unless otherwise noted. Typical values specified at  $T_A = T_J = 25^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>							
$BV_{IN}$	Q1 drain-to-source breakdown voltage	$V_{ON/OFF} = 0\text{ V}$ , $V_{GS}(Q1) = 0\text{ V}$ , $I_{D}(Q1) = 250\ \mu\text{A}$		-8			V
$I_{LOAD}^{(1)}$	VIN Pin total leakage current	$V_{IN} = 8\text{ V}$ , $V_{ON/OFF} = 0\text{ V}$ , $R1 = 10\text{ k}\Omega$	$T_J = 25^{\circ}\text{C}$	0.15	0.75		$\mu\text{A}$
			$T_J = 85^{\circ}\text{C}^{(2)}$	5	20		
$I_{LOAD}^{(1)}$	VIN Pin total leakage current	$V_{IN} = 5\text{ V}$ , $V_{ON/OFF} = 0\text{ V}$ , $R1 = 10\text{ k}\Omega$	$T_J = 25^{\circ}\text{C}$	0.05			$\mu\text{A}$
			$T_J = 85^{\circ}\text{C}^{(2)}$	2			
$I_{FQ2}$	Q2 drain-to-source leakage current	$V_{IN} = 8\text{ V}$ , $V_{ON/OFF} = 0\text{ V}$	$T_J = 25^{\circ}\text{C}$	0.030	0.050		$\mu\text{A}$
			$T_J = 85^{\circ}\text{C}^{(2)}$	0.350	0.600		
$I_{FQ2}$	Q2 drain-to-source leakage current	$V_{IN} = 5\text{ V}$ , $V_{ON/OFF} = 0\text{ V}$	$T_J = 25^{\circ}\text{C}$	0.025			$\mu\text{A}$
			$T_J = 85^{\circ}\text{C}^{(2)}$	0.250			
<b>ON CHARACTERISTICS<sup>(3)</sup></b>							
$V_{IL}$	ON/OFF pin low-level input voltage	$V_{IN} = 5.0\text{ V}$ , $I_{D}(Q1) < 2\ \mu\text{A}$ , $R1 = 10\text{ k}\Omega$ , $R2 = RL = 0\ \Omega$	$T_J = 25^{\circ}\text{C}$	0.3			V
			$T_J = 85^{\circ}\text{C}^{(2)}$	0.2			
$V_{IH}$	ON/OFF pin high-level input voltage	$V_{IN} = 5.0\text{ V}$ , $R1 = 10\text{ k}\Omega$	1.0			V	
$R_{Q1(ON)}$	Q1 Channel ON resistance <sup>(4)</sup>		$V_{GS} = -4.5\text{ V}$ , $I_{D}(Q1) = 3.0\text{ A}$	32	55	m $\Omega$	
			$V_{GS} = -3.0\text{ V}$ , $I_{D}(Q1) = 2.5\text{ A}$	44	77		
			$V_{GS} = -2.5\text{ V}$ , $I_{D}(Q1) = 2.5\text{ A}$	50	85		
			$V_{GS} = -1.8\text{ V}$ , $I_{D}(Q1) = 2.0\text{ A}$	82	147		
			$V_{GS} = -1.5\text{ V}$ , $I_{D}(Q1) = 1.0\text{ A}$	93	166		
			$V_{GS} = -1.2\text{ V}$ , $I_{D}(Q1) = 0.5\text{ A}$	155	260		
$R_{Q2(ON)}$	Q2 Channel ON resistance		$V_{GS} = 4.5\text{ V}$ , $I_{D}(Q2) = 0.4\text{ A}$	1.8	3	$\Omega$	
			$V_{GS} = 3.0\text{ V}$ , $I_{D}(Q2) = 0.3\text{ A}$	2.3	6.2		
			$V_{GS} = 2.5\text{ V}$ , $I_{D}(Q2) = 0.2\text{ A}$	2.6	6.1		
			$V_{GS} = 1.8\text{ V}$ , $I_{D}(Q2) = 0.1\text{ A}$	3.8	10		
			$V_{GS} = 1.5\text{ V}$ , $I_{D}(Q2) = 0.05\text{ A}$	4.4	8.5		
			$V_{GS} = 1.2\text{ V}$ , $I_{D}(Q2) = 0.03\text{ A}$	6.25	13.5		
<b>Q1 DRAIN-SOURCE DIODE PARAMETERS<sup>(3)(5)</sup></b>							
$I_{FSD}$	Source-drain diode peak forward current	$V_{FSD} = 0.8\text{ V}$ , $V_{ON/OFF} = 0\text{ V}$	1.0			A	
$V_{FSD}$	Source-drain diode forward voltage	$V_{ON/OFF} = 0\text{ V}$ , $I_{FSD} = -0.6\text{ A}$ ,	1.0			V	

- (1) Pull-up Resistor R1 dependent
- (2) Guaranteed by design only
- (3) Pulse width  $< 300\ \mu\text{s}$ , Duty Cycle  $< 2.0\%$
- (4) Refer to SOA charts for current rating
- (5) Not rated for continuous current operation

**DEVICE INFORMATION**



**TPS27081A PIN DESCRIPTION**

PIN		DESCRIPTION
NAME	NUMBER	
R2	1	Source Terminal of NMOS (Q2) - Connect to system GND directly or through a slew rate control resistor
VOUT	2, 3	Drain Terminal of Power PFET (Q1) - Connect a slew control capacitor between pins VOUT and R1/C1
VIN	4	Source Terminal of Power PFET (Q1) - connect a pull-up resistor between the pins VIN/R1 and R1/C1
ON/OFF	5	Active high enable pin – when driven with a high impedance driver connect an external pull down resistor to GND
R1/C1	6	Gate Terminal of Power PFET (Q1)

## APPLICATION INFORMATION

The TPS27081A IC is a high side load switch that integrates a Power PFET and a Control NMOS in a tiny package. The TPS27081A internal components are rated for up to 8V supply and support up to 3A of load current. The TPS27081A can be used in a variety applications. Figure 3 below shows a general application of TPS27081A to control the load inrush current.

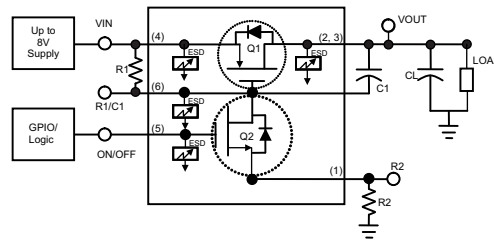


Figure 3. Typical Application Diagram

### Configuring Q1 ON Resistance

The  $V_{GS-Q1}$  Gate-Source voltage across the PMOS transistor Q1 sets its ON resistance  $R_{Q1(ON)}$ . Directly connecting the pin R2 to ground maximizes the ON state  $V_{GS-Q1}$  and thus minimizes the VIN to VOUT voltage dropout. When a resistor R2 is installed to control the Turn-ON slew rate then  $V_{GS-Q1}$  is given by:

$$V_{GS-Q1} = -VIN \times \frac{R1}{R1+R2} \text{ V}$$

e.g.  $R1 = 10 \times R2$ ,  $VIN = 5V$  sets  $V_{GS-Q1} = -4.5V$  (1)

**Note:** It is recommended to keep  $R1 > 10 \times R2$ . Higher value of resistor R1 minimizes quiescent current when is PMOS is on, however may adversely impact off state leakage current. Refer to the ILoad parameter in the [ELECTRICAL CHARACTERISTICS](#).

### Configuring Turn-ON Slew Rate

Switching a large capacitive load CL instantaneously results in a load inrush current given by the following equation:

$$I_{inrush} = C_{load} \times \frac{dv}{dt} = C_{load} \times \frac{V_{OUT_{final}} - V_{OUT_{initial}}}{V_{out \text{ Slew Rate}}} \text{ (2)}$$

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate at the output resulting in a very high dv/dt thus leading to a higher inrush current. To control the inrush current connect a resistor R2 and a capacitor C1 as shown in the [Electrical Characteristics Table](#). Use the following equation to configure the TPS27081A slew rate to a specific value. Refer to [Table 1](#) for component values to configure TPS27081A to achieve standard slew rates.

$$t_{rise} = \frac{3.9 \times R2 \times C1}{VIN^{2/3}} \text{ sec} \text{ (3)}$$

Where  $t_{rise}$  is the time delta starting from the ON/OFF signal's rising edge to charge up the load capacitor CL from 10% to 90% of VIN voltage.

**Note:** The  $t_{rise}$  equation is accurate to within +/-20% across full VIN range supported by TPS27081A. Ensure that  $R1 > 10 \times R2$ .

**Table 1. Component Values for VOUT Rise Time**

C1 (1)	Rise Time (μs) <sup>(2)(3)</sup>							
	R1=10kΩ, R2=1kΩ				R1=5.1kΩ, R2=510Ω			
	VIN = 7V	VIN = 5V	VIN = 3.3V	VIN = 1.2V	VIN = 7V	VIN = 5V	VIN = 3.3V	VIN = 1.2V
220pF	.253	.316	.416	.810	.129	.161	.212	.413
1000pF	1.15	1.44	1.89	3.68	.586	.732	.963	1.88
4700pF	5.4	6.75	8.88	17.3	2.76	3.44	4.53	8.83
0.18uF	207	258	340	663	106	132	173	338
0.27uF	310	388	510	994	158	198	260	507
0.33uF	379	474	623	1220	194	242	318	620
1uF	1150	1440	1890	3680	586	732	963	1880

(1) Typical ceramic capacitor values

(2) CLoad=10uF. Output rise time is independent of CLoad when CLoad >> C1

(3) Rise Time is 250ns for R2=0Ω and C1=CLoad=0F

### Configuring Turn-OFF Delay

TPS27081A PMOS turn-off delay from the falling edge of ON/OFF logic signal depends upon the component values of resistor R1 & capacitor C1. Lower values of resistor R1 ensures quicker turn-off.

$$t_{off} > 2 \times R1 \times C1 \text{ sec}$$

### Low Voltage ON/OFF Interface

The VGS<sub>Q2</sub> is set by the ON/OFF logic level. To turn ON, the transistor Q2 requires a VGS > 1.0V (Typical). For reliable operation apply ON/OFF logic that has the following VIH and VIL limits:

$$VIH_{ON} > 1.0V + I_{Q2} \times R2 \text{ V}$$

$$VIL_{OFF} < 0.2 \text{ V}$$

Minimizing I<sub>Q2</sub> x R2 drop helps achieve a direct interface with a low voltage ON/OFF logic. To minimize I<sub>Q2</sub> x R2 voltage drop select a high R1/R2 ratio. E.g. When VIN= 1.8V, selecting R1/R2 = 40 will require VIH > 1.0 + 45mV and thus allowing a 1.2V GPIO interface.

In applications where ON/OFF signal is not available connect ON/OFF pin to VIN. The TPS27081A will turn ON/OFF in sync with the input supply connected to VIN.

**Note:** Connect a pull down resistor between ON/OFF pin to GND when ON/OFF is driven by a high-impedance (tri-state) driver.

### On-Chip Power Dissipation

Use the below equation to calculate TPS27081A on-chip power dissipation P<sub>D</sub>:

$$PD = ID_{Q1}^2 \times R_{Q1(ON)} + ID_{Q2}^2 \times R_{Q2(ON)}$$

Where, ID<sub>Q1</sub> and ID<sub>Q2</sub> are the DC current flowing through the transistors Q1 and Q2 respectively. Refer to the [ELECTRICAL CHARACTERISTICS](#) table and/or [Figure 10](#) through [Figure 16](#) to estimate R<sub>Q1(ON)</sub> and R<sub>Q2(ON)</sub> for various values of VGS<sub>Q1</sub> and VGS<sub>Q2</sub> respectively.

**Note:** MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 and Q2 going into saturation region set VGS > VT +VDS. E.g. VGS > 1.5V and VDS < 200mV ensures operation as a switch.

## Thermal Reliability

For higher reliability it is recommended to limit TPS27081A IC's die junction temperature to less than 105°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to achieve the maximum die junction temperature target:

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

Where:

$T_{J(MAX)}$  is the target maximum junction temperature.

$T_A$  is the operating ambient temperature.

$R_{\theta JA}$  is the package junction to ambient thermal resistance.

(4)

## Improving Package Thermal Performance

The package  $\theta_{JA}$  value under standard conditions on a High-K board is listed in the [DISSIPATION RATINGS](#).  $\theta_{JA}$  value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce  $\theta_{JA}$  and thus improve device thermal capabilities. Refer to TI's design support web page at [www.ti.com/thermal](http://www.ti.com/thermal) for a general guidance on improving device thermal performance.

APPLICATION EXAMPLES

TFT LCD Module Inrush Current Control

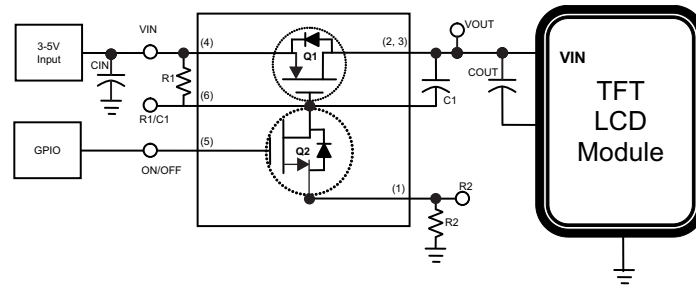


Figure 4. Inrush Current Control Using TPS27081A

LCD panels require inrush current control to prevent permanent system damages during turn-ON and turn-OFF events.

Standby Power Isolation

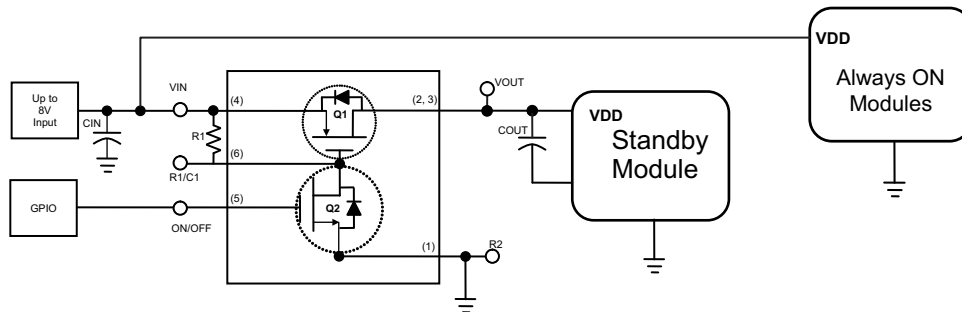


Figure 5. Standby Power Generation Using TPS27081A

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27081A requires only a single pull-up resistor. In this configuration the VOUT voltage rise time is approximately 250ns when VIN = 5V.



### Boost Regulator with True Shutdown

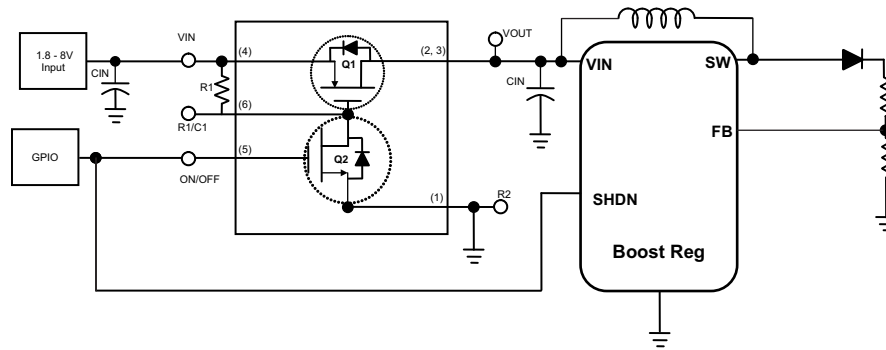


Figure 6. True Shutdown Using TPS27081A

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator is shut down. Adding a TPS27081A in the input side power path prevents this leakage current and thus providing a true shutdown.

### Single Module Multiple Power Supply Sequencing

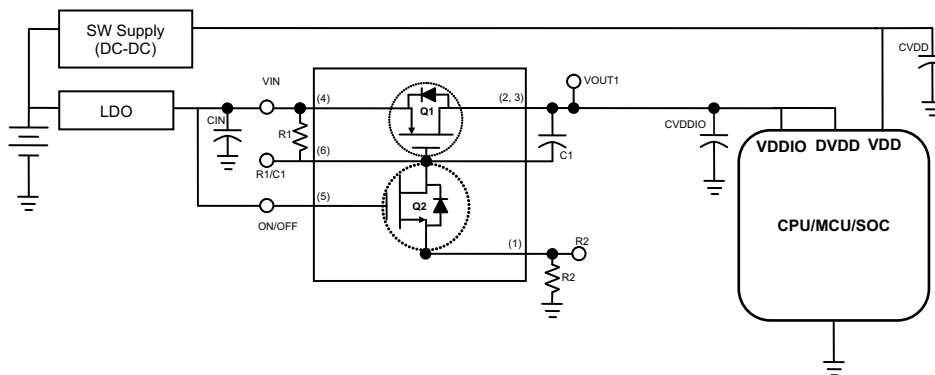
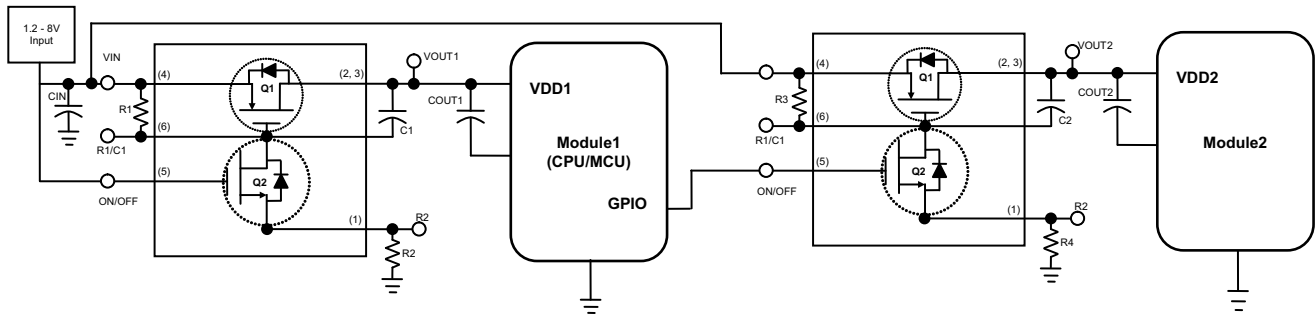


Figure 7. Power Sequencing Using TPS27081A, Example 1

Most modern SOC's and CPU's require multiple voltage inputs for its Analog, Digital cores and IO interfaces. These ICs require that these supplies be applied simultaneously or in a certain sequence. TPS27081A when configured, as shown in Figure 7, with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, will delay the early arriving LDO output to match up with late arriving DC-DC output and thus achieving power sequencing.

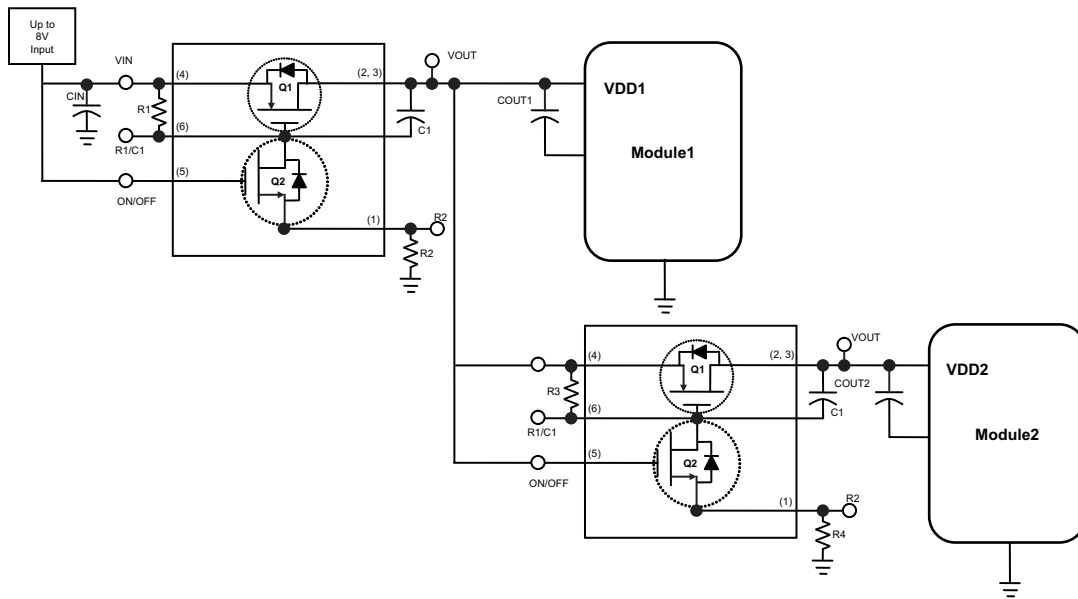
**Multiple Modules Interdependent Power Supply Sequencing**



**Figure 8. Power Sequencing Using TPS27081A, Example 2**

For system integrity reasons a certain power sequencing may be required among various modules. As shown in [Figure 8](#), Module 2 will power up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. TPS27081A when used as shown in [Figure 8](#) will not only sequence the Module 2 power, but also it will help prevent inrush current into the power path of Module 1 and 2.

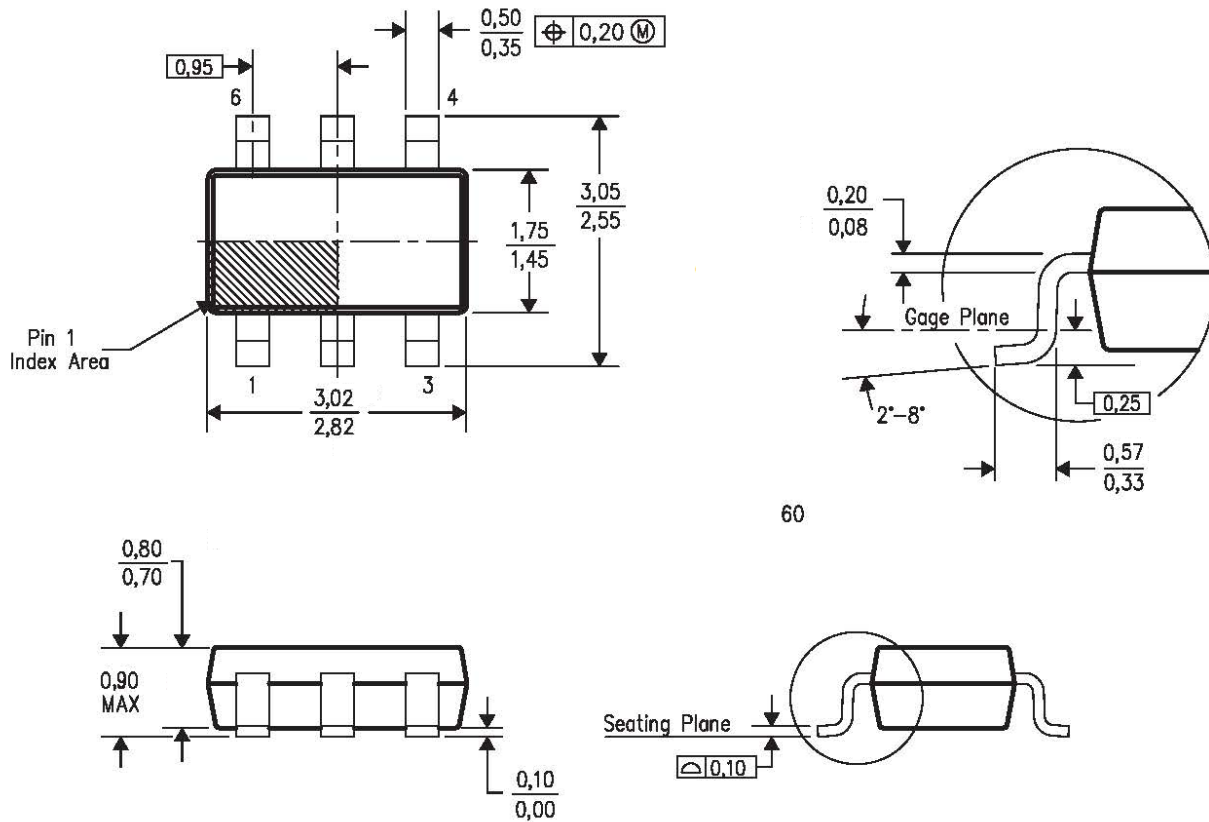
**Multiple Modules Interdependent Supply Sequencing without a GPIO Input**



**Figure 9. Power Sequencing using TPS27081A, Example 3**

When a GPIO signal is not available connecting the ON/OFF pin of TPS27081 connected to Module 2 will power up Module 2 after Module 1, when resistor R4 and capacitor C1 are chosen appropriately. The two TPS27081A in this configuration will also control load inrush current.

TPS27081A THIN SOT<sub>(DDC)</sub> SPECIFIC PACKAGE DIMENSIONS



NOTES:

- All linear dimensions are in millimeters.
- Body dimensions do not include mold flash or protrusion.
- Falls within JEDEC MO-193 variation AA (6 pin).

TYPICAL CHARACTERISTICS

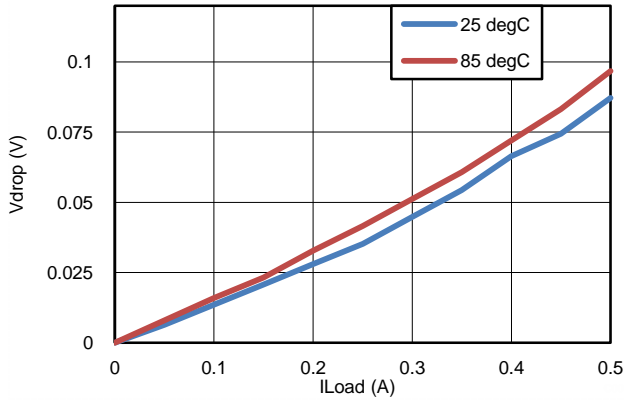


Figure 10. Vdrop vs IL; VGS<sub>Q1</sub>=-1.2V

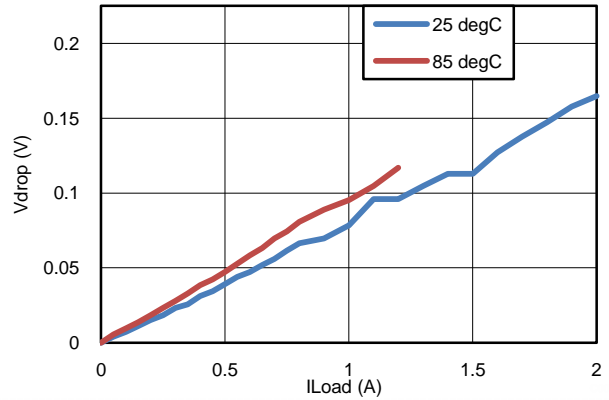


Figure 11. Vdrop vs IL; VGS<sub>Q1</sub>=-1.8V

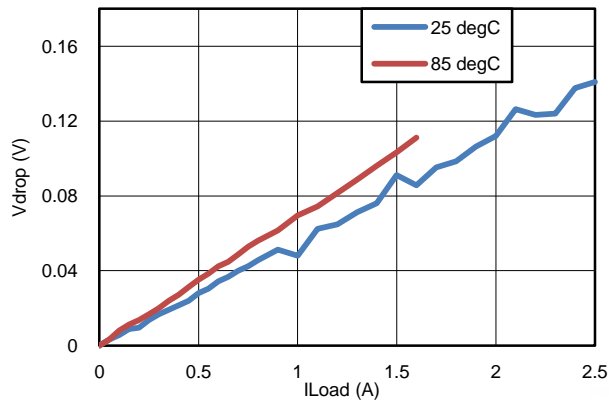


Figure 12. Vdrop vs IL; VGS<sub>Q1</sub>=-2.5V

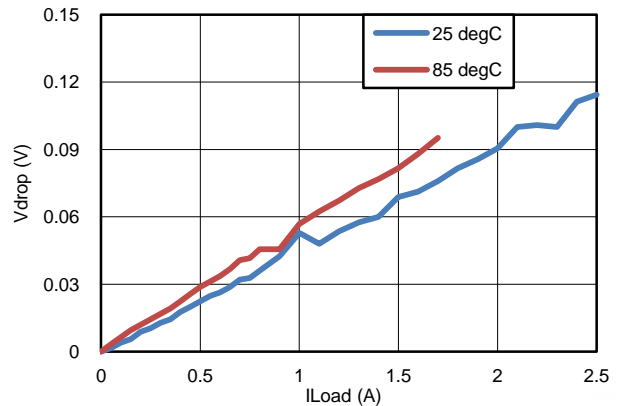


Figure 13. Vdrop vs IL; VGS<sub>Q1</sub>=-3.3V

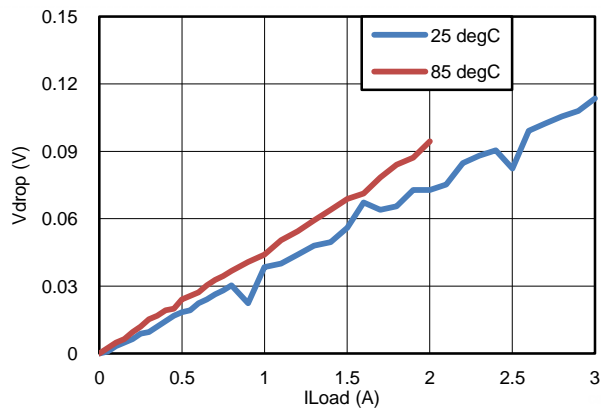


Figure 14. Vdrop vs IL; VGS<sub>Q1</sub>=-4.5V

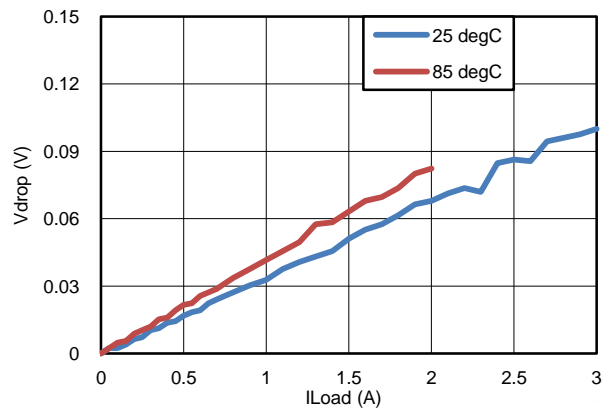
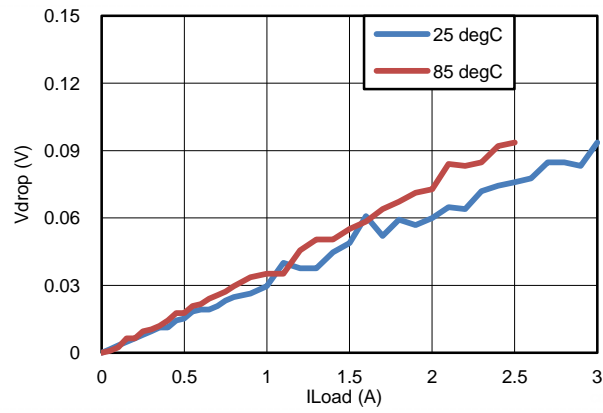


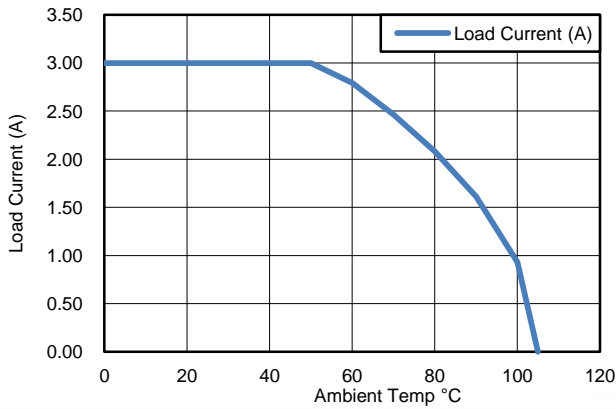
Figure 15. Vdrop vs IL; VGS<sub>Q1</sub>=-5.5V

**TYPICAL CHARACTERISTICS (continued)**

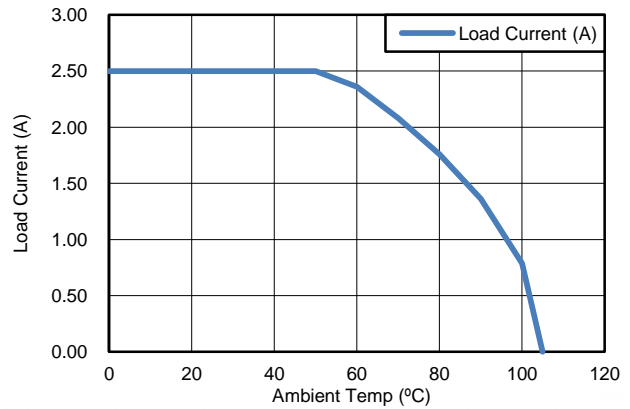


**Figure 16. Vdrop vs ILoad; VGS<sub>Q1</sub> = -7V**

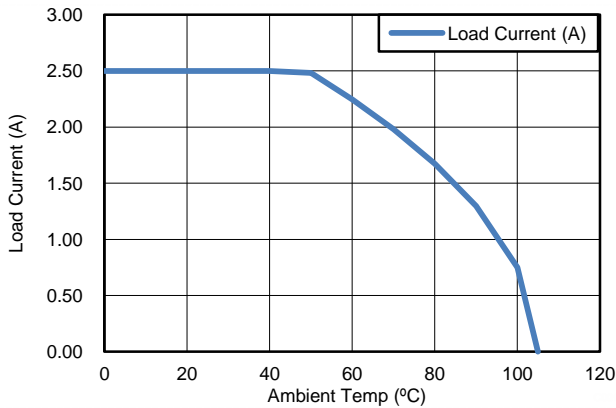
**PFET Q1 Minimum Safe Operating Area (SOA)**



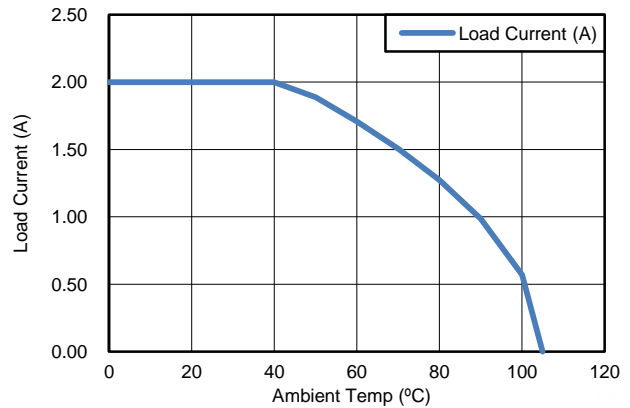
**Figure 17. Q1 SOA @ VGS\_Q1 = -4.5V**



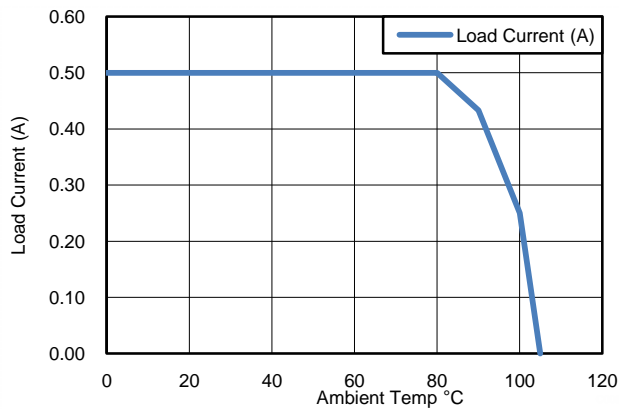
**Figure 18. Q1 SOA @ VGS\_Q1 = -3.0V**



**Figure 19. Q1 SOA @ VGS\_Q1 = -2.5V**



**Figure 20. Q1 SOA @ VGS\_Q1 = -1.8V**



**Figure 21. Q1 SOA @ VGS\_Q1 = -1.2V**

**REVISION HISTORY****Changes from Revision B (September 2012) to Revision C** **Page**

- 
- 从数据表中删除了 DRV 封装预览。 ..... 1
- 

**Changes from Revision C (January 2013) to Revision D** **Page**

- 
- 更新了文档中的措词。 ..... 1
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS27081ADDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	Call TI   SN	Level-1-260C-UNLIM	-40 to 85	AUA	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	180.0	9.5	3.17	3.1	1.1	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS27081ADDCR	SOT-23-THIN	DDC	6	3000	184.0	184.0	19.0

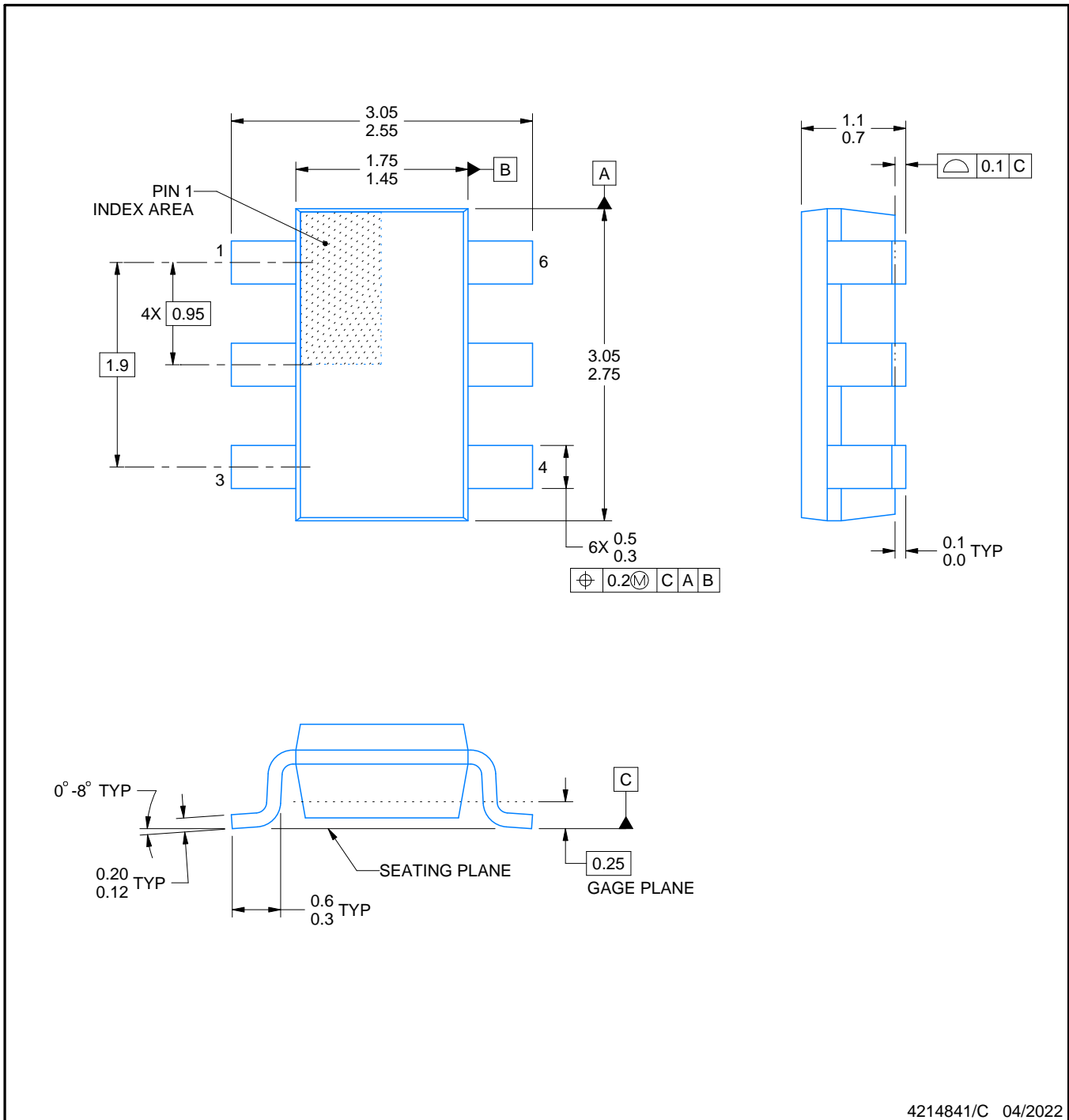
# DDC0006A



# PACKAGE OUTLINE

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214841/C 04/2022

## NOTES:

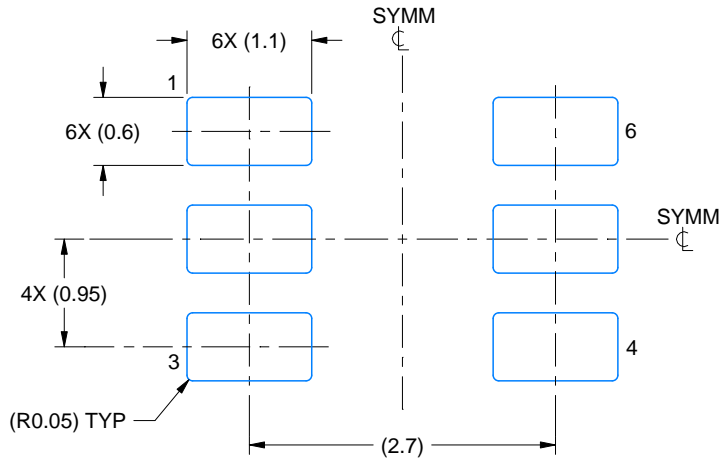
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

# EXAMPLE BOARD LAYOUT

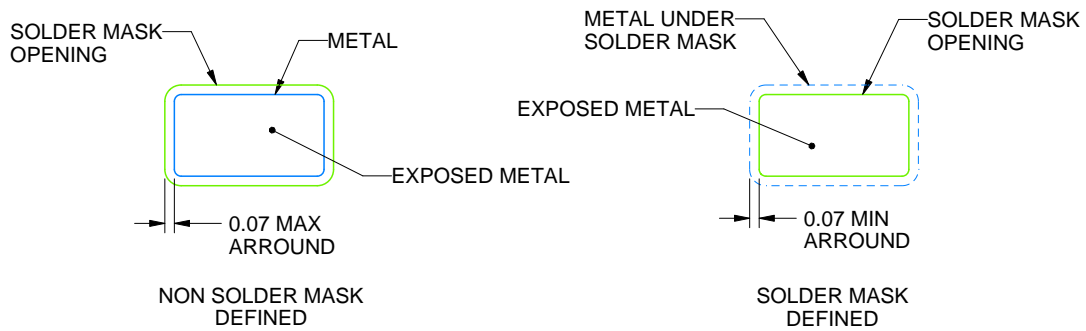
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDEMASK DETAILS

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NOTES: (continued)

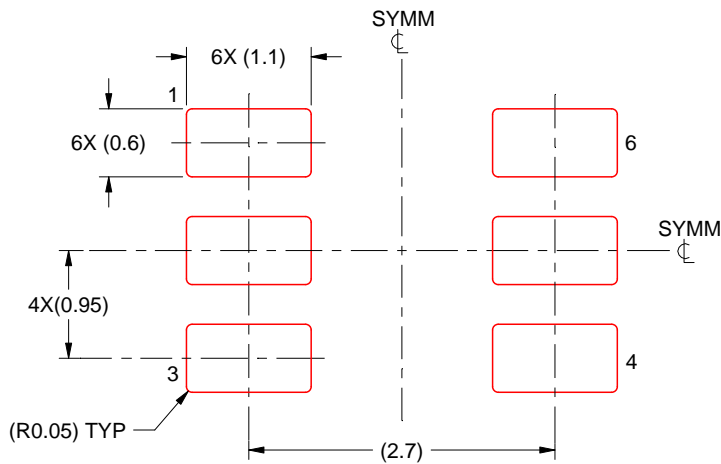
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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