适用于 VR12.6 V_{CPU} 的两相 D-CAP+™ 降压控制器

1 特性

- Intel® *VR12.6 PWM 规格*符合串行 VID (SVID) 标准
- 单相或两相运行
- 完整的 VR12.6 移动功能集，包括数字电流监控器、PS3 和 PS4 运行
- 输出电压范围为 0.50V 至 2.30V 的 8 位 DAC
- 优化了轻负载和重负载条件下的效率
- 8 级独立的过冲衰减 (OSR) 和下冲衰减 (USR)
- 无驱动器配置，有助于实现高效的高频开关
- 支持分立式、电源块、功率级或 DrMOS MOSFET 实施
- 精确可调电压定位
- 300kHz 至 1.5MHz 的频率选择
- 获得专利的 AutoBalance 相位平衡
- 可选 8 级电流限制
- 4.5V 至 28V 转换电压范围
- 小型 4 × 4 32 引脚 QFN PowerPAD™ 集成电路封装

2 应用

- VR12.6 VCPU 应用，适用于
  - 适配器
  - 电池
  - NVDC
  - 5V 至 12V 电源轨

3 说明

TPS51624 是一款无驱动器、完全符合 SVID 标准的 VR12.6 降压控制器。高级控制特性（例如 D-CAP+ 架构）借助重叠脉冲支持下冲衰减 (USR) 和过冲衰减 (OSR)，可提供快速瞬态响应、最低输出电容和高效率。TPS51624 还支持在 CCM 或 DCM 运行情况下进行单相运行，从而提高轻负载情况下的效率。TPS51624 集成了完整的 VR12.6 I/O 功能，包括 VR_READY (PGOOD)、$\overline{\text{ALERT}}$ 和 $\overline{\text{VR\_HOT}}$。SVID 接口地址允许在 0 到 7 的时间范围内进行编程。在 PS4 中，控制器的静态功耗通常为 0.25mW。VCPU 压摆率和电压定位的可调节控制完善了 VR12.6 功能。与新的 TPS51604 FET 栅极驱动器配合使用时，该解决方案可提供超高速度和低开关损耗。TPS51624 与选定的 TI Power Stage™ 产品以及 DrMOS 产品一起使用，可实现出色效率。

TPS51624 器件采用节省空间的热增强型 32 引脚 QFN 封装，可在 –40°C 到 105°C 温度下运行。

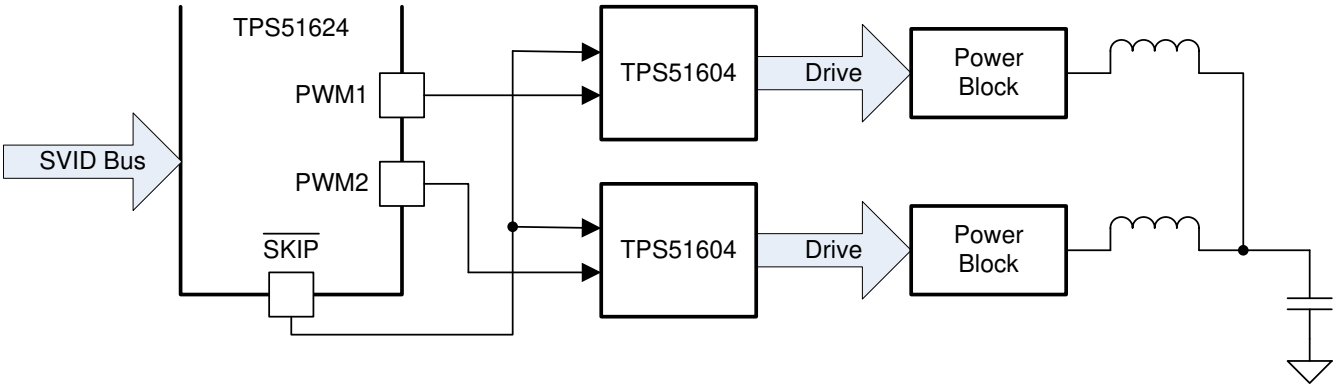

图 3-1. 简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
June 2022	*	Initial Release

5 Device and Documentation Support

5.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

5.3 Trademarks

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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

6 Mechanical, Packaging, and Orderable Information

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51624RSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TPS 51624	Samples
TPS51624RSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	TPS 51624	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

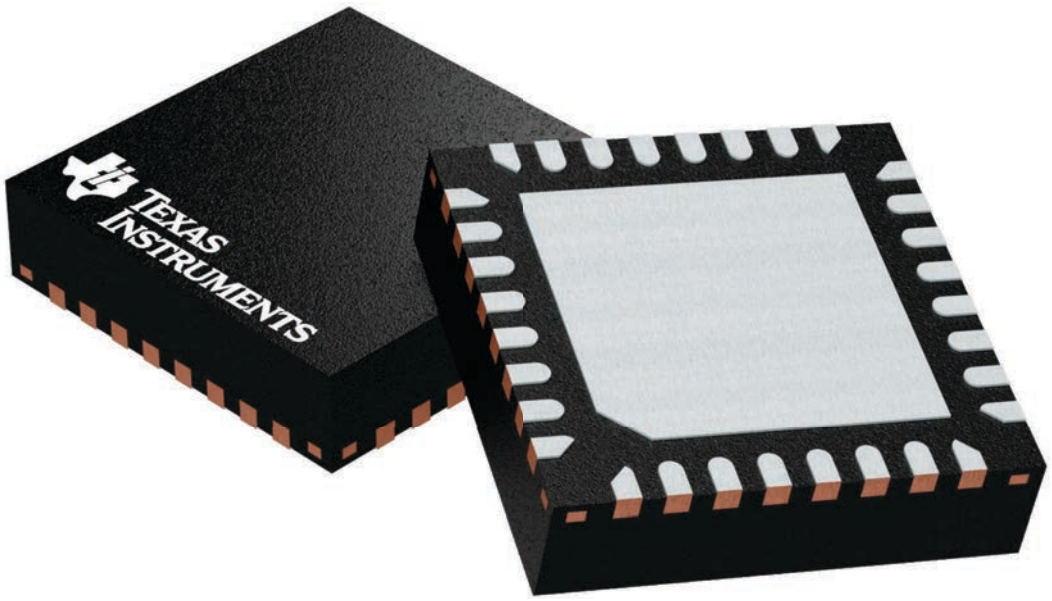
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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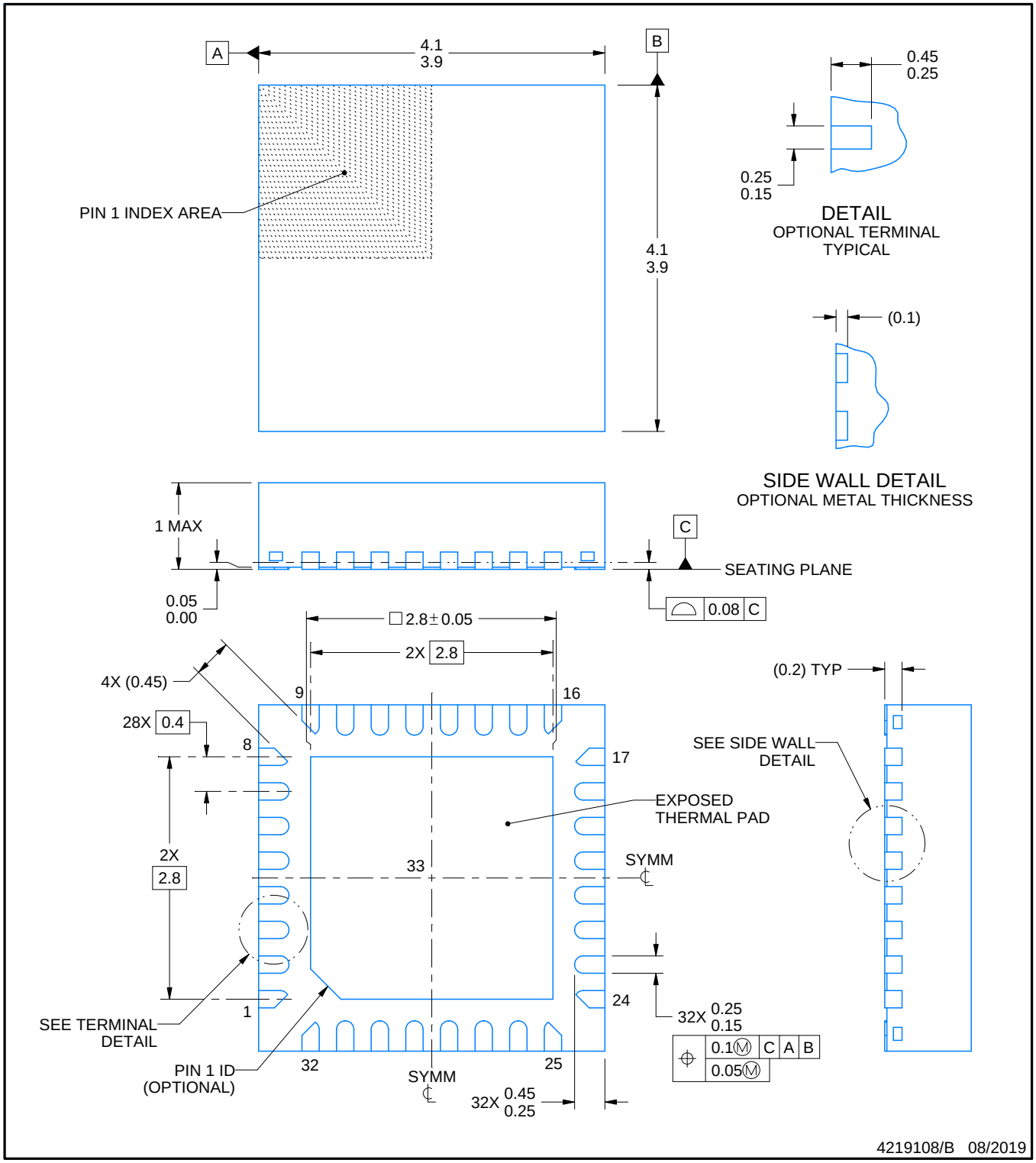
PACKAGE OUTLINE

RSM0032B

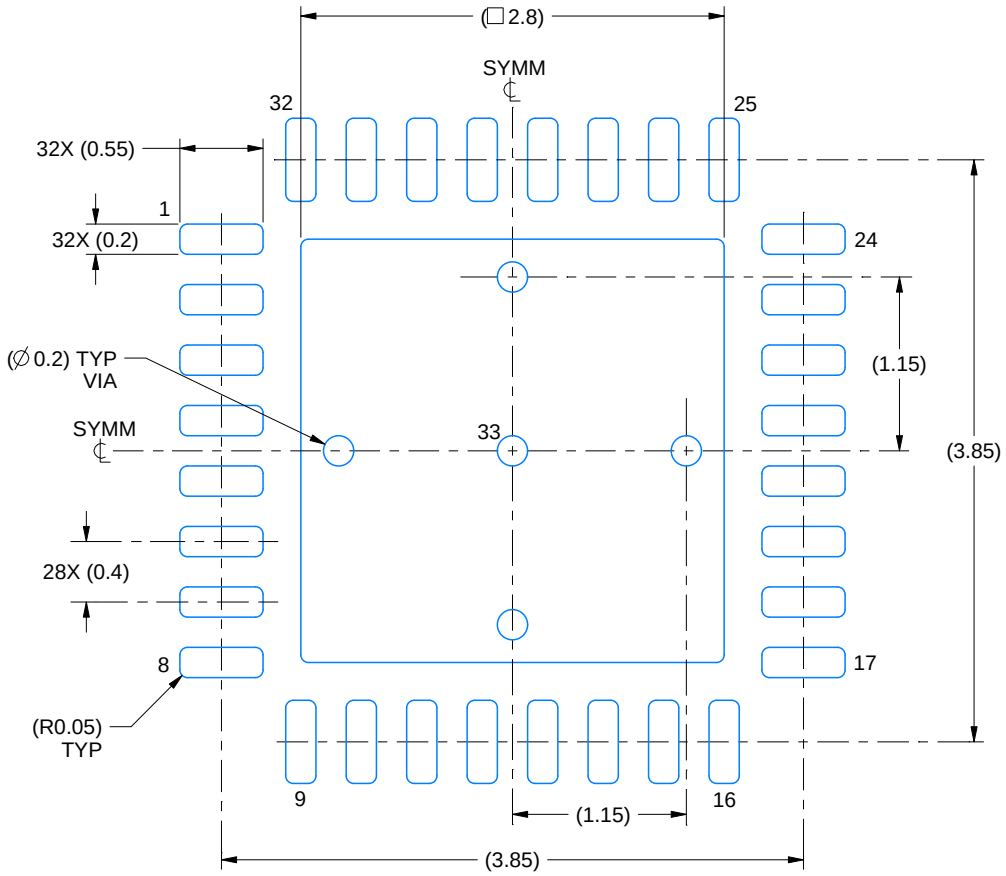
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

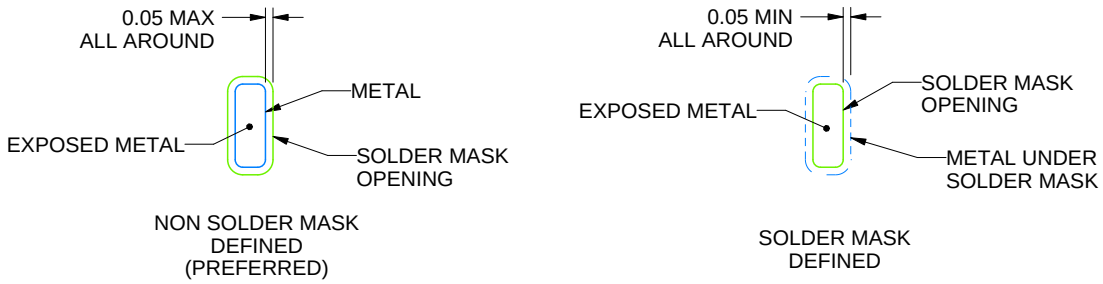


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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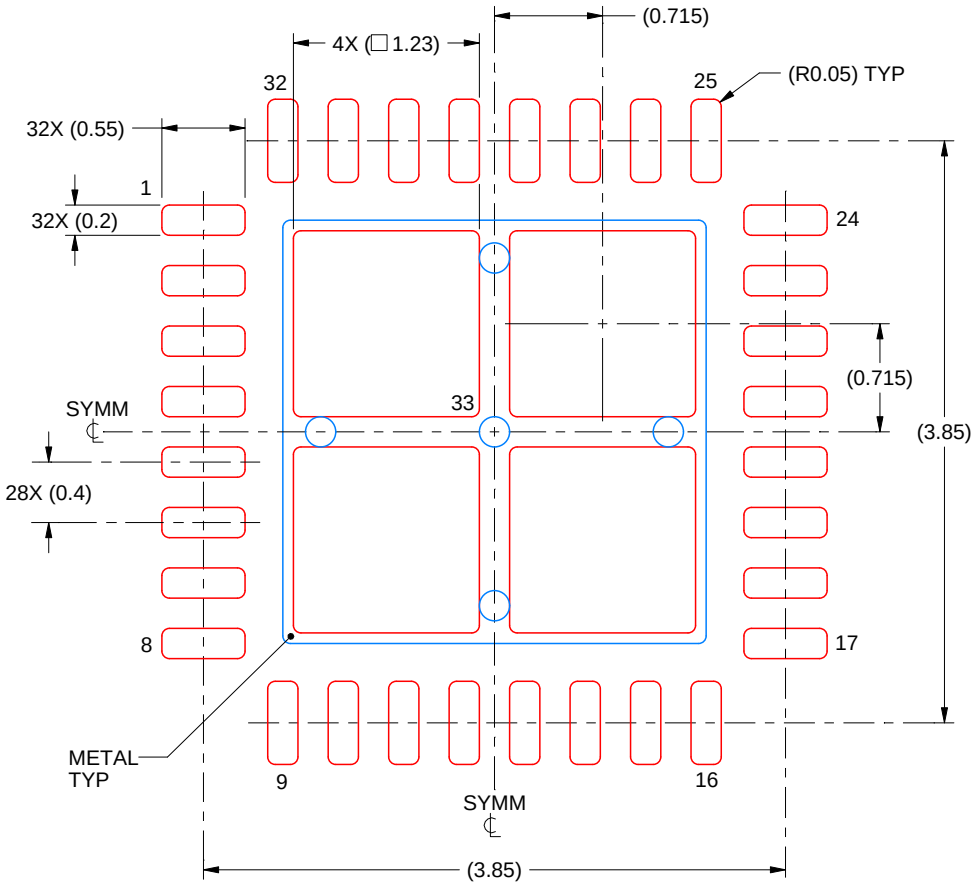
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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