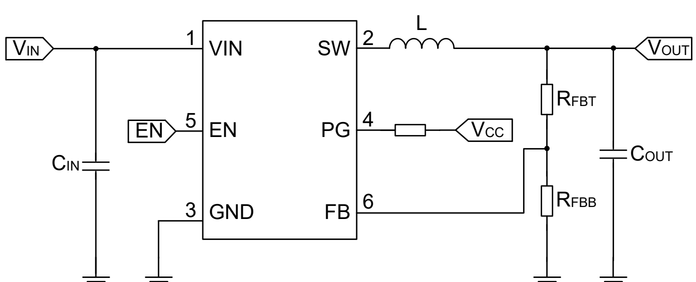
TPS56325x 采用 SOT-563 封装的 3V 至 16V 输入、3A 同步降压转换器

1 特性

- 专用于多种应用
  - 3V 至 16V 输入电压范围
  - 0.6V 至 7V 输出电压范围
  - 0.6V 基准电压
  - 25°C 时，基准精度为 ±1%
  - 在 -40°C 至 125°C 温度范围内，基准精度为 ±1.5%
  - 集成式 55.2mΩ 和 24.3mΩ MOSFET
  - 100 µA 低静态电流
  - 1.4MHz 开关频率
  - 以最大 93% 的高占空比运行
  - 精密 EN 阈值电压
  - 1.6 ms 固定软启动时间（典型值）
- 解决方案尺寸小巧且易于使用
  - 轻负载下 TPS563252 采用 Eco-mode，TPS563257 采用 FCCM 模式
  - D-CAP3™ 控制拓扑
  - 通过集成自举电容器轻松布局
  - 支持带预偏置输出的启动
  - 开漏电源正常状态指示器
  - 非锁存 OV、OT 和 UVLO 保护
  - UV 保护的断续模式
  - 逐周期 OC 和 NOC 保护
  - 1.6mm × 1.6mm SOT-563 封装
- 使用 TPS563252 并借助 WEBENCH® Power Designer 创建定制设计方案
- 使用 TPS563257 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- WLAN/Wi-Fi 接入点、开关、路由器
- 专业音频、监控、无人机
- DTV、STB 和 DVR、智能扬声器



简化原理图

3 说明

TPS56325x 是一款简单、易用、高效率、高功率密度的同步降压转换器，输入电压范围为 3V 至 16V，在 0.6V 至 7V 的输出电压范围内，支持高达 3A 的持续输出电流。

TPS56325x 采用 DCAP3 拓扑提供快速瞬态响应并支持低 ESR 输出电容器，无需外部补偿。该器件可支持以高达 93% 的占空比运行。集成自举电容器有助于实现单层 PCB 并节省总 BOM 成本。

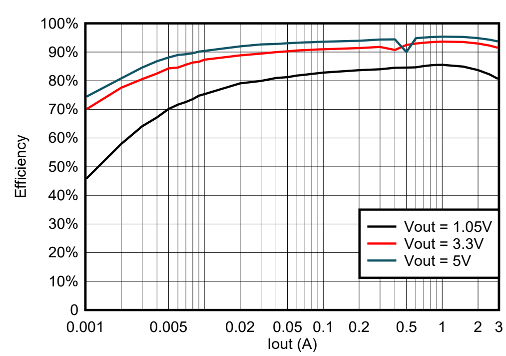
TPS563252 在 Eco-mode 下运行，可在轻负载时保持高效率。TPS563257 在 FCCM 模式下运行，可在所有负载条件下保持相同的频率和较低的输出纹波。该器件集成了全面的断续模式 OVP、OCP、UVLO、OTP 和 UVP 保护。

该器件采用 1.6mm x 1.6mm SOT-563 封装。额定结温范围为 -40°C 至 125°C。

器件信息

器件型号	模式	封装(1)
TPS563252	ECO	DRL（SOT-563，6）
TPS563257	FCCM	

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



TPS563252 在 V_{IN} = 12V 时的效率

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
August 2022	*	Advance Information

5 Pin Configuration and Functions

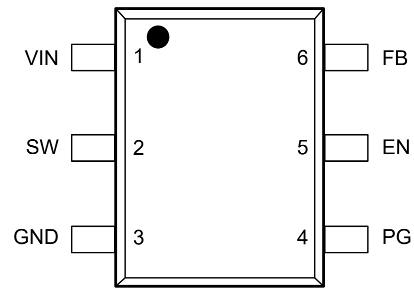

图 5-1. 6-Pin SOT563 DRL Package (Top View)

表 5-1. Pin Functions

Pin		Type[(1)]	Description
Name	NO.		
VIN	1	P	Input voltage supply pin. Connect the input decoupling capacitors between VIN and GND.
SW	2	P	Switch node pin. Connect the output inductor to this pin.
GND	3	G	GND pin for the controller circuit and the internal circuitry
PG	4	A	Open-drain power-good indicator
EN	5	A	Enable input control. Driving EN high enables the converter
FB	6	A	Converter feedback input. Connect to output voltage with a feedback resistor divider.

(1) A = Analog, P = Power, G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Pin voltage[(2)]	VIN	–0.3	18	V
	FB, EN, PG	–0.3	6	
	GND	–0.3	0.3	
	SW, DC	–2	18	
	SW (transient < 20 ns)	–5.5	20	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)], all pins	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Pin voltage	VIN	3		16	V
	FB, EN, PG	–0.1		5.5	
	GND	–0.1		0.1	
	SW, DC	–1		16	
	SW (transient < 20 ns)	–5		18	
Output current	I_{OUT}	0		3	A
Temperature	Operating junction temperature, T_J	–40		125	°C
	Storage temperature, T_{stg}	-40		150	

6.4 Thermal Information

THERMAL METRIC[(1)]		DRL (SOT-563)	UNIT
		6 PINS	
$R_{\theta JA}$ [(2)]	Junction-to-ambient thermal resistance	137.4	°C/W
$R_{\theta JA\_effective}$ [(3)]	Junction-to-ambient thermal resistance on EVM board	74	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		DRL (SOT-563)	UNIT
		6 PINS	
ψ_{JB}	Junction-to-board characterization parameter	29.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were simulated on a standard JEDEC board. They do not represent the performance obtained in an actual application.
(3) This $R_{\theta JA\_effective}$ is tested on TPS563252EVM board (2 layer, copper thickness is 2-oz) at V_{IN} = 12V, V_{OUT} =5V, I_{OUT} = 3A, T_A = 25°C.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
V_{IN}	Input voltage range	V_{IN}	3		16	V
I_{VIN}	VIN supply current	No load, V_{EN} = 5 V, V_{FB} = 0.65 V, non-switching, ECO version		100		µA
		No load, V_{EN} = 5 V, V_{FB} = 0.65 V, non-switching, FCCM version		360		µA
I_{INSDN}	VIN shutdown current	No load, V_{EN} = 0 V		2		µA
UVLO						
V_{IN_UVLO}	Input undervoltage lockout threshold	Rising threshold		2.92		V
		Falling threshold		2.72		V
		Hysteresis		200		mV
FEEDBACK VOLTAGE						
V_{REF}	FB voltage	T_J = 25°C	594	600	606	mV
		T_J = –40°C to 125°C	591	600	609	mV
INTEGRATED POWER MOSFETS						
R_{DSON_HS} [1]	High-side MOSFET on-resistance	T_J = 25°C, $V_{IN} \geqslant$ 5 V		55.2		mΩ
		T_J = 25°C, V_{IN} = 3 V		67.5		mΩ
R_{DSON_LS}	Low-side MOSFET on-resistance	T_J = 25°C, $V_{IN} \geqslant$ 5 V		24.3		mΩ
		T_J = 25°C, V_{IN} = 3 V		30.2		mΩ
SWITCHING FREQUENCY						
f_{sw}	Switching frequency	T_J = 25°C, V_{OUT} = 3.3 V		1400		kHz
$t_{ON(MIN)}$ [1]	Minimum on time	T_J = 25°C		60		ns
$t_{OFF(MIN)}$ [1]	Minimum off time	V_{FB} = 0.5 V		110		ns
LOGIC THRESHOLD						
V_{ENH}	EN threshold high level	Rising enable threshold	1.15	1.19	1.25	V
V_{ENL}	EN threshold low level	Falling disable threshold	0.9	1	1.1	V
V_{ENHYS}	EN hysteris	Hysteresis		190		mV
R_{EN}	EN pulldown resistor			2		MΩ
CURRENT LIMIT						
I_{OCL_LS}	Overcurrent threshold	Valley current set point	3.1	4.1	5	A
I_{NOC}	Negtive overcurrent threshold		1.5	2.1	2.5	A
SOFT START						
t_{SS}	Internal soft start time			1.6		ms
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold	V_{FB} rising	110%	115%	120%	

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T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVPDLY}	OVP prop deglitch			24		µs
V_{UVP}	UVP trip threshold	V_{FB} falling	55%	60%	65%	
t_{UVPDLY}	UVP prop deglitch			256		µs
t_{UVPDEL}	Hiccup delay relative to SS time	UVP detect		256		µs
t_{UVPEN}	Hiccup enable delay relative to SS time	UVP detect		14		ms
POWER GOOD						
V_{PGTH}	Power good threshold	FB falling, PG from high to low	80%	85%	90%	
		FB rising, PG from low to high	85%	90%	95%	
		FB falling, PG from low to high	105%	110%	115%	
		FB rising, PG from high to low	110%	115%	120%	
$V_{PG(OL)}$	PG pin output low-level voltage	I_{OL} = 4 mA			0.4	V
$I_{PG(LKG)}$	PG pin leakage current when open drain output is high	V_{PG} = 5.5 V			1	µA
$t_{PG(R)}$	PG delay going from low to high			1		ms
$t_{PG(F)}$	PG delay going from high to low			32		µs
THERMAL SHUTDOWN						
T_{SDN} (1)	Thermal shutdown threshold	Shutdown temperature		155		°C
T_{OTPHSY} (1)		Hysteresis		20		

(1) Specified by design

6.6 Typical Characteristics

T_J = -40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

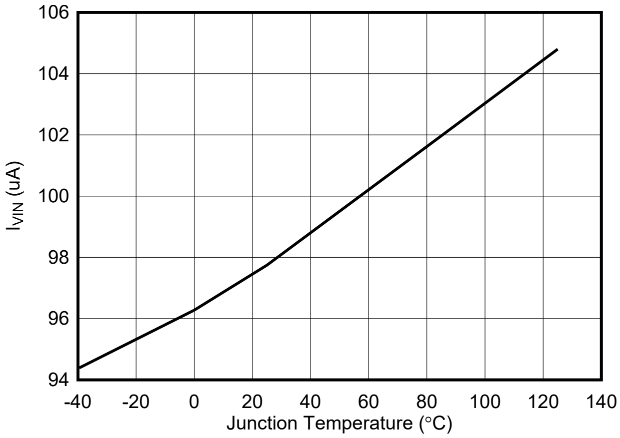

图 6-1. TPS563252 Quiescent Current

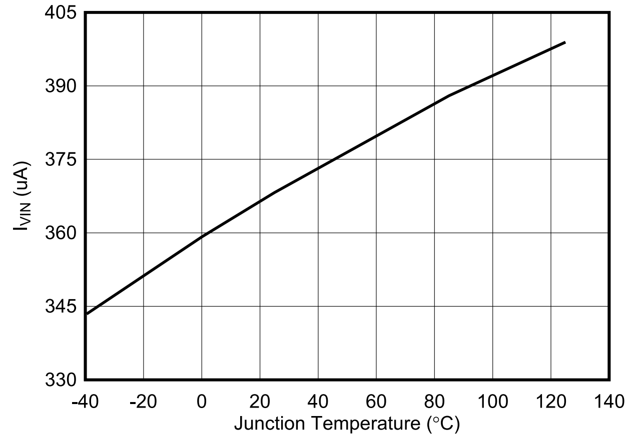

图 6-2. TPS563257 Quiescent Current

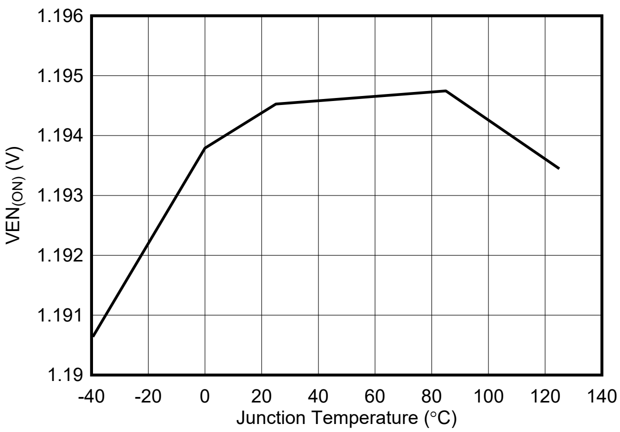

图 6-3. Enable On Threshold Voltage

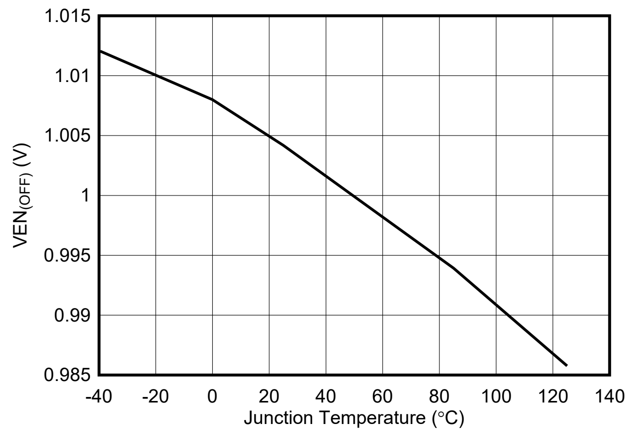

图 6-4. Enable Off Threshold Voltage

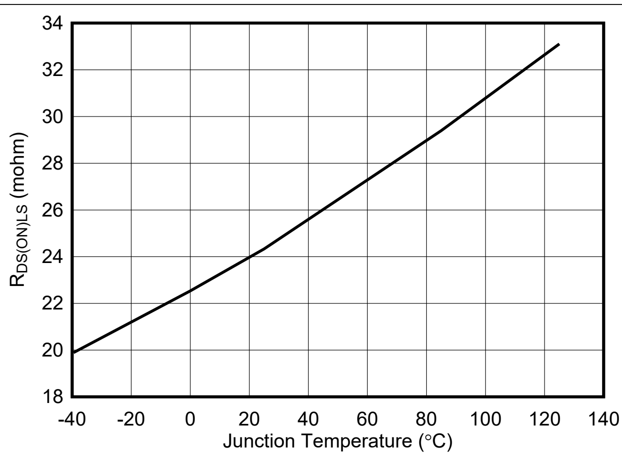

图 6-5. Low-Side $R_{DS(ON)}$

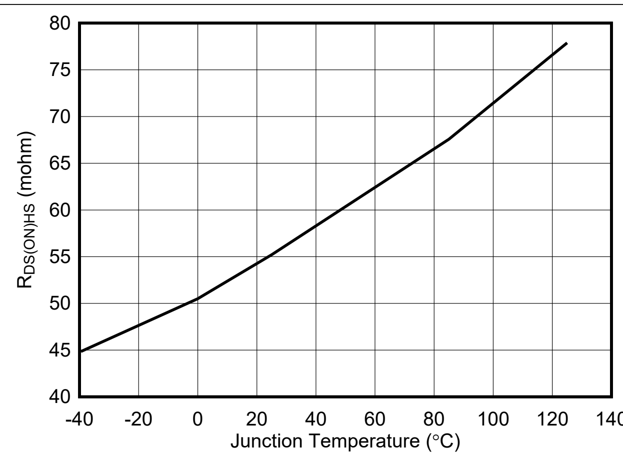

图 6-6. High-Side $R_{DS(ON)}$

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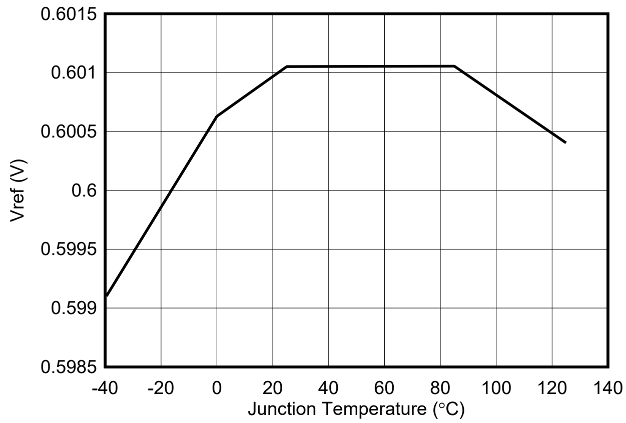

图 6-7. VREF Voltage

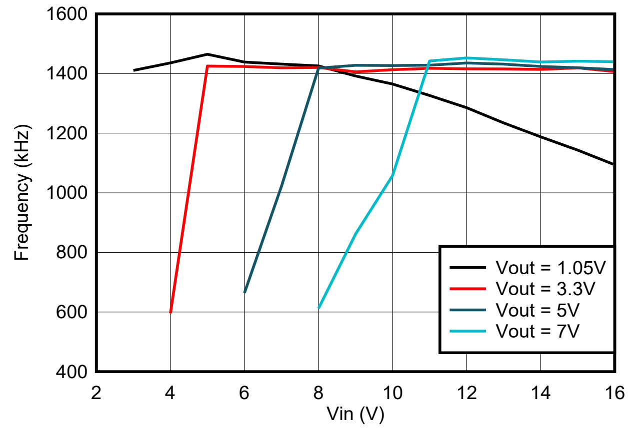

图 6-8. Frequency vs Input Voltage, I_{OUT} = 3 A

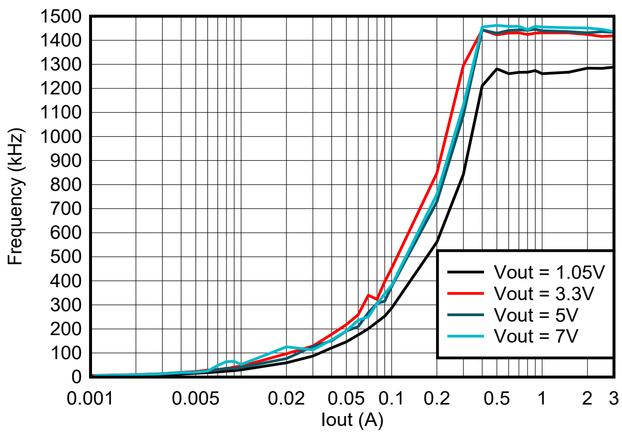

图 6-9. TPS563252 Frequency vs Loading, V_{IN} = 12 V

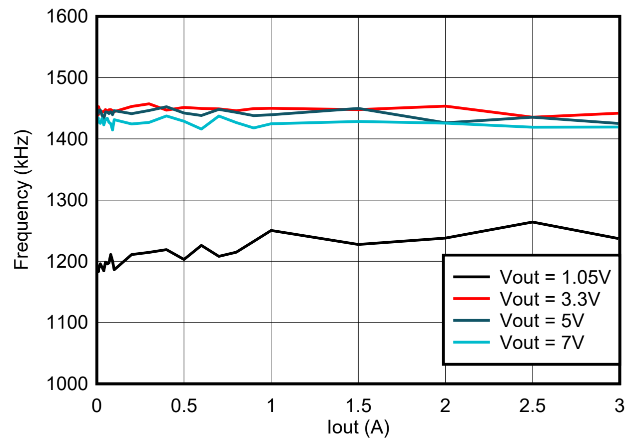

图 6-10. TPS563257 Frequency vs Loading, V_{IN} = 12 V

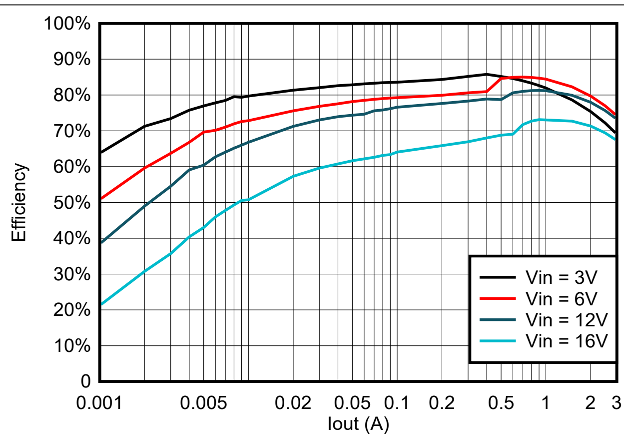

图 6-11. TPS563252 Efficiency at 0.6 V_{OUT} with a 0.68-μH Inductor

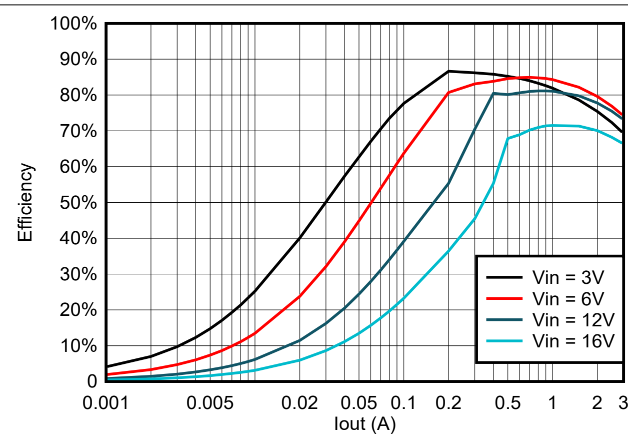

图 6-12. TPS563257 Efficiency at 0.6 V_{OUT} with a 0.68-μH Inductor

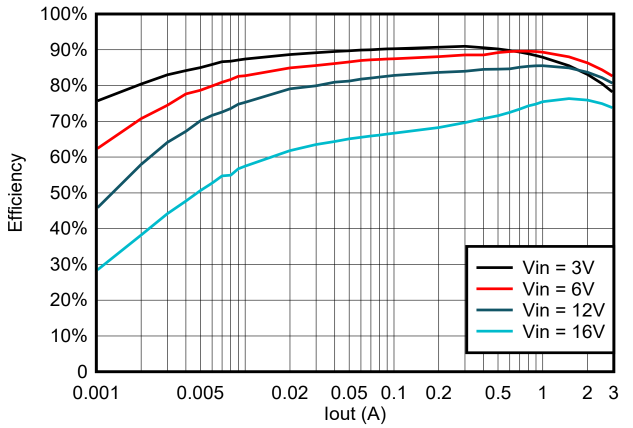

图 6-13. TPS563252 Efficiency at 1.05 V_{OUT} with a 0.82-µH Inductor

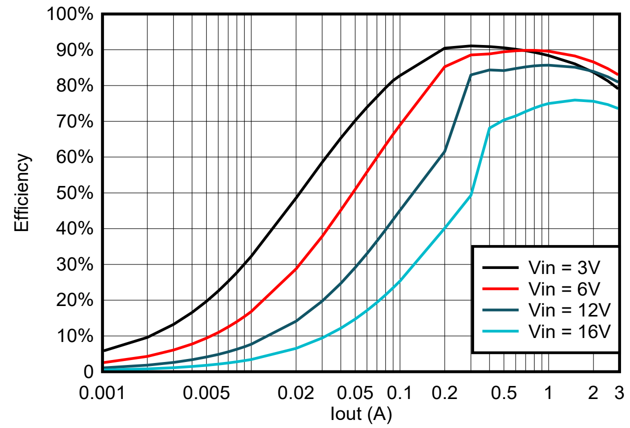

图 6-14. TPS563257 Efficiency at 1.05 V_{OUT} with a 0.82-µH Inductor

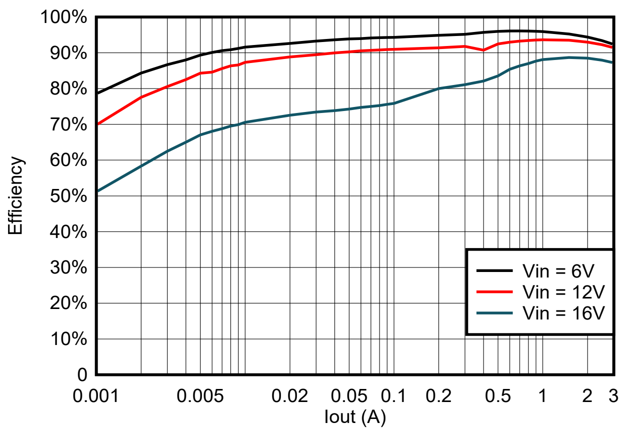

图 6-15. TPS563252 Efficiency at 3.3 V_{OUT} with a 2.2-µH Inductor

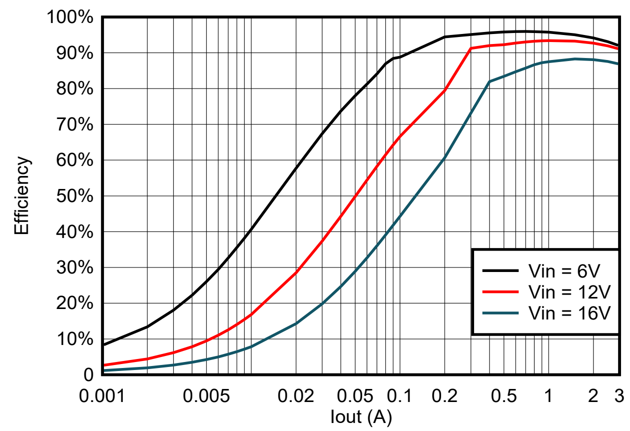

图 6-16. TPS563257 Efficiency at 3.3 V_{OUT} with a 2.2-µH Inductor

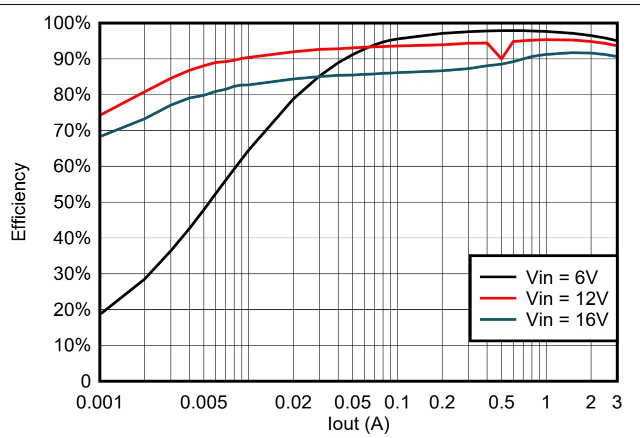

图 6-17. TPS563252 Efficiency at 5 V_{OUT} with a 2.2-µH Inductor

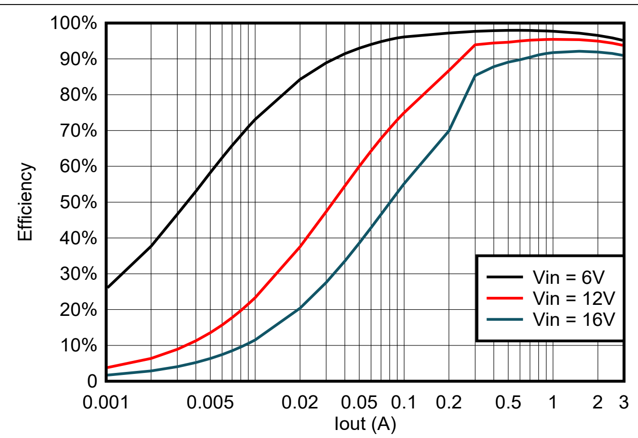

图 6-18. TPS563257 Efficiency at 5 V_{OUT} with a 2.2-µH Inductor

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7 Detailed Description

7.1 Overview

The TPS56325x is a 3-A integrated FET synchronous buck converter that operates from 3-V to 16-V input voltage and 0.6-V to 7-V output voltage. This device also integrates the BST pin in an internal IC, which is helpful for easy layout. The device employs a D-CAP3 topology that provides fast transient response with no external compensation components and an accurate feedback voltage. The proprietary D-CAP3 mode enables low external component count, ease of design, and optimization of the power design for cost, size, and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation mode at lighter load condition.

The Eco-mode version allows the TPS563252 to maintain high efficiency at light load. The FCCM version allows the TPS563257 to maintain a fixed switching frequency and lower voltage output ripple. The TPS56325x is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

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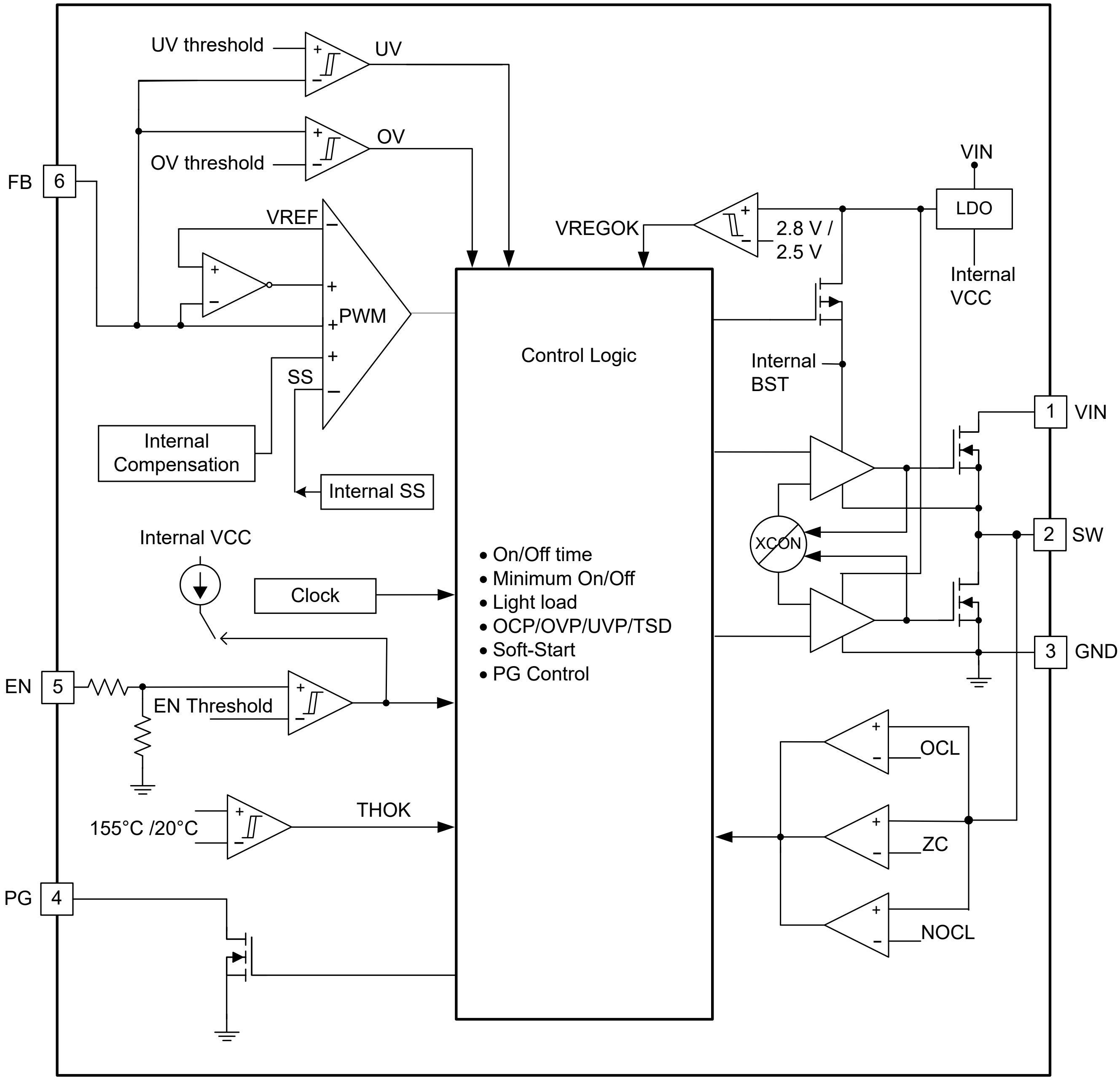
7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Operation and D-CAP3 Control

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3 mode control. The DCAP3 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The device is stable even with virtually no ripple at the output. The TPS56325x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage

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range, hence, it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to reference voltage to emulate the output ripple, enabling the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3 control topology.

7.3.2 Eco-Mode Control

The TPS563252 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 方程式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Prebiased Soft Start

The TPS56325x has an internal fixed 1.6-ms soft-start time. The EN default status is low. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage, V_{FB}. This scheme makes sure that the converter ramps up smoothly into the regulation point.

7.3.4 Overvoltage Protection

The TPS56325x has the overvoltage protection feature. When the output voltage becomes higher than the OVP threshold, the OVP is triggered in which, the deglitch time is 24 μs. Both the high-side MOSFET and the low-side MOSFET drivers are turned off. When the overvoltage condition is removed, the device returns to switching.

7.3.5 Large Duty Operation

The TPS56325x can support large duty operations up to 93% by smoothly dropping down the switching frequency. When V_{IN} / V_{OUT} < 1.6 and V_{FB} is lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make t_{ON} extended to implement the large duty operation and improve the performance of the load transient performance. Please refer frequency test waveform in 图 6-8. The minimum switching frequency is limited to approximately 600 kHz.

7.3.6 Current Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the off state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by the following:

- V_{IN}
- V_{OUT}
- On time
- Output inductor value

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current, I_{OUT}. If the monitored valley current is above the OCL level, the converter maintains a low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter, which can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it and the device shuts down after the UVP delay time (typically 256 µs) and restarts after the hiccup wait time (typically 14 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPS563257 is a FCCM mode part. In this mode, the device has negative inductor current at light loading. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When the NOC condition is removed, the device returns to normal switching.

Because the TPS563257 is a FCCM mode port, if the inductance is so small that the device trigger NOC, it causes the output voltage to be higher than target value. The minimum inductance is identified as 方程式 2.

$$L = \frac{V_{out} \times (1 - \frac{V_{out}}{V_{in}})}{2 \times Frequency \times NOC_{min}} \quad (2)$$

7.3.7 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This is a non-latch protection.

7.3.8 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value, the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Eco-mode Operation

The TPS563252 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction mode. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as it was in continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

7.4.2 FCCM Mode Operation

The TPS563257 operates in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load conditions and allows the inductor current to become negative. During FCCM mode, the switching frequency is maintained at an almost constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is a typical buck DC-DC converter that is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for TPS56325x. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in 图 8-1 was developed to meet the requirements in 表 8-1. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

图 8-1 shows the TPS56325x 12-V input, 1.05-V output converter schematic.

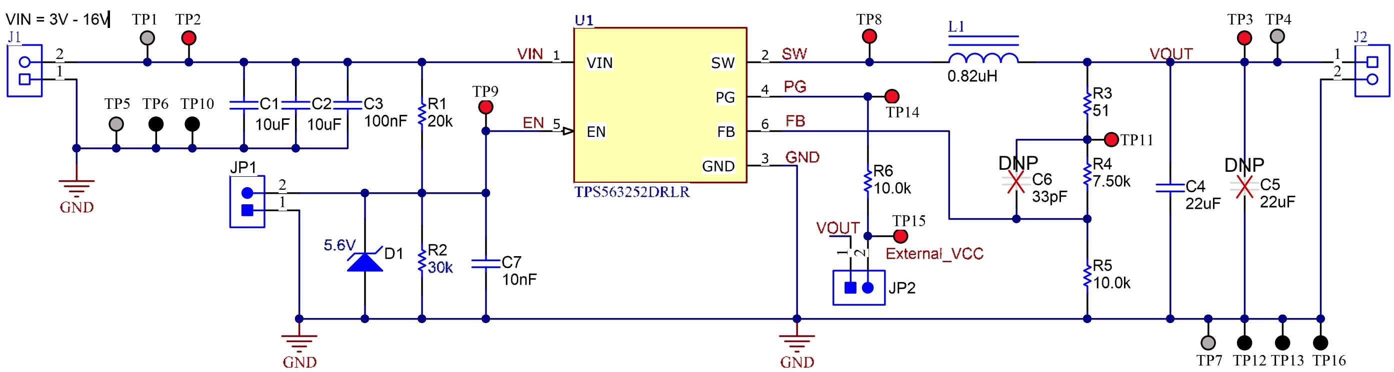

图 8-1. Schematic

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

Parameter		Conditions	MIN	TYP	MAX	Unit
V_{OUT}	Output voltage			1.05		V
I_{OUT}	Output current			3 A		A
ΔV_{OUT}	Transient response	0.3 A - 2.7 A load step, 0.8-A/μs slew rate		±3% × V_{OUT}		V
V_{IN}	Input voltage		3	12	16	V
$V_{OUT(ripple)}$	Output voltage ripple	CCM condition		20		mV
F_{SW}	Switching frequency			1.4 MHz		kHz
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Start by using 方程式 3 to calculate V_{OUT}.

To improve efficiency at very light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable. Use a 10-kΩ or 30-kΩ resistor for R_5 to start the design.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_4}{R_5}\right) \tag{3}$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has a double pole at 方程式 4. In this equation, C_{OUT} uses its effective value after derating, not its nominal value.

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

For any control topology that is compensated internally, there is a range of the output filter it can support. At low frequency, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops has a 180 degree drop. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40 dB to –20 dB per decade and leads the 90 degree phase boost. The internal ripple injection high-frequency zero is about 156 kHz. The inductor and capacitor selected for the output filter is recommended such that the double pole is located approximately 40 kHz, so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system should usually be targeted to be less than one-third of the switching frequency (f_{SW}).

表 8-2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	Minimum L1 (μH)	Typical L1 (μH)	Maximum L1 (μH)	Minimum C_{OUT} (μF)	Typical C_{OUT} (μF)	Maximum C_{OUT} (μF)	CFF (pF)
0.6	0	10.0	0.47	0.68	0.68	22	44	88	—
1.05	7.5	10.0	0.68	0.82	1	10	22	88	—
3.3	45.0	10.0	1.8	2.2	2.2	10	22	88	10-470
5	220.0	30.0	2.2	2.2	3.3	10	22	88	10-470
7	320.0	30.0	2.2	2.2	4.7	10	22	88	10-470

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 方程式 5, 方程式 6, and 方程式 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{lP-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{5}$$

$$I_{lPEAK} = I_O + \frac{I_{lP-P}}{2} \tag{6}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{lP-P}^2} \tag{7}$$

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For this design example, the calculated peak current is 3.4 A and the calculated RMS current is 3.01 A. The inductor used is 744383660082 with 8.8-A rated current and 11-A saturation current.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56325x are intended for use with ceramic or other low-ESR capacitors. Use 方程式 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (8)$$

For this design, one MuRata GRM21BR61A226ME44L 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.25 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS56325x requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor from the VIN pin to ground is recommended to provide high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

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8.2.3 Application Curves

The following data is tested with V_{IN} = 12 V, V_{OUT} = 1.05 V, T_A = 25°C, unless otherwise specified.

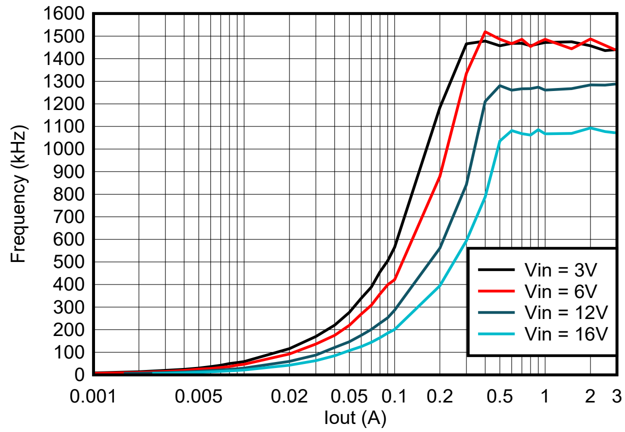

图 8-2. TPS563252 Frequency vs Loading

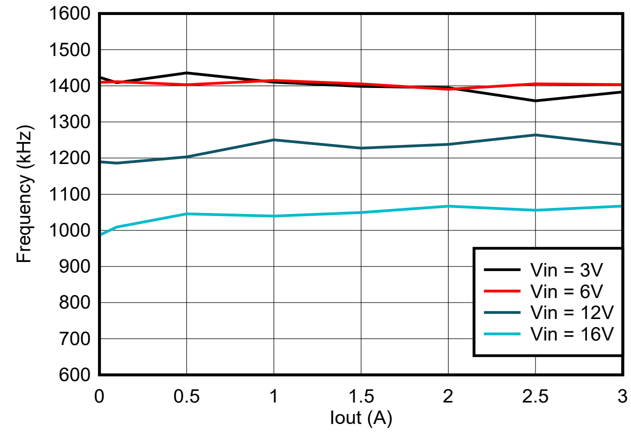

图 8-3. TPS563257 Frequency vs Loading

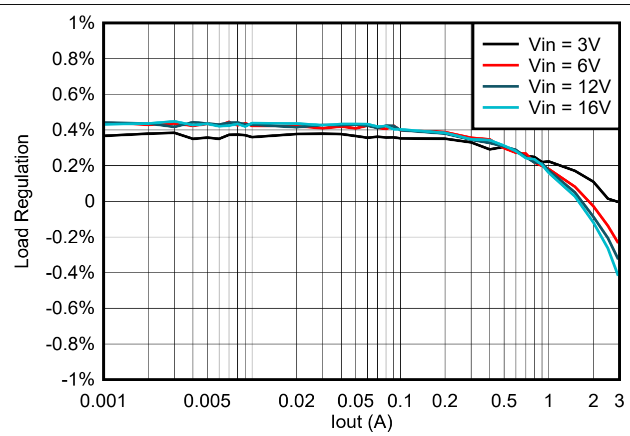

图 8-4. TPS563252 Load Regulation vs Loading

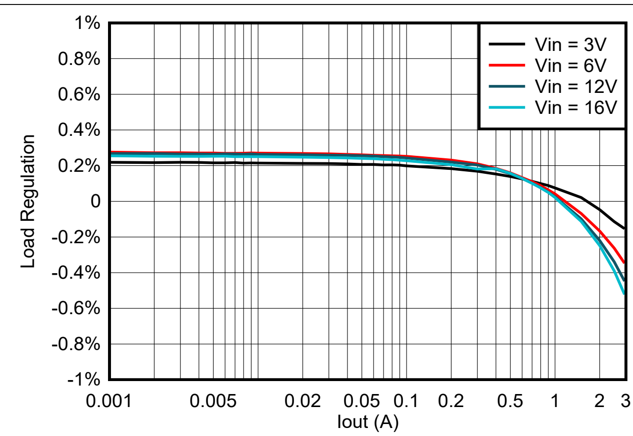

图 8-5. TPS563257 Load Regulation vs Loading

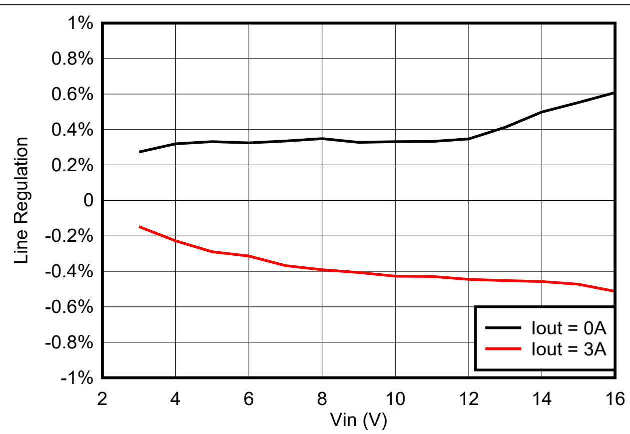

图 8-6. TPS563252 Line Regulation vs V_{IN}

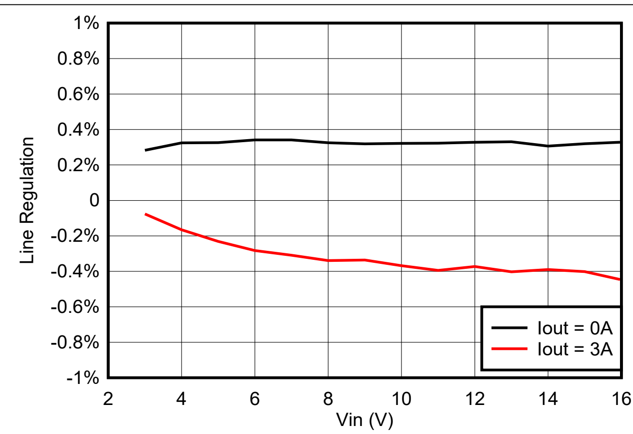

图 8-7. TPS563257 Line Regulation vs V_{IN}

ADVANCE INFORMATION

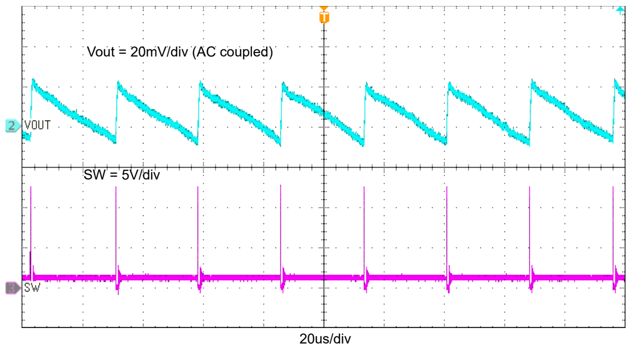

图 8-8. TPS563252 Output Voltage Ripple with 0.01-A Loading

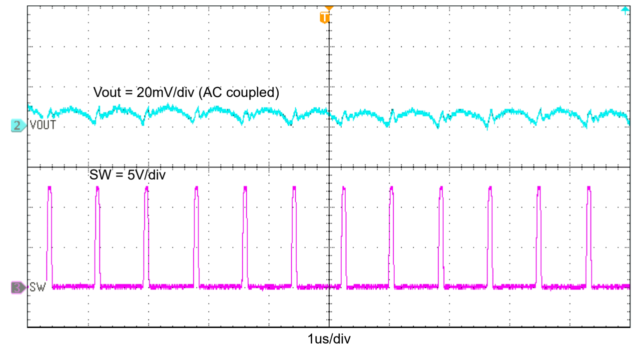

图 8-9. TPS563257 Output Voltage Ripple with 0.01-A Loading

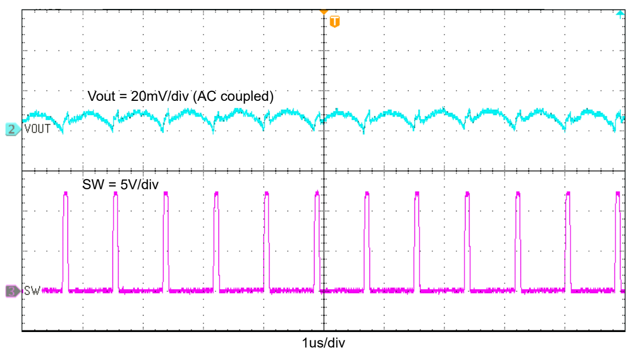

图 8-10. Output Voltage Ripple with 3-A Loading

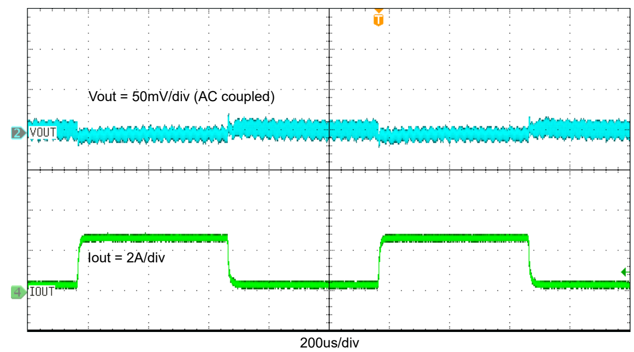

图 8-11. TPS563252 Transient Response with 0.3 A to 2.7 A

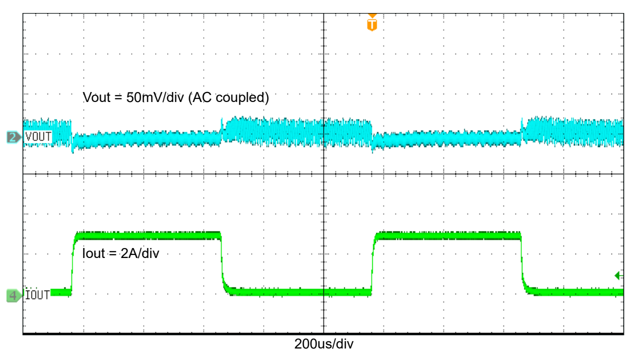

图 8-12. TPS563252 Transient Response with 0.1 A to 3 A

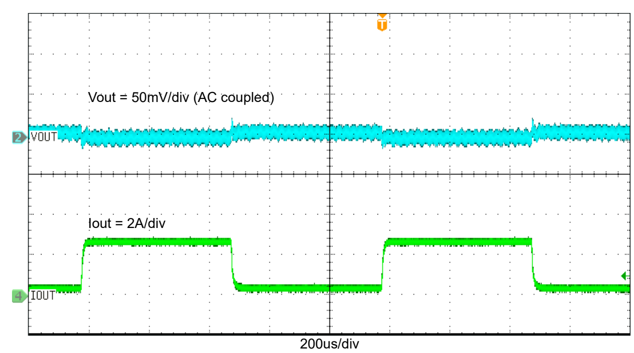

图 8-13. TPS563257 Transient Response with 0.3 A to 2.7 A

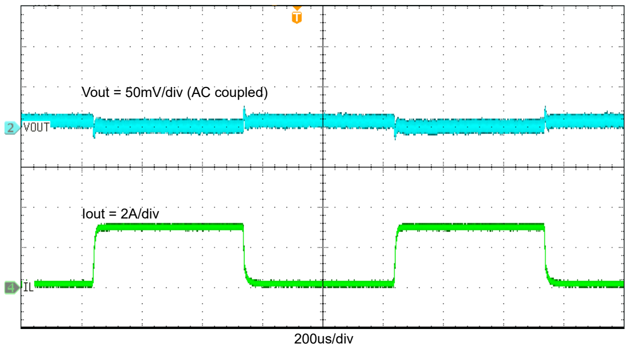

图 8-14. TPS563257 Transient Response with 0.1 A to 3 A

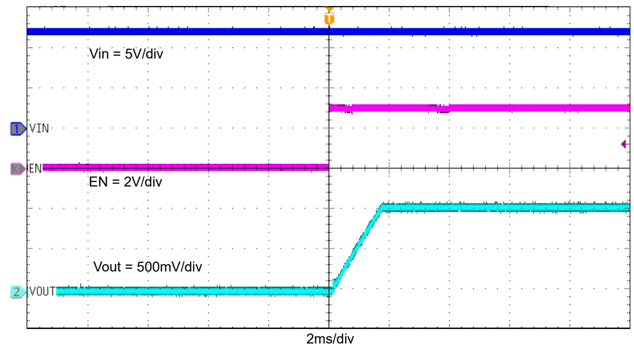

图 8-15. Start-Up Through EN, I_{OUT} = 3 A

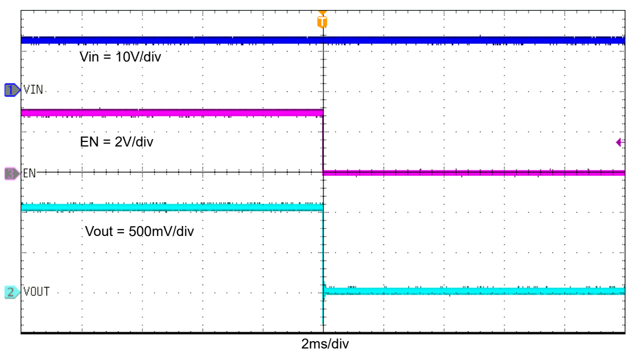

图 8-16. Shutdown Through EN, I_{OUT} = 3 A

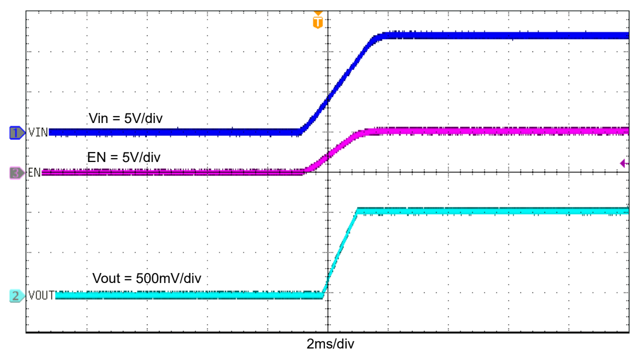

图 8-17. Start-Up with V_{IN} Rising, I_{OUT} = 3 A

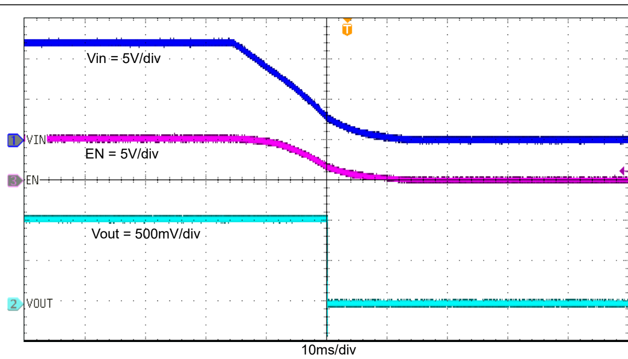

图 8-18. Shutdown with V_{IN} Falling, I_{OUT} = 3 A

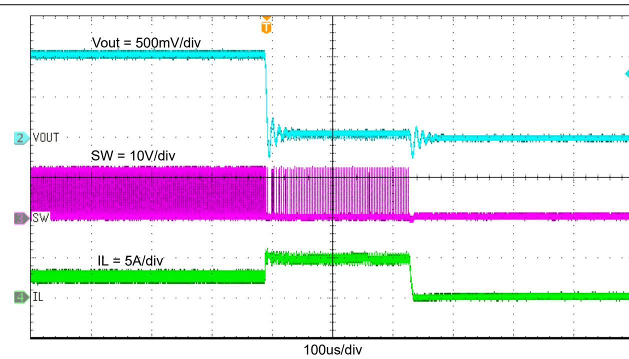

图 8-19. TPS563252 Normal Operation to Output Hard Short

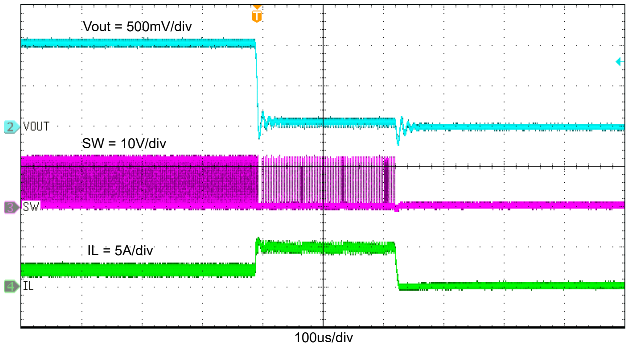

图 8-20. TPS563257 Normal Operation to Output Hard Short

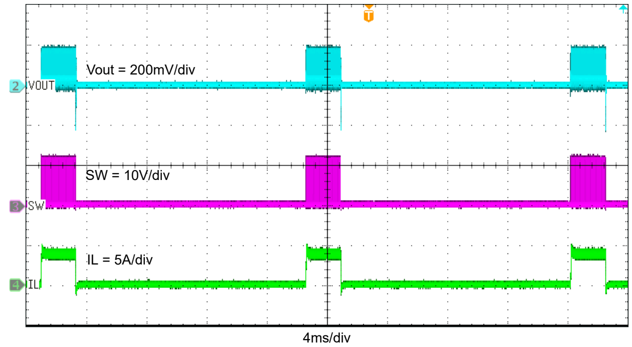

图 8-21. Output Hard Short Hiccup

ADVANCE INFORMATION

8.3 Power Supply Recommendations

The TPS56325x are designed to operate from input supply voltages in the range of 3 V to 16 V. Buck converters require the input voltage to be higher than the output voltage for proper operation.

8.4 Layout

8.4.1 Layout Guidelines

- VIN and GND traces must be as wide as possible to reduce trace impedance. The wide areas are also an advantage from the view point of heat dissipation.
- Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- Connect a separate VOUT path to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Place a voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the FB node must be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin must be as wide as possible to minimize its trace impedance.

8.4.2 Layout Example

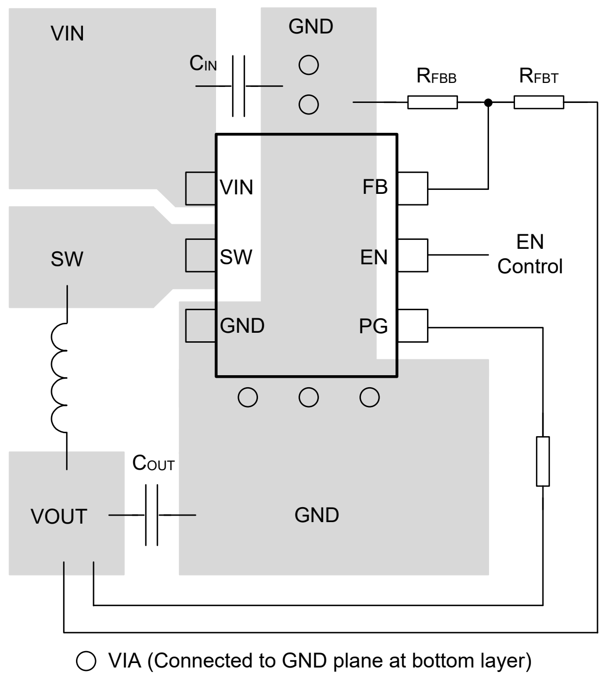

图 8-22. Suggested Layout

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 术语表

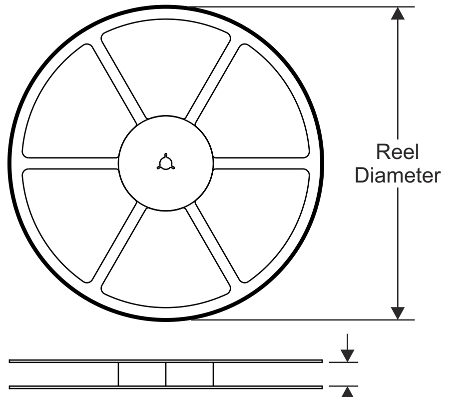
TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

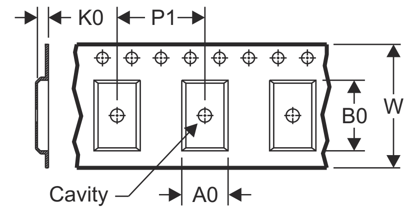
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

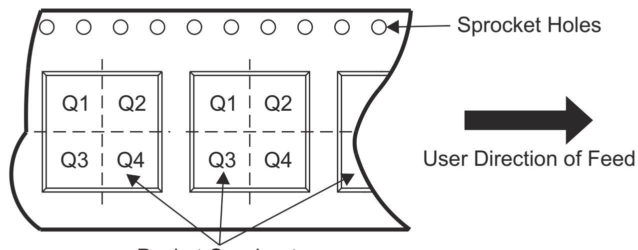


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

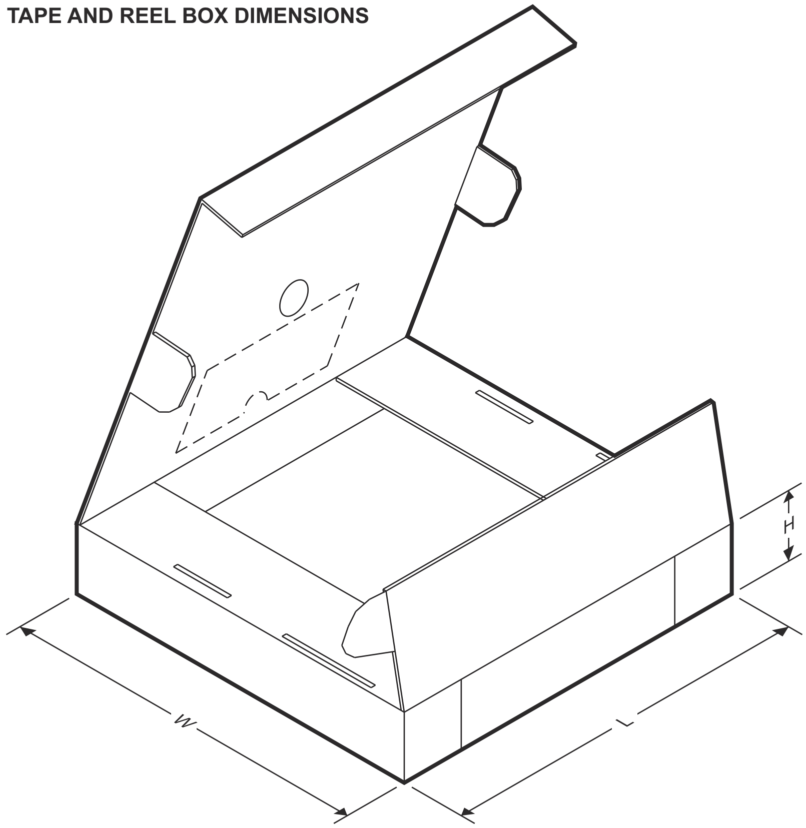
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS563252DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS563257DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS563252DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS563257DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XTPS563252DRLR	ACTIVE	SOT-5X3	DRL	6	4000	TBD	Call TI	Call TI	-40 to 125		Samples
XTPS563257DRLR	ACTIVE	SOT-5X3	DRL	6	4000	TBD	Call TI	Call TI	-40 to 125		Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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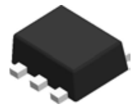
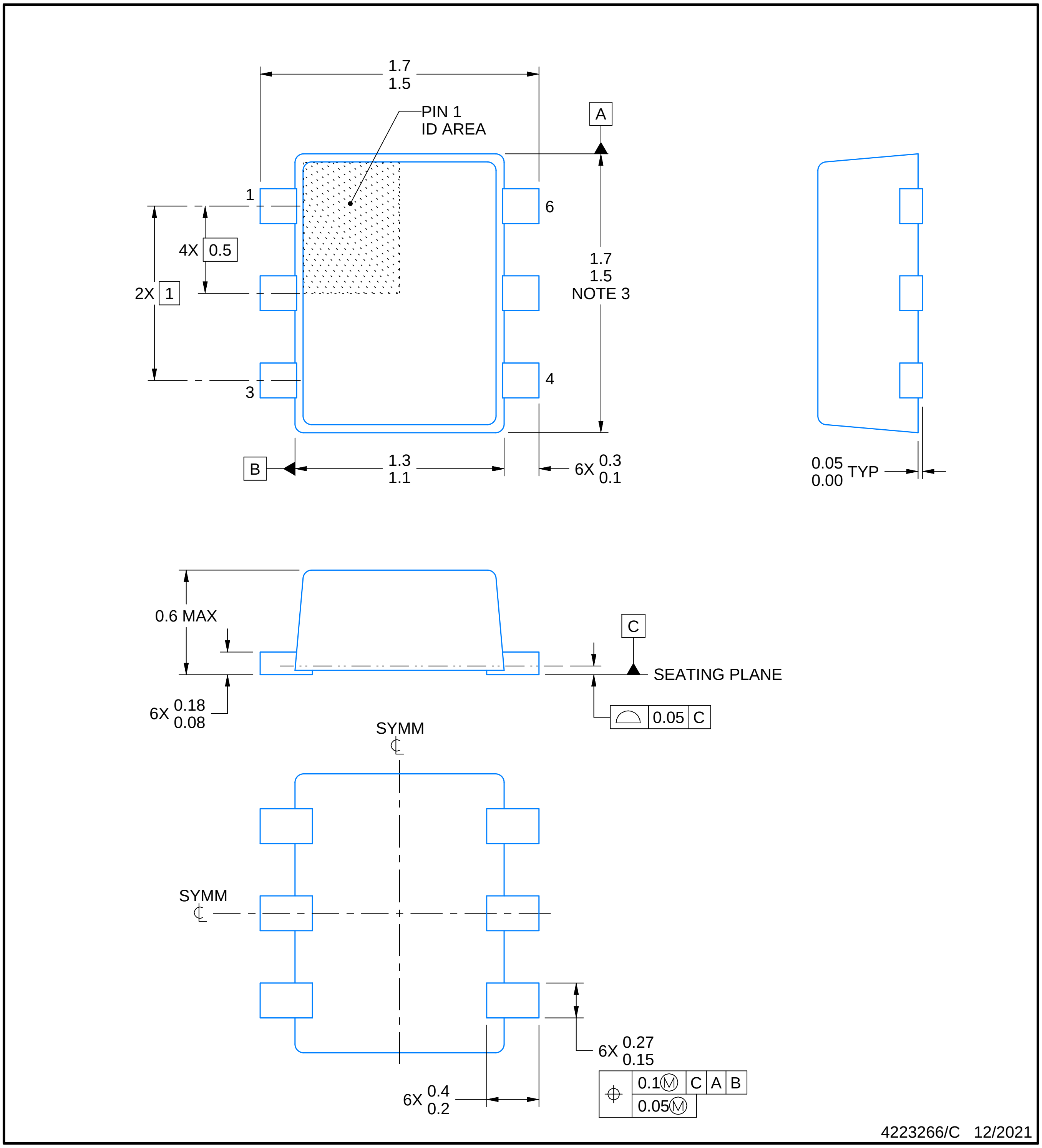
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



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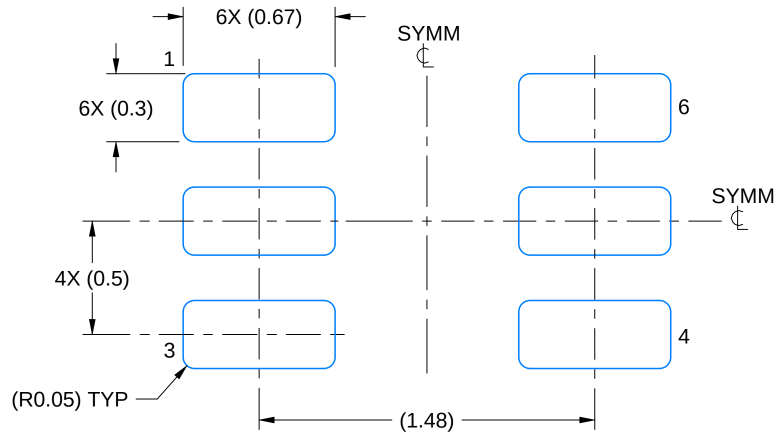
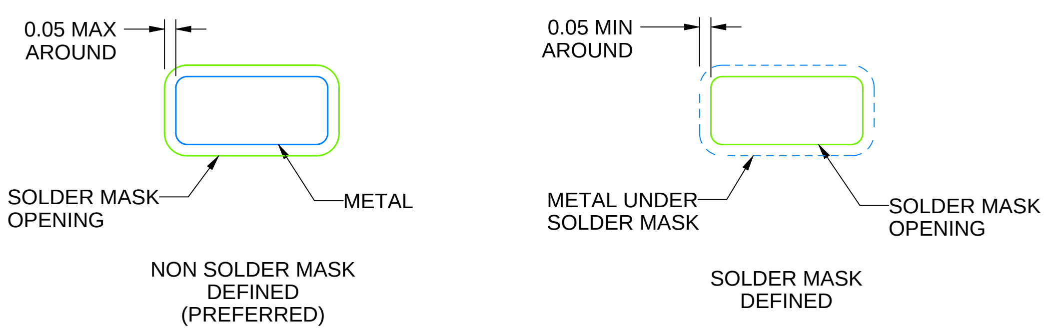
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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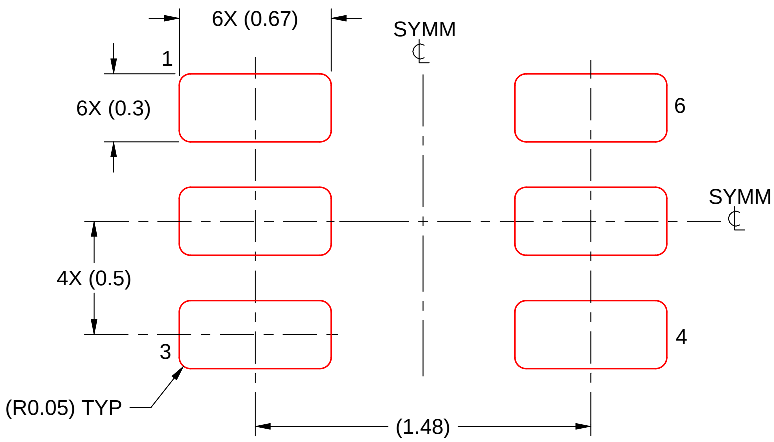
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.