

# TPS7H2201-SP 耐辐射 1.5V 至 7V、6A 负载开关

## 1 特性

- 辐射性能：
  - 抗辐射加固保障 (RHA) 高达 100krad (Si) TID
  - 单粒子锁定 (SEL)、单粒子烧毁 (SEB) 和单粒子栅穿 (SEGR) 对于 LET 的抗扰度 = 75MeV-cm<sup>2</sup>/mg
  - SEFI/SET 对于 LET 的额定值 = 75MeV-cm<sup>2</sup>/mg
- 集成型单通道负载开关
- 输入电压范围：1.5V 至 7V
- 低导通电阻 (R<sub>ON</sub>)，在温度为 25°C 和输入电压为 5V 时具有 35mΩ 的最大值
- 6A 最大持续开关电流
- 低控制输入阈值支持使用 1.2V、1.8V、2.5V 和 3.3V 逻辑器件
- 可配置上升时间（软启动）
- 反向电流保护
- 可编程和内部电流限制（快速跳变）
- 可编程故障计时器（电流限制和重试模式）
- 热关断
- 带散热垫的陶瓷封装

## 2 应用

- 航天卫星电源管理和配电
- 耐辐射电源树 应用
- 支持军用（-55°C 至 125°C）温度范围

## 3 说明

TPS7H2201-SP 是一款单通道负载开关，可提供用于最大限度地降低浪涌电流的可配置上升时间和反向电流保护。此器件包括一个 P 沟道 MOSFET，可在 1.5V 至 7V 的输入电压范围内运行并可支持 6A 的最大持续电流。此开关由一个开关输入 (EN) 控制，该输入能够直接连接至低电压控制信号。

TPS7H2201-SP 采用具有集成式散热垫的陶瓷封装，从而支持高功率耗散。该器件在自然通风环境下的额定运行温度范围为 -55°C 至 125°C。

器件信息<sup>(1)</sup>

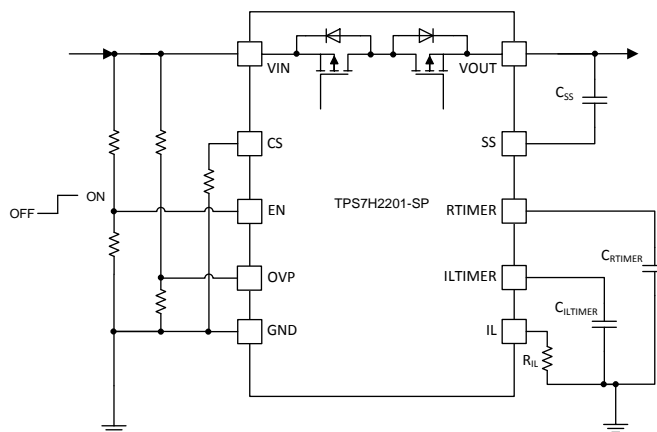
器件型号	等级	封装
5962R1722001VXC	耐辐射等级 RHA 100krad(Si)	16 引脚 CDFP 11.00 × 9.60mm 重量： 1.56g <sup>(3)</sup>
5962-1722001VXC	耐辐射等级 QMLV	
TPS7H2201HKR/EM	工程样片 <sup>(2)</sup>	
TPS7H2201EVM-CVAL	陶瓷评估板	EVM

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 这些部件仅适用于工程评估。部件按照不合规的流程进行加工处理。这些部件不适用于质检、生产、辐射测试或飞行。这些零部件无法在 -55°C 至 125°C 的完整 MIL 额定温度范围内或运行寿命中保证其性能。

(3) 重量误差在 ±10% 以内。

简化原理图



目录

1	特性 .....	1	8.3	Feature Description .....	17
2	应用 .....	1	8.4	Device Functional Modes .....	25
3	说明 .....	1	<b>9</b>	<b>Application and Implementation .....</b>	<b>26</b>
4	修订历史记录 .....	2	9.1	Application Information .....	26
5	<b>Pin Configuration and Functions .....</b>	<b>3</b>	9.2	Typical Applications .....	26
6	<b>Specifications .....</b>	<b>7</b>	<b>10</b>	<b>Power Supply Recommendations .....</b>	<b>31</b>
6.1	Absolute Maximum Ratings .....	7	<b>11</b>	<b>Layout .....</b>	<b>31</b>
6.2	ESD Ratings .....	7	11.1	Layout Guidelines .....	31
6.3	Recommended Operating Conditions .....	7	11.2	Layout Example .....	31
6.4	Thermal Information .....	8	<b>12</b>	<b>器件和文档支持 .....</b>	<b>32</b>
6.5	Electrical Characteristics .....	8	12.1	文档支持 .....	32
6.6	Switching Characteristics .....	10	12.2	接收文档更新通知 .....	32
6.7	Quality Conformance Inspection .....	10	12.3	社区资源 .....	32
6.8	Typical Characteristics .....	11	12.4	商标 .....	32
<b>7</b>	<b>Parameter Measurement Information .....</b>	<b>14</b>	12.5	静电放电警告 .....	32
<b>8</b>	<b>Detailed Description .....</b>	<b>16</b>	12.6	Glossary .....	32
8.1	Overview .....	16	<b>13</b>	<b>机械、封装和可订购信息 .....</b>	<b>33</b>
8.2	Functional Block Diagram .....	16			

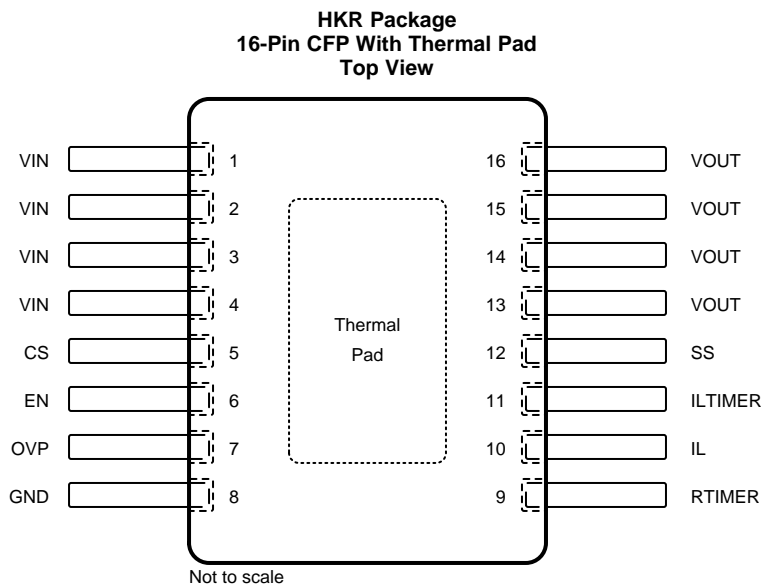
4 修订历史记录

Changes from Revision A (January 2019) to Revision B		Page
•	Added Bare Die Information table in <i>Pin Configuration and Functions</i> section .....	4
•	Added Bond Pad Coordinates in Microns table in <i>Pin Configuration and Functions</i> section .....	5
•	Added after TID specification for I <sub>SD</sub> VIN .....	8
•	已添加 Quality Conformance Inspection table to <i>Specifications</i> section .....	10

Changes from Original (September 2018) to Revision A		Page
•	已更改 将器件状态从高级信息 更改为生产数据 .....	1

## 5 Pin Configuration and Functions



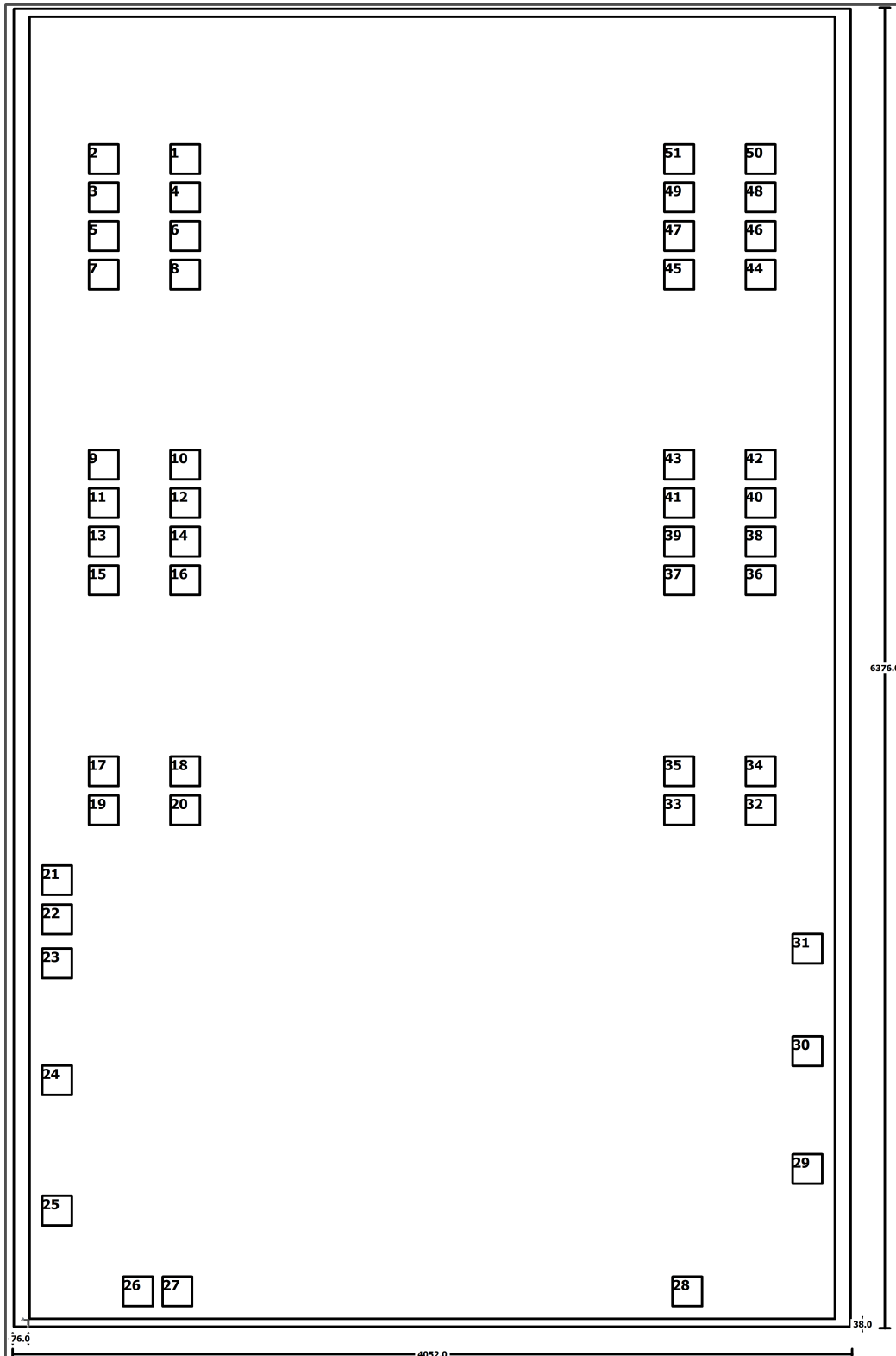
### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing $V_{IN}$ dip.
2			
3			
4			
5	CS	O	Current sense pin proportional to output current. Connect a resistor to GND.
6	EN	I	Active high switch control input. Do not leave floating.
7	OVP	I	Overvoltage protection. Programmable using an external resistor divider. If no OVP is desired, this pin should be connected to GND.
8	GND	—	Device ground. <sup>(1)</sup>
9	RTIMER	I/O	Capacitor programmed fault timer control during disabled and retry mode. Connecting this pin to GND holds the switch disabled until the EN pin is cycled. Do not float this pin or connect it to VIN.
10	IL	I/O	Current limiter control. Programmable using an external resistor to GND. Do not float this pin.
11	ILTIMER	I	Capacitor programmed fault timer control during current limiting mode. Connecting this pin to VIN uses the internal current limit timer and connecting this pin to GND disables the internal timer functionality for the ILTIMER as well as retry mode. In this case, the device will remain at programmed current limit indefinitely in the event of a short without going into retry mode. Do not float this pin.
12	SS	I/O	Switch slew rate control. See the <a href="#">Adjustable Rise Time</a> section for more information.
13	VOUT	O	Switch output. A minimum 10- $\mu$ F output capacitor is recommended.
14			
15			
16			
—	Thermal Pad	—	Thermal pad (exposed center pad) for heat dissipation purposes. Thermal pad is internally connected to seal ring and GND.

(1) Thermal pad is internally connected to the seal ring and GND.

**Table 1. Bare Die Information**

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	ALCU	1050 nm



**Table 2. Bond Pad Coordinates in Microns**

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VIN	1	679.75	5529	835.25	5684.5
VIN	2	286.85	5529	442.35	5684.5
VIN	3	286.85	5343.5	442.35	5499
VIN	4	679.75	5343.5	835.25	5499
VIN	5	286.85	5157.1	442.35	5312.6
VIN	6	679.75	5157.1	835.25	5312.6
VIN	7	286.85	4970.65	442.35	5126.15
VIN	8	679.75	4970.65	835.25	5126.15
VIN	9	286.85	4053	442.35	4208.5
VIN	10	679.75	4053	835.25	4208.5
VIN	11	286.85	3867.5	442.35	4023
VIN	12	679.75	3867.5	835.25	4023
VIN	13	286.85	3681.1	442.35	3836.6
VIN	14	679.75	3681.1	835.25	3836.6
VIN	15	286.85	3494.65	442.35	3650.15
VIN	16	679.75	3494.65	835.25	3650.15
VIN	17	286.85	2572.85	442.35	2728.35
VIN	18	679.75	2572.85	835.25	2728.35
VIN	19	286.85	2384.85	442.35	2540.35
VIN	20	679.75	2384.85	835.25	2540.35
AVDD	21	61.1	2046.7	216.6	2202.2
AVDD	22	61.1	1857.2	216.6	2012.7
CS	23	61.1	1645.3	216.6	1800.8
EN	24	61.1	1080.75	216.6	1236.25
OVP	25	61.1	451.4	216.6	606.9
GND	26	452.45	61.1	607.95	216.6
GND	27	641.95	61.1	797.45	216.6
RTIMER	28	3103.2	61.1	3258.7	216.6
IL	29	3683.4	652.7	3838.9	808.2
ILTIMER	30	3683.4	1221.4	3838.9	1376.9
SS	31	3683.4	1715.65	3838.9	1871.15
VOUT	32	3457.4	2384.85	3612.9	2540.35
VOUT	33	3064.5	2384.85	3220	2540.35
VOUT	34	3457.4	2572.85	3612.9	2728.35
VOUT	35	3064.5	2572.85	3220	2728.35
VOUT	36	3457.4	3494.65	3612.9	3650.15
VOUT	37	3064.5	3494.65	3220	3650.15
VOUT	38	3457.4	3681.1	3612.9	3836.6
VOUT	39	3064.5	3681.1	3220	3836.6
VOUT	40	3457.4	3867.5	3612.9	4023
VOUT	41	3064.5	3867.5	3220	4023
VOUT	42	3457.4	4053	3612.9	4208.5
VOUT	43	3064.5	4053	3220	4208.5
VOUT	44	3457.4	4970.65	3612.9	5126.15
VOUT	45	3064.5	4970.65	3220	5126.15
VOUT	46	3457.4	5157.1	3612.9	5312.6
VOUT	47	3064.5	5157.1	3220	5312.6

**Table 2. Bond Pad Coordinates in Microns (continued)**

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
VOUT	48	3457.4	5343.5	3612.9	5499
VOUT	49	3064.5	5343.5	3220	5499
VOUT	50	3457.4	5529	3612.9	5684.5
VOUT	51	3064.5	5529	3220	5684.5

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	−0.3	7.5	V
V <sub>OUT</sub>	Output voltage	−0.3	7.5	V
EN, OVP	Enable and over voltage protection pins	−0.3	7.5	V
CS, ILTIMER, RTIMER, IL, SS	Current sense, current limit timer, retry timer, current limit and soft start pins	−0.3	V <sub>IN</sub> + 0.3	V
I <sub>MAX</sub>	Maximum continuous switch current		9	A
I <sub>PLS</sub>	Maximum pulsed switch current (t <sub>≤5</sub> μs)		45	A
T <sub>J</sub>	Maximum junction temperature	−55	150	°C
T <sub>stg</sub>	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	1.5	7	V
SR <sub>VIN</sub>	Input voltage slew rate		0.01	V/μs
V <sub>OUT</sub>	Output voltage	0	V <sub>IN</sub>	V
I <sub>MAX</sub>	Maximum continuous switch current		6	A
T <sub>J</sub>	Operating junction temperature <sup>(1)</sup>	−55	125	°C

- (1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> − (θ<sub>JA</sub> × P<sub>D(max)</sub>).

## 6.4 Thermal Information

THERMAL METRIC		TPS7H2201-SP	
		HKR (CFP)	
		16 PINS	
R <sub>JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	0.6	°C/W

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SUBGROUP <sup>(1)</sup>	MIN	TYP	MAX	UNIT
<b>POWER SUPPLIES AND CURRENTS</b>							
V <sub>INHU</sub> V <sub>LO</sub>	Internal VIN UVLO voltage, rising				1.32		V
V <sub>INLU</sub> V <sub>LO</sub>	Internal VIN UVLO voltage, falling				1.23		V
HYST <sub>VIN-UVLO</sub>	Internal VIN UVLO hysteresis				92		mV
I <sub>Q</sub>	Quiescent current	I <sub>OUT</sub> = 0 mA, V <sub>IN</sub> = EN = 5 V, CS resistor of 20 kΩ to GND	1, 2, 3		2.4	6.5	mA
I <sub>F</sub>	VIN to VOUT forward leakage current	EN = VOUT = GND, measured VOUT current	1, 2, 3			3	mA
I <sub>SD</sub> VIN	VIN off-state supply current	EN = GND, I <sub>OUT</sub> = 0 mA, measured VIN current	VIN = 5 V	1, 2, 3	0.4	3	mA
			VIN = 3.3 V	1, 2, 3	0.3	3	
			VIN = 1.8 V	1, 2, 3	0.2	3	
			After TID = 100 krad, VIN = 1.8, 3.3, and 5 V	1		3.1	
I <sub>RCP</sub>	Reverse current protection leakage current	EN = 0 V, VIN = 0 to 7 V, VOUT = 0 to 7 V for VOUT > VIN	1, 2, 3		0.45	2.5	mA
		EN = 7 V, VIN = 0 V, VOUT = 0 to 7 V					
<b>SOFT START</b>							
I <sub>SS</sub>	Soft start charge current	1 V on SS pin	1, 2, 3		65	83	μA
SR <sub>SS</sub>	Soft start slew rate	SS pin floating, C <sub>OUT</sub> = 10 μF			295		mV/μs
<b>ENABLE AND UNDERVOLTAGE LOCKOUT (EN/UVLO) INPUT</b>							
V <sub>IHEN</sub>	EN/UVLO threshold voltage, rising		1, 2, 3	0.56	0.61	0.65	V
V <sub>ILEN</sub>	EN/UVLO threshold voltage, falling		1, 2, 3	0.47	0.51	0.55	V
HYST <sub>EN</sub>	EN/UVLO hysteresis voltage		1, 2, 3		93	124	mV
t <sub>LOW</sub>	EN signal low time during cycling	RTIMER = GND, I <sub>L</sub> = 1 A, I <sub>VOUT</sub> = 2 A	9, 10, 11	20			μs
V <sub>INEN</sub>	VIN percentage for enable		4, 5, 6	75%			
I <sub>EN</sub>	EN pin input leakage current	EN = VIN = 5 V	1, 2, 3			12	nA
<b>OVERVOLTAGE PROTECTION (OVP)</b>							
V <sub>OVP</sub> R	OVP threshold voltage, rising		1, 2, 3	0.52	0.57	0.63	V
V <sub>OVP</sub> F	OVPF threshold voltage, falling		1, 2, 3	0.5	0.55	0.59	V
HYST <sub>OVP</sub>	OVP hysteresis voltage	1.6 V < VIN < 7 V	1, 2, 3		20	55	mV
I <sub>OVP</sub>	OVP pin input leakage current		1, 2, 3			15	nA
<b>CURRENT LIMIT AND CURRENT SENSE</b>							
t <sub>CSEN</sub>	Time for valid CS output after enable	C <sub>SS</sub> = 120 nF	9, 10, 11			5	ms
Minimum VOUT current for valid CS output			1, 2, 3	750			mA
VOUT current change to CS change delay time		0.5-A rising step, 100 mA/μs, 1.5 V ≤ VIN ≤ 7 V	9, 10, 11		16	74	μs
VOUT current change to CS change delay time		0.5-A falling step, 100 mA/μs, 1.5 V ≤ VIN ≤ 7 V	9, 10, 11		16	73	μs
CS pin accuracy		0.75 A ≤ I <sub>VOUT</sub> ≤ 7.5 A	4, 5, 6	-10%		10%	
CS pin voltage		0.75 A ≤ I <sub>VOUT</sub> ≤ 7.5 A, no OCP	1, 2, 3			V <sub>IN</sub> - 0.4	V

 (1) For subgroup definitions, see [Quality Conformance Inspection](#) table.



## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SUBGROUP <sup>(1)</sup>	MIN	TYP	MAX	UNIT	
Current limit setting, $I_{LL}$		$I_{VOUT} \leq 1 \text{ A}$	1, 2, 3	$I_{VOUT} + 0.5$			A	
		$1 \text{ A} < I_{VOUT} \leq 3 \text{ A}$	1, 2, 3	$I_{VOUT} + 1$				
		$I_{VOUT} > 3 \text{ A}$	1, 2, 3	$I_{VOUT} + 1.5$				
Programmable current limit accuracy		$1.5 \text{ V} \leq V_{IN} \leq 7 \text{ V}$	4, 5, 6	-20%		20%		
Fast trip off current limit		$V_{IN} = 5 \text{ V}$ , 10-m $\Omega$ short in 10 $\mu\text{s}$			22		A	
Fast trip off off-time		$V_{IN} = 5 \text{ V}$ , $C_{SS} = 2.7 \text{ nF}$	9, 10, 11		61	158	$\mu\text{s}$	
Internal current limit timer (fast trip off current limit)		$V_{IN} = 5 \text{ V}$ , $I_{VOUT} = 3 \text{ A}$ , $I_L = 6 \text{ A}$ , $ILTIMER = V_{IN}$ , 10-m $\Omega$ short in 10 $\mu\text{s}$	9, 10, 11		15	35	$\mu\text{s}$	
<b>TIMERS</b>								
$I_{LTIMER}$	ILTIMER charge current		1, 2, 3	0.7	1	1.38	$\mu\text{A}$	
$PD_{LTIMER}$	ILTIMER internal pull-down resistance	40 mV on ILTIMER pin	1, 2, 3		38	153	$\Omega$	
$I_{RTIMER}$	RTIMER charge current		1, 2, 3	0.7	1	1.38	$\mu\text{A}$	
$PD_{RTIMER}$	RTIMER internal pull-down resistance	40 mV on RTIMER pin	1, 2, 3		38	153	$\Omega$	
<b>THERMAL SHUTDOWN</b>								
Thermal shutdown		$V_{IN} = 5 \text{ V}$			175		$^{\circ}\text{C}$	
Thermal shutdown hysteresis		$V_{IN} = 5 \text{ V}$			20		$^{\circ}\text{C}$	
<b>RESISTANCE CHARACTERISTICS</b>								
$R_{ON}$	ON-state resistance, lead length = 2.5 mm	$V_{IN} = 7 \text{ V}$ , $I_{LL} = 7.5 \text{ A}$	-55 $^{\circ}\text{C}$	1, 2, 3			24	m $\Omega$
			-40 $^{\circ}\text{C}$				26	
			25 $^{\circ}\text{C}$			31	34	
			85 $^{\circ}\text{C}$			37	40	
			125 $^{\circ}\text{C}$			41	45	
		$V_{IN} = 5 \text{ V}$ , $I_{LL} = 7.5 \text{ A}$	-55 $^{\circ}\text{C}$	1, 2, 3			26	
			-40 $^{\circ}\text{C}$				27	
			25 $^{\circ}\text{C}$			32	35	
			85 $^{\circ}\text{C}$			39	42	
			125 $^{\circ}\text{C}$			43	47	
		$V_{IN} = 3.3 \text{ V}$ , $I_{LL} = 7.5 \text{ A}$	-55 $^{\circ}\text{C}$	1, 2, 3			28	
			-40 $^{\circ}\text{C}$				30	
			25 $^{\circ}\text{C}$			35	38	
			85 $^{\circ}\text{C}$			42	46	
			125 $^{\circ}\text{C}$			47	52	
		$V_{IN} = 1.8 \text{ V}$ , $I_{LL} = 7.5 \text{ A}$	-55 $^{\circ}\text{C}$	1, 2, 3			36	
			-40 $^{\circ}\text{C}$				39	
			25 $^{\circ}\text{C}$			45	51	
			85 $^{\circ}\text{C}$			55	62	
			125 $^{\circ}\text{C}$			61	70	
		$V_{IN} = 1.5 \text{ V}$ , $I_{LL} = 7.5 \text{ A}$	-55 $^{\circ}\text{C}$	1, 2, 3			44	
			-40 $^{\circ}\text{C}$				48	
			25 $^{\circ}\text{C}$			52	63	
			85 $^{\circ}\text{C}$			63	77	
125 $^{\circ}\text{C}$			70		87			

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

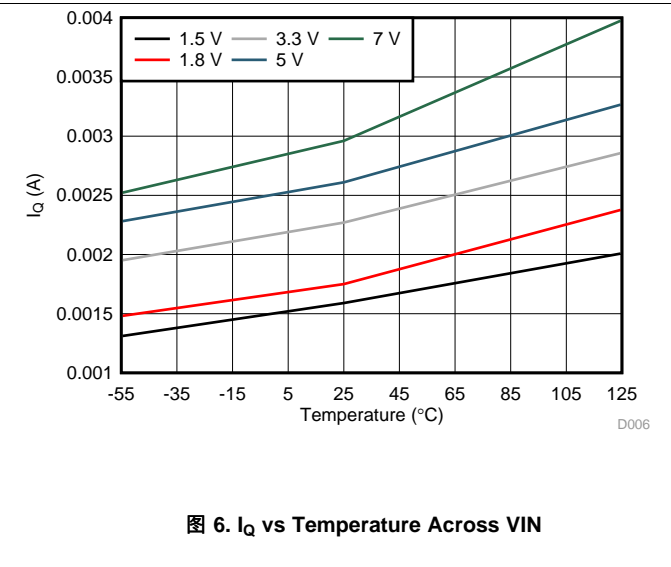
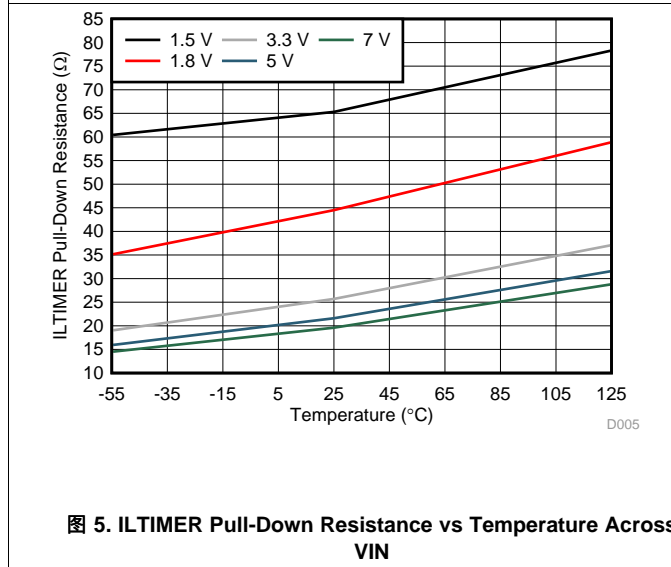
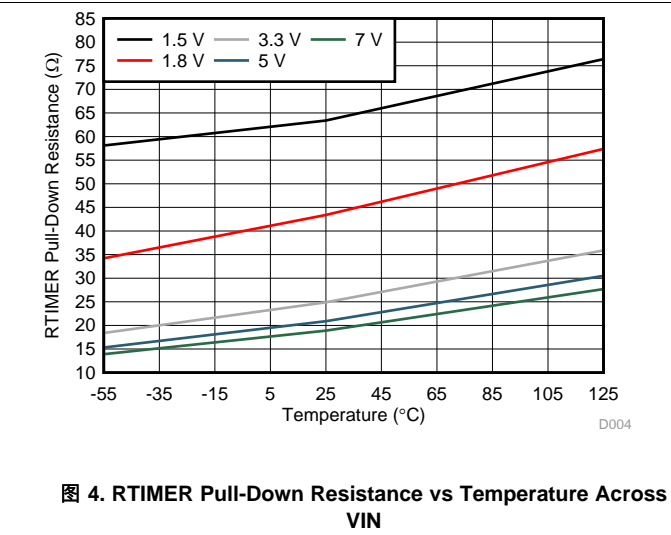
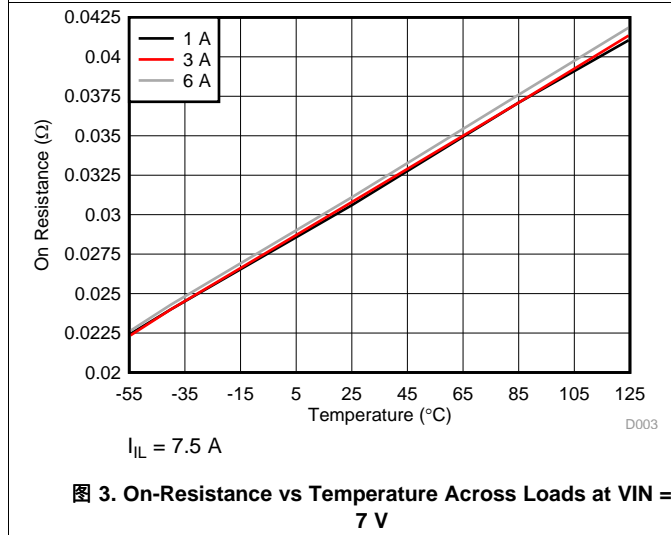
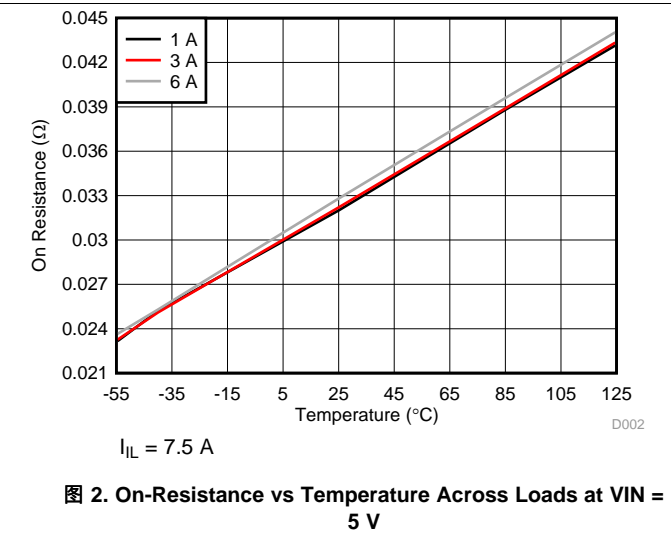
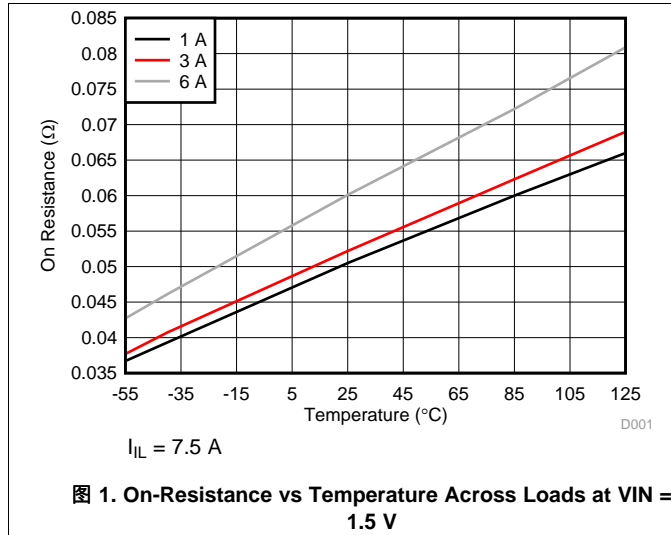
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>V<sub>IN</sub> = EN = 5 V, T<sub>A</sub> = 25°C (unless otherwise noted)</b>						
t <sub>ON</sub>	Turn-on time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		208		μs
t <sub>OFF</sub>	Turn-off time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		60		μs
t <sub>F</sub>	VO <sub>UT</sub> fall time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		90		μs
t <sub>ASSERT</sub>	OVP assert time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		4.5		μs
t <sub>DEASSERT</sub>	OVP deassert time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		9.6		μs
<b>V<sub>IN</sub> = EN = 1.5 V, T<sub>A</sub> = 25°C (unless otherwise noted)</b>						
t <sub>ON</sub>	Turn-on time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		173		μs
t <sub>OFF</sub>	Turn-off time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		64		μs
t <sub>F</sub>	VO <sub>UT</sub> fall time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		70		μs
t <sub>ASSERT</sub>	OVP assert time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		2.65		μs
t <sub>DEASSERT</sub>	OVP deassert time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 10 μF, C <sub>SS</sub> = 1000 pF		6.56		μs

## 6.7 Quality Conformance Inspection

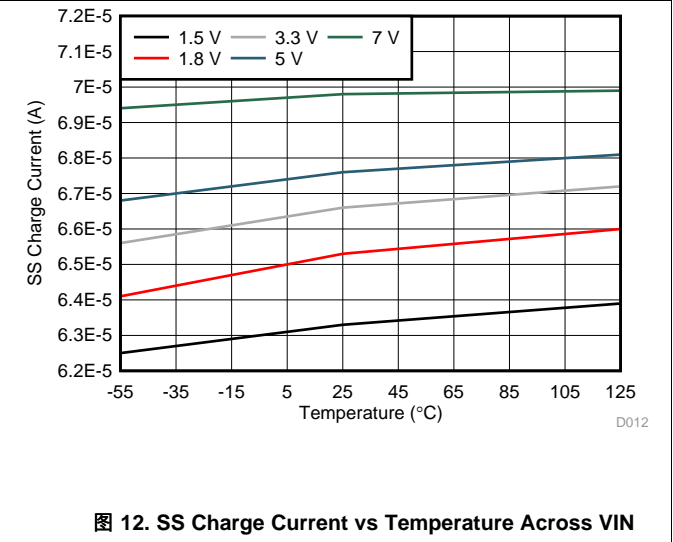
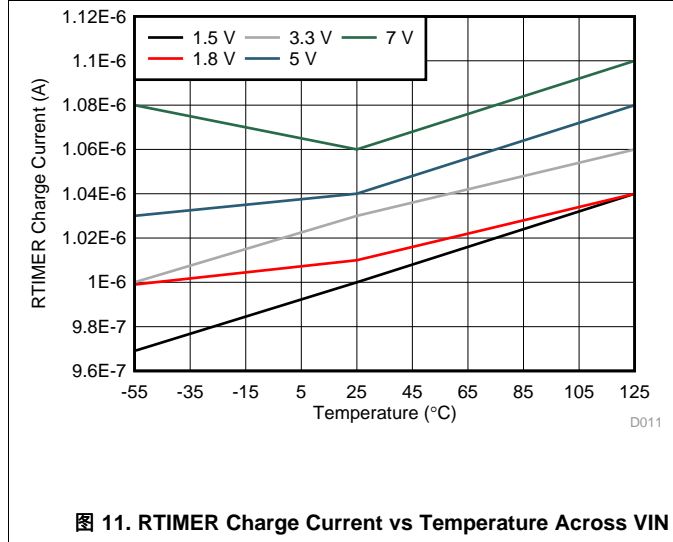
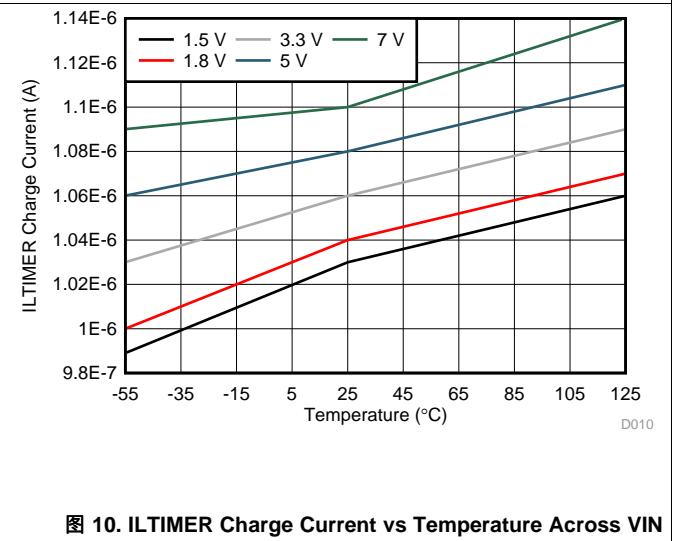
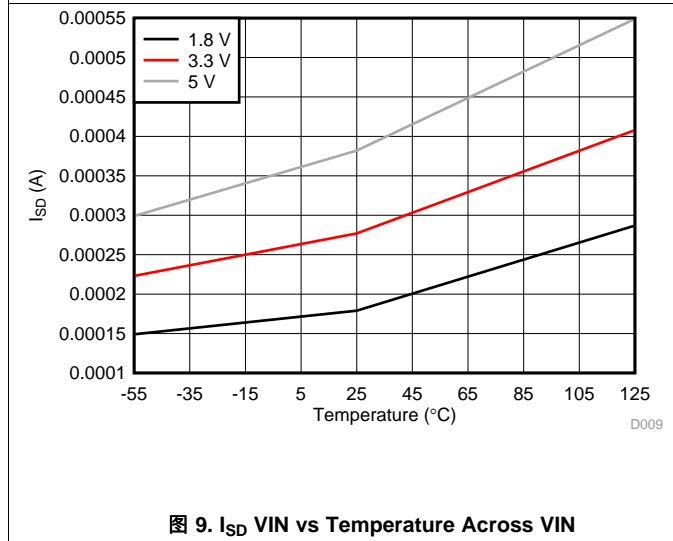
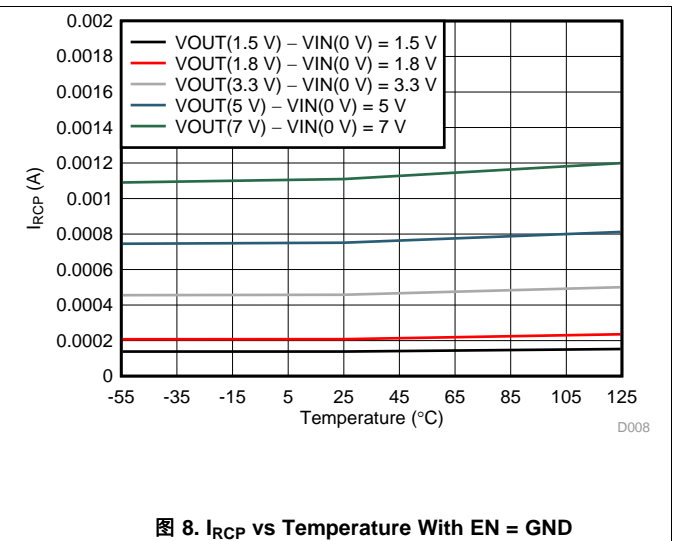
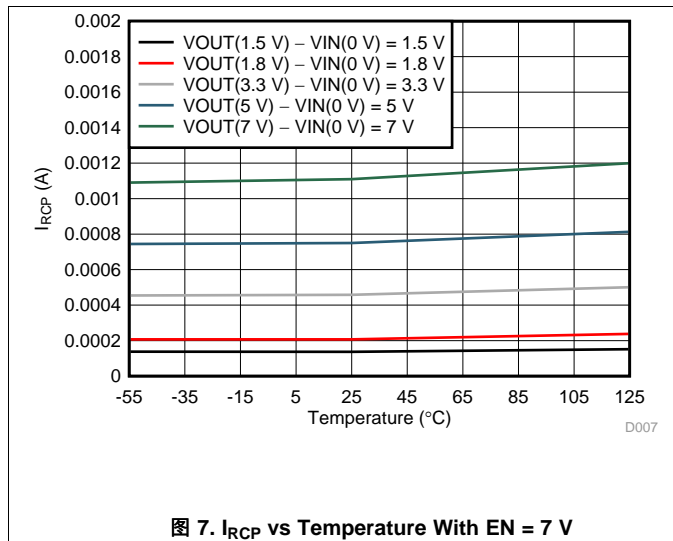
MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

### 6.8 Typical Characteristics



Typical Characteristics ( 接下页 )



Typical Characteristics (接下页)

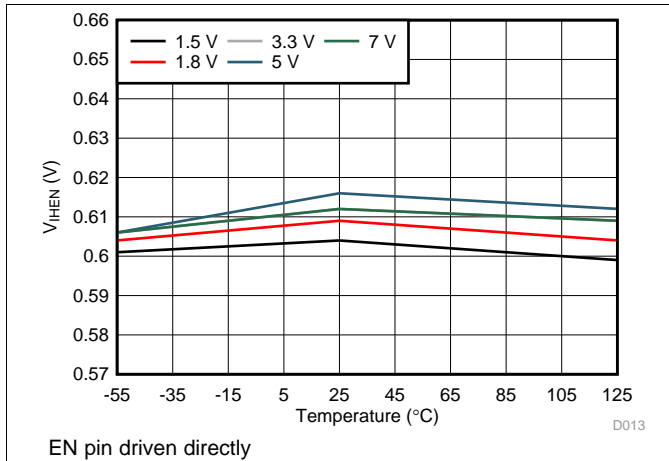


图 13.  $V_{IHEN}$  vs Temperature Across  $V_{IN}$

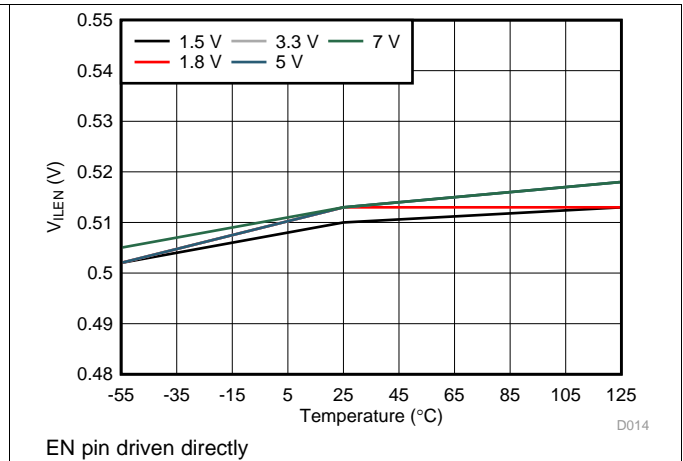


图 14.  $V_{ILEN}$  vs Temperature Across  $V_{IN}$

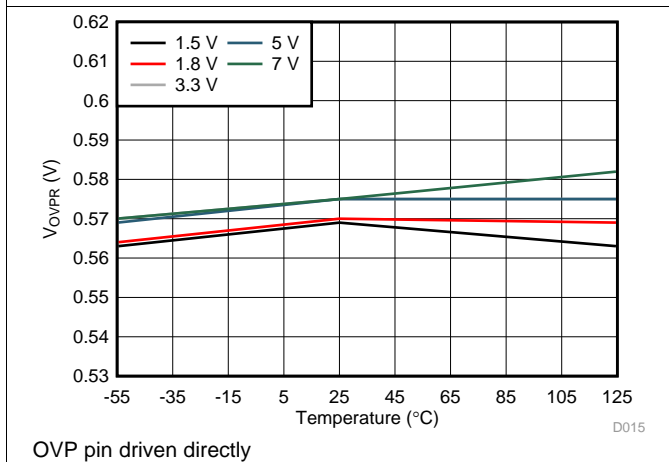


图 15.  $V_{OVPR}$  vs Temperature Across  $V_{IN}$

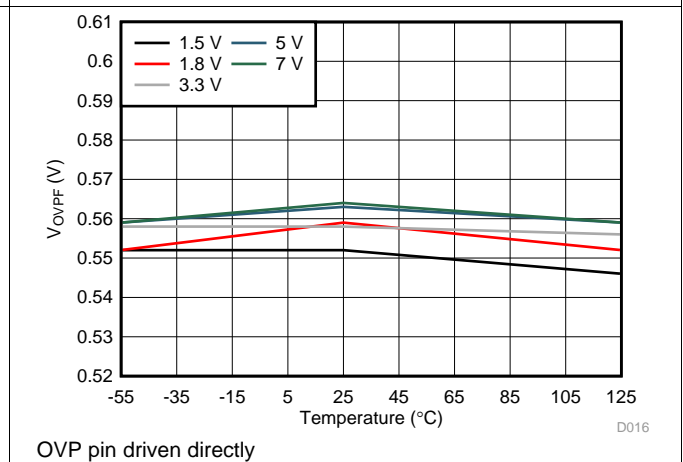


图 16.  $V_{OVPF}$  vs Temperature Across  $V_{IN}$

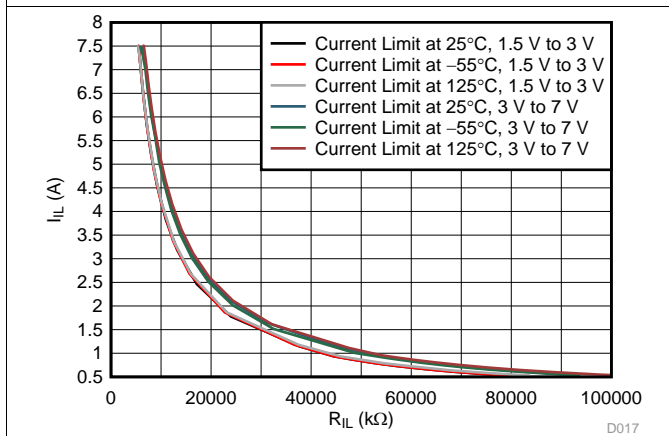


图 17.  $I_{IL}$  vs  $R_{IL}$  Across Temperature

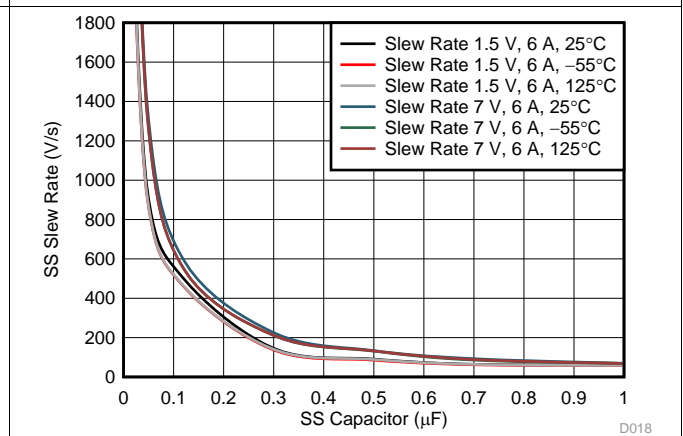


图 18. SS Slew Rate vs SS Capacitor Across Temperature

## 7 Parameter Measurement Information

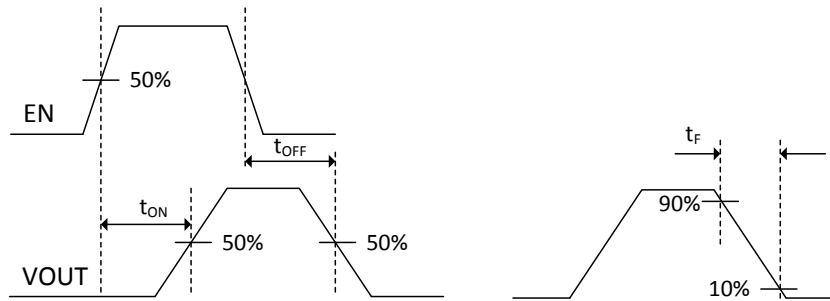


图 19.  $t_{ON}/t_{OFF}$  Waveforms

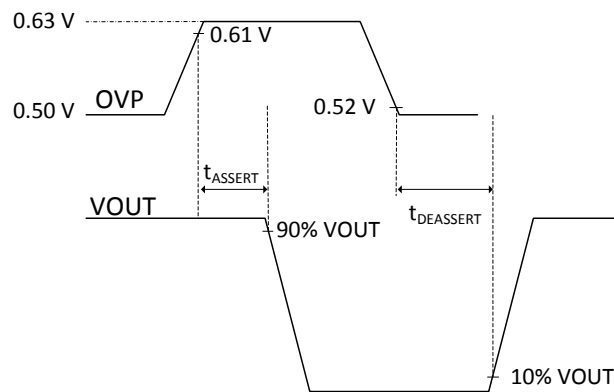


图 20.  $t_{ASSERT}/t_{DEASSERT}$  Waveforms

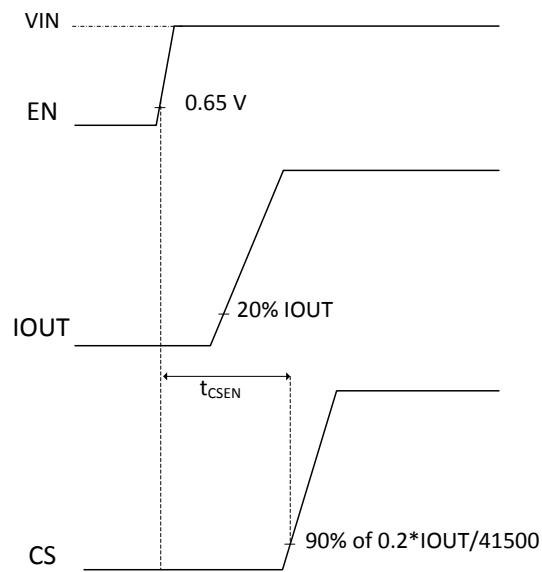


图 21.  $t_{CSEN}$  Waveforms

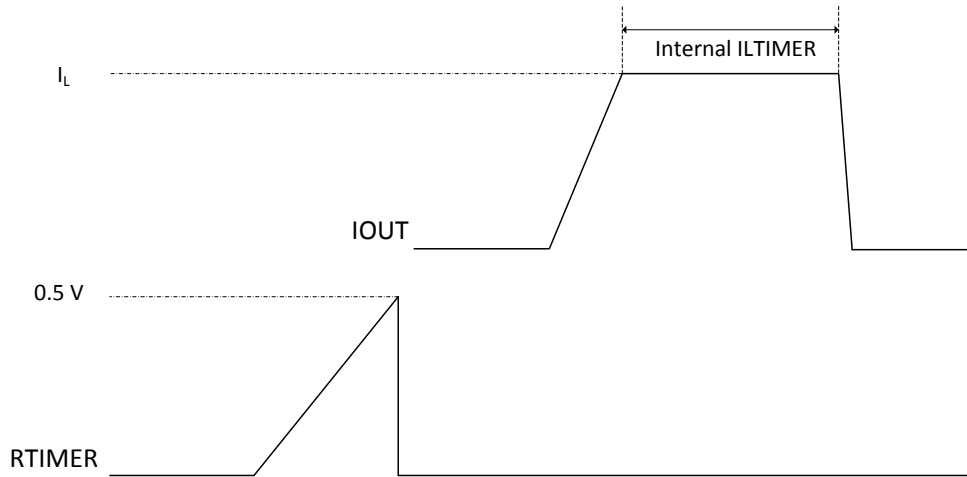


图 22. Internal ILTIMER Waveforms

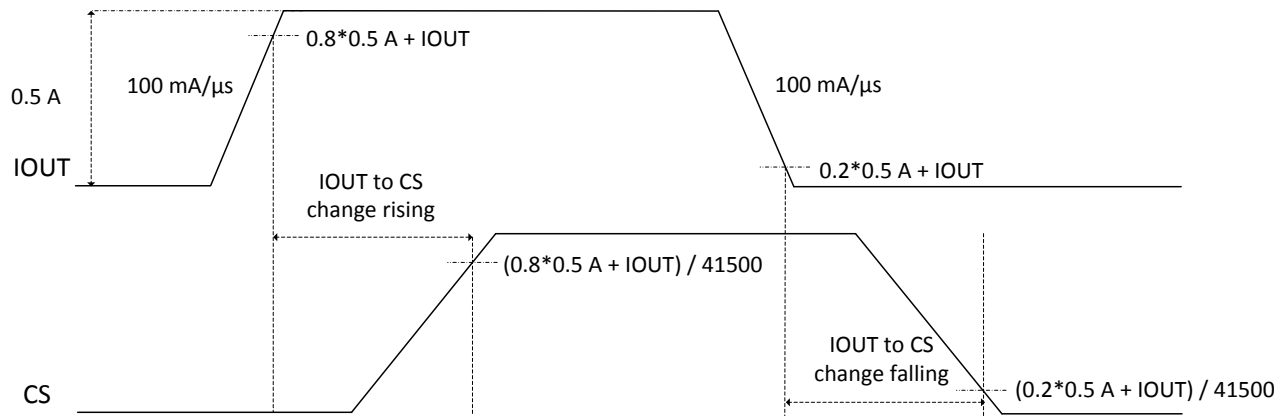


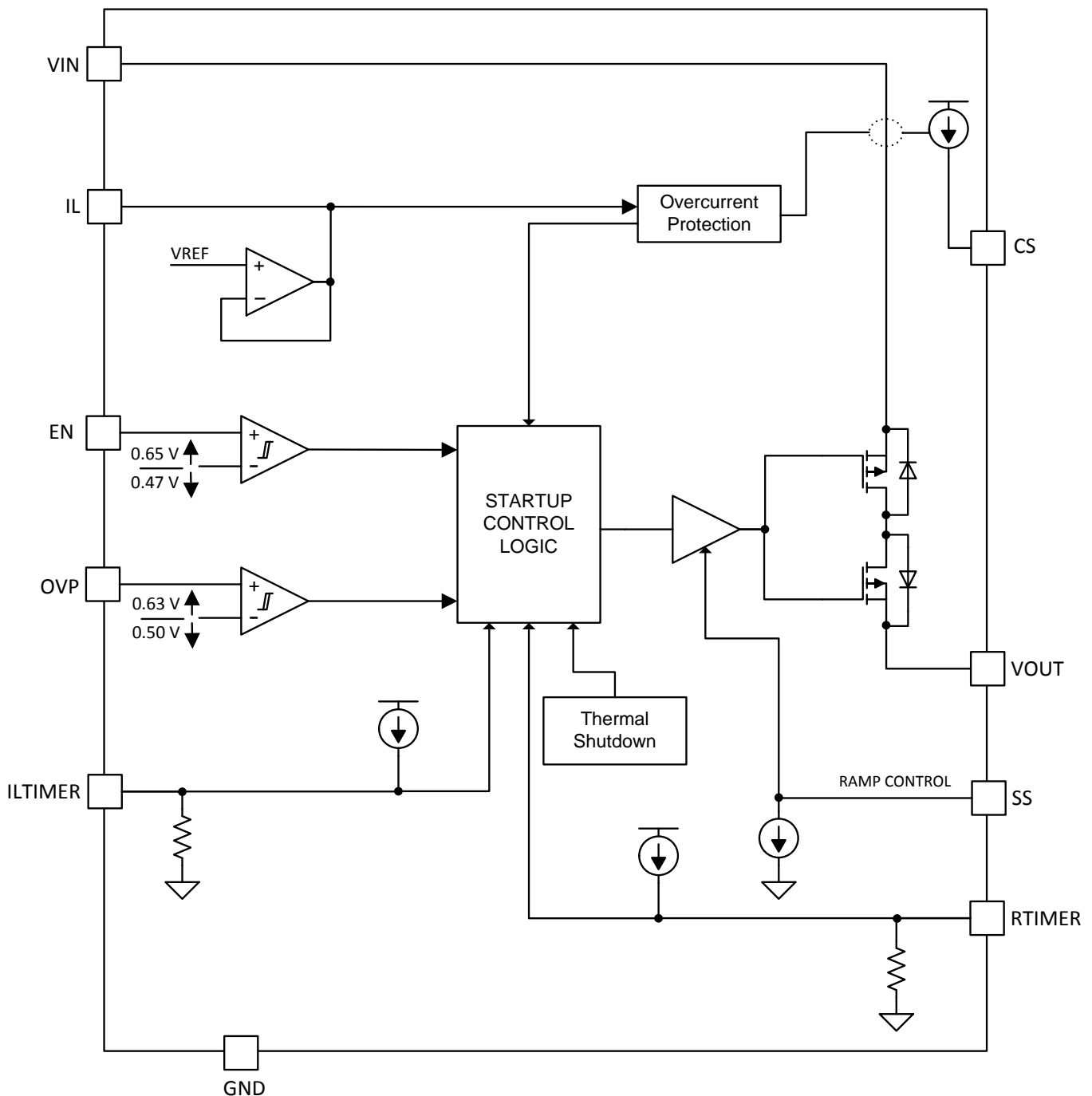
图 23. VOUT Current to CS Change Delay Time

## 8 Detailed Description

### 8.1 Overview

The TPS7H2201-SP device is a single channel, 6-A load switch with a programmable slew rate for applications that require specific rise-time as well as programmable current limit for protection purposes. In addition, the TPS7H2201-SP features a reverse current protection capability for power distribution applications.

### 8.2 Functional Block Diagram





## 8.3 Feature Description

### 8.3.1 Enable, Undervoltage, and Overvoltage Protection

图 24 shows how resistor dividers from VIN connected to the EN and OVP pins can be used to set the UVLO and OVP trip voltages. The EN pin controls the ON and OFF state of the internal FET. A voltage at this pin greater than  $V_{IHEN}$  turns on the FET and a voltage less than  $V_{ILEN}$  turns it off. The addition of an external resistor divider from VIN allows the EN pin to configure a different enable rising voltage or an undervoltage monitor (UVLO) based on the  $V_{IHEN}$  and  $V_{ILEN}$  specifications respectively. Typically, applications are optimized to either configure the enable rising voltage or the UVLO threshold. As an example, 公式 1 can be used to calculate the UVLO trip point fixing  $R_{TOP\_EN} = 100\text{ k}\Omega$ .

In a similar way to the EN pin, the overvoltage protection (OVP) feature of the device can be configured using a resistor divider from VIN connected to the OVP pin. The trip voltage for the OVP has to be less than the absolute maximum VIN voltage. A voltage at the OVP pin greater than  $V_{OVPR}$  will trip the OVP feature and will turn off the FET and a voltage less than  $V_{OVPF}$  will keep the FET on. If this feature is not desired, the OVP pin should be grounded. 公式 2 can be used to calculate the rising OVP trip point fixing  $R_{TOP\_OVP} = 100\text{ k}\Omega$ .

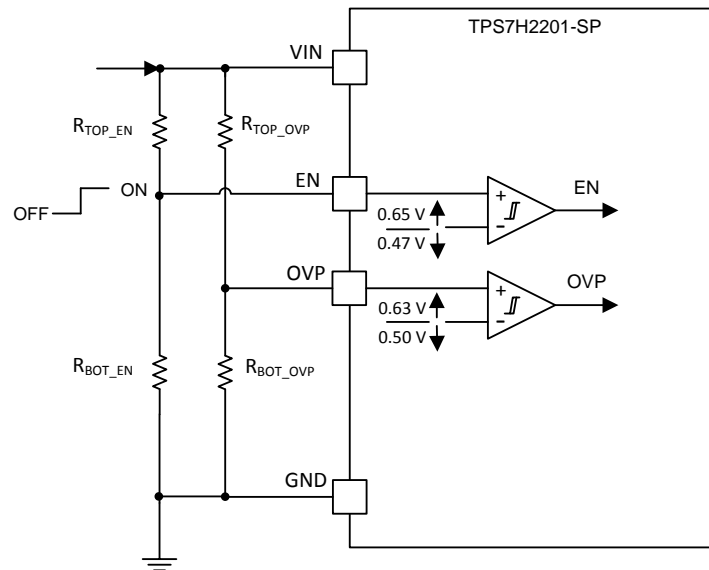


图 24. UVLO and OVP Thresholds Set by Resistor Dividers

$$R_{BOT\_EN} (\text{k}\Omega) \leq \frac{47}{V_{UVLO\_TRIP} (\text{V}) - 0.47} \quad (1)$$

$$R_{BOT\_OVP} (\text{k}\Omega) \geq \frac{63}{V_{OVP\_TRIP} (\text{V}) - 0.63} \quad (2)$$

### 8.3.2 Adjustable Rise Time

An external capacitor,  $C_{SS}$ , connected between the VOUT and SS pins sets the slew rate. The desired slew rate  $V_{OUT\_SR}$  is determined by  $t_r$ , the rise time in seconds, and  $\Delta V$ , the change in VOUT voltage in Volts as shown in 公式 3.

$$V_{OUT\_SR} (\text{V/s}) = \frac{\Delta V_{OUT} (\text{V})}{t_r (\text{s})} \quad (3)$$

In order to avoid false trips due to the programmable current limit, the desired slew rate must be less than  $V_{OUT\_SR\_MAX}$  as shown in 公式 4, where  $I_L$  is the programmed current limit,  $I_{VOUT}$  is the normal operation current flowing through the switch, and  $C_{OUT}$  is the output capacitor.

$$V_{OUT\_SR\_MAX} (\text{V/s}) < \frac{0.8 \times I_L (\text{A}) - 0.95 \times I_{VOUT} (\text{A})}{C_{OUT} (\text{F})} \quad (4)$$

## Feature Description (接下页)

Once the slew rate has been calculated and meeting the constraint in 公式 4, the  $C_{SS}$  capacitor is then calculated using 公式 5 for  $V_{IN} < 3\text{-V}$  and  $I_{OUT} \geq 3\text{-A}$  applications. For all other applications, use 公式 6.

$$C_{SS}(\mu\text{F}) = \frac{45}{V_{OUT_{SR}}(\text{V/s})}$$

for  $V_{IN} < 3\text{ V}$  and  $I_{OUT} \geq 3\text{ A}$

(5)

$$C_{SS}(\mu\text{F}) = \frac{65}{V_{OUT_{SR}}(\text{V/s})}$$

for all other conditions

(6)

### 8.3.3 Programmable Current Limiting

A current limit can be programmed using an external resistor connected from the IL pin to GND. This programmed current limit ( $\pm 20\%$  accurate) refers to the continuous current through the device and therefore, when operated at its maximum current rating (6 A), the programmed current limit needs to be set 20% higher. As shown in 图 25, a current limit event of this nature is defined as a soft short. The resistor value  $R_{IL}$ , can be calculated using 公式 7 for  $V_{IN} \leq 3\text{ V}$ , and 公式 8 for  $V_{IN} > 3\text{ V}$ , where  $I_L$  is the programmed current limit value in amperes. This programmable current limiting feature is different from the internal current limiting activated during fast trip mode as shown in 图 26. A current limit event in this case is defined as a hard short and this current limit (typical of 22 A) cannot be programmed.

$$R_{IL}(\Omega) = \frac{45500}{I_L(\text{A})}$$

for  $V_{IN} \leq 3\text{ V}$

(7)

$$R_{IL}(\Omega) = \frac{49000}{I_L(\text{A})}$$

for  $V_{IN} > 3\text{ V}$

(8)

### 8.3.4 Programmable Fault Timer

A capacitor connected from the ILTIMER pin to GND determines the programmable current limit fault time duration. The ILTIMER pin will charge the capacitor to 0.5 V during an overload condition and will discharge it otherwise through an internal pull down resistance. The time that the device will be in current limit before turning off is configured by  $C_{ILTIMER}$  and the time can be calculated using 公式 9. Connecting this pin to  $V_{IN}$  will cause the device to be disabled once the internal current limit timer expires as shown in 图 22. However, connecting it to GND will disable the internal timer functionality completely and therefore, in the case of a short, the device will remain at the programmed current limit indefinitely. When using the internal timer, only the fast trip off current limit is active.

$$t(\mu\text{s}) = \frac{C(\text{pF})}{2}$$

(9)

The time that the device remains disabled after the current limit timer expires is configurable through a capacitor connected from the RTIMER pin to GND. The RTIMER pin will charge the capacitor to 0.5 V after the switch is turned off and will discharge it otherwise. The time can be calculated using 公式 9. Connecting this pin to GND will keep the device disabled and it will require the device to be enabled by cycling the EN pin. The behavior of the ILTIMER and RTIMER pins for a soft short, hard short and internal timer conditions are shown in 图 25, 图 26, and 图 27, respectively. Please notice that 图 25 and 图 26 assume the fault is not present after the switch has been disabled and enabled again (retry mode). If the fault is present after the retry mode, the device will go into current limit mode and this cycle will repeat until the fault is no longer present.

Feature Description (接下页)

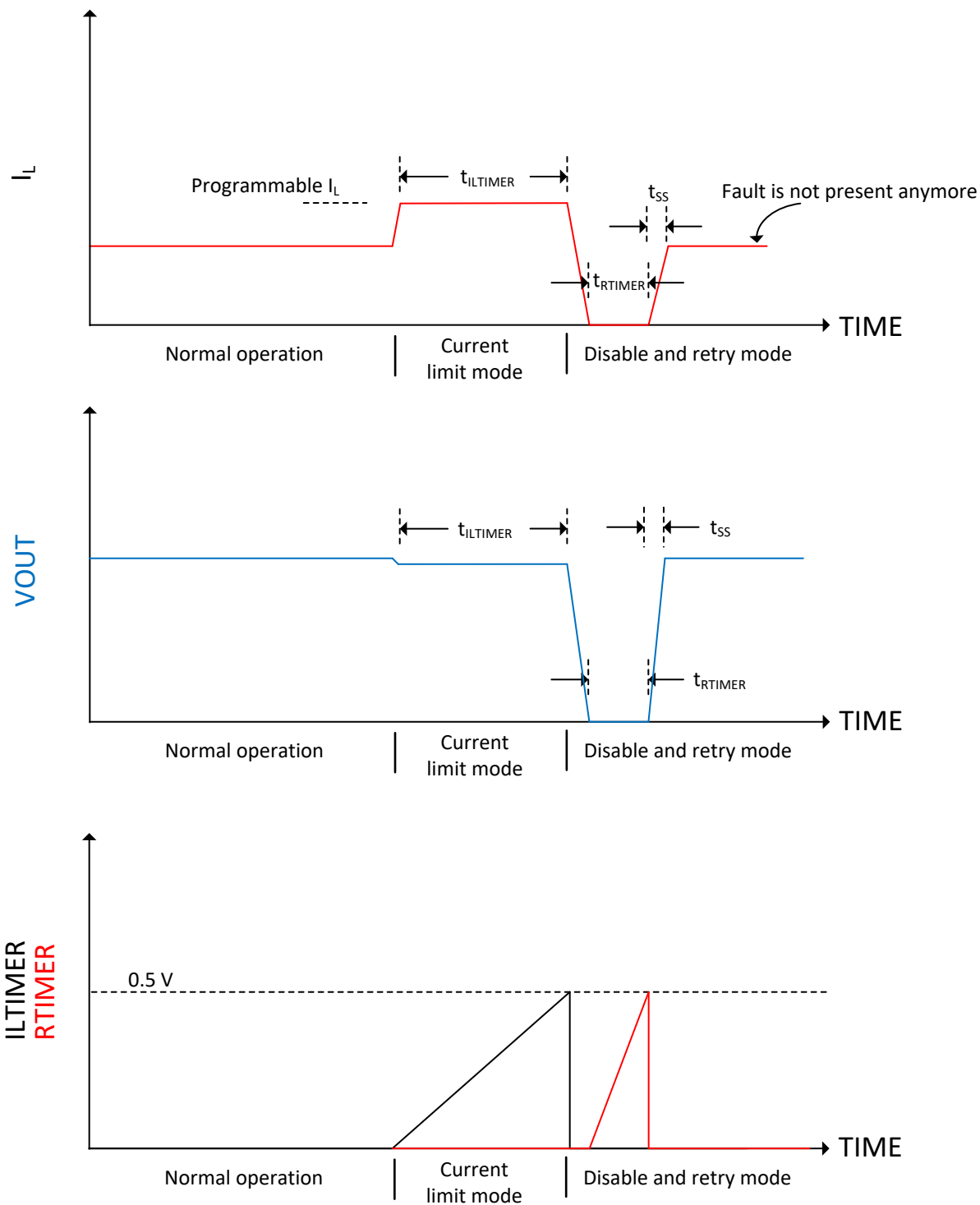


图 25. Soft Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

Feature Description (接下页)

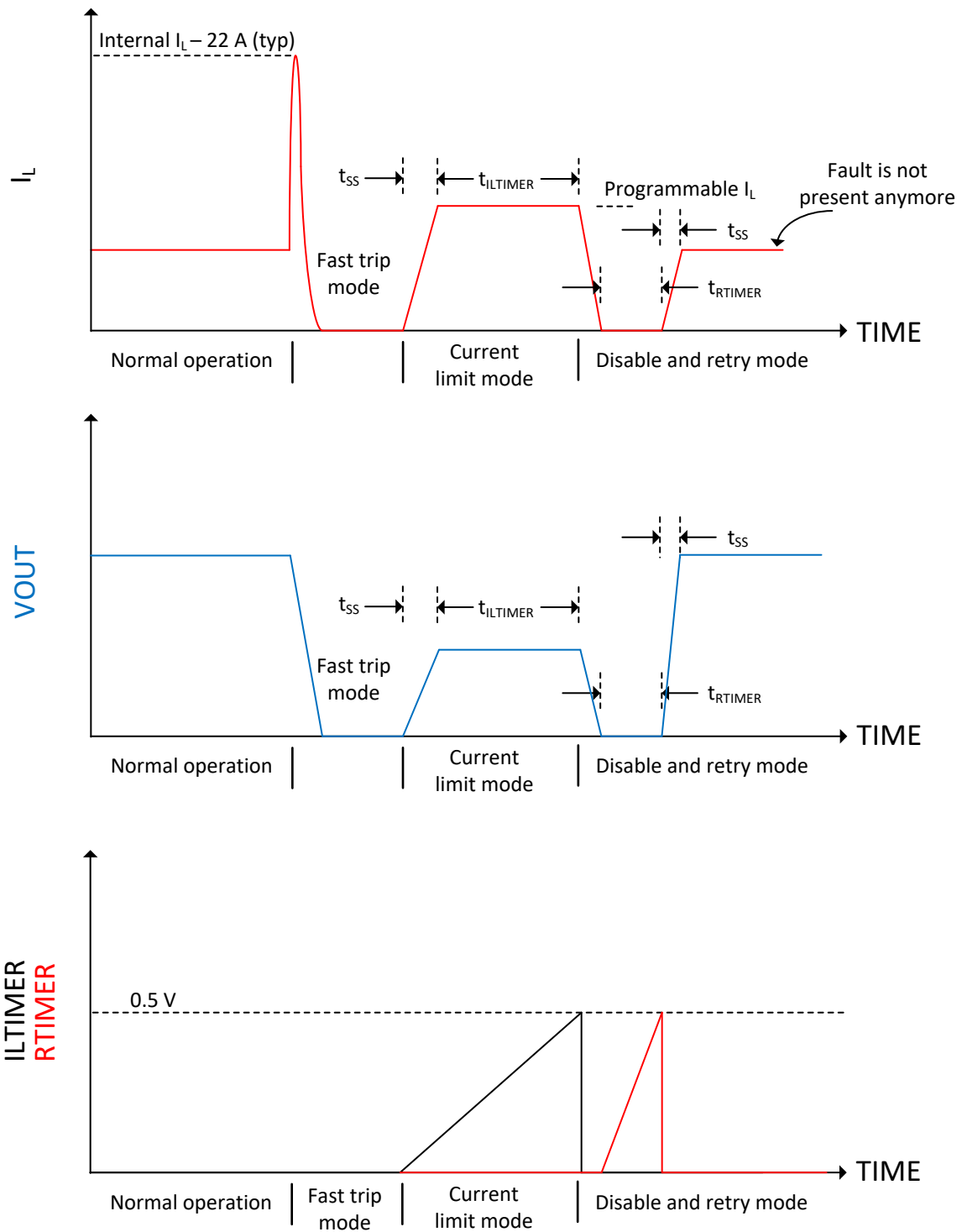


图 26. Hard Short Programmable Fault Timer Operation Connecting Capacitors to ILTIMER and RTIMER Pins

Feature Description (接下页)

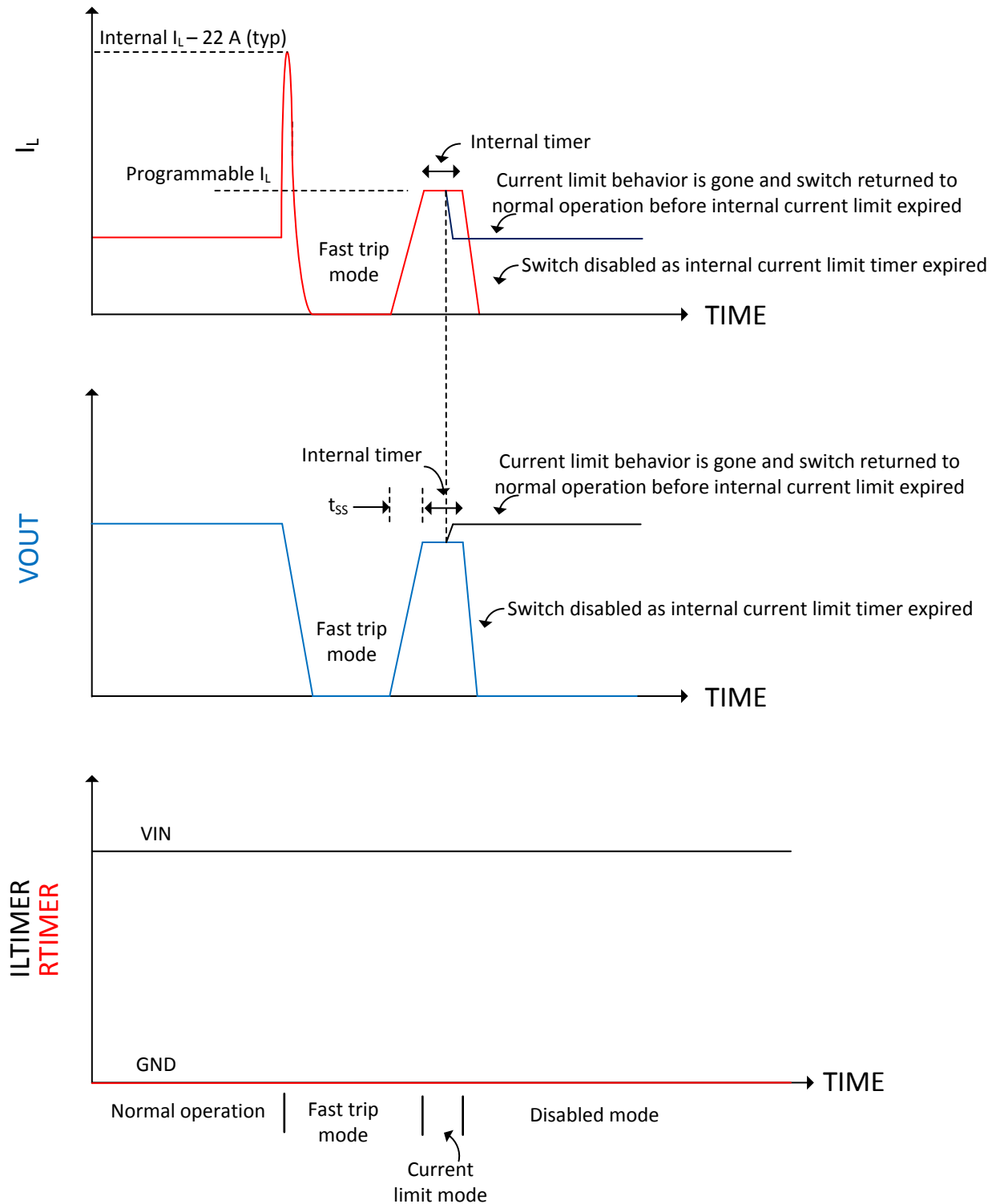
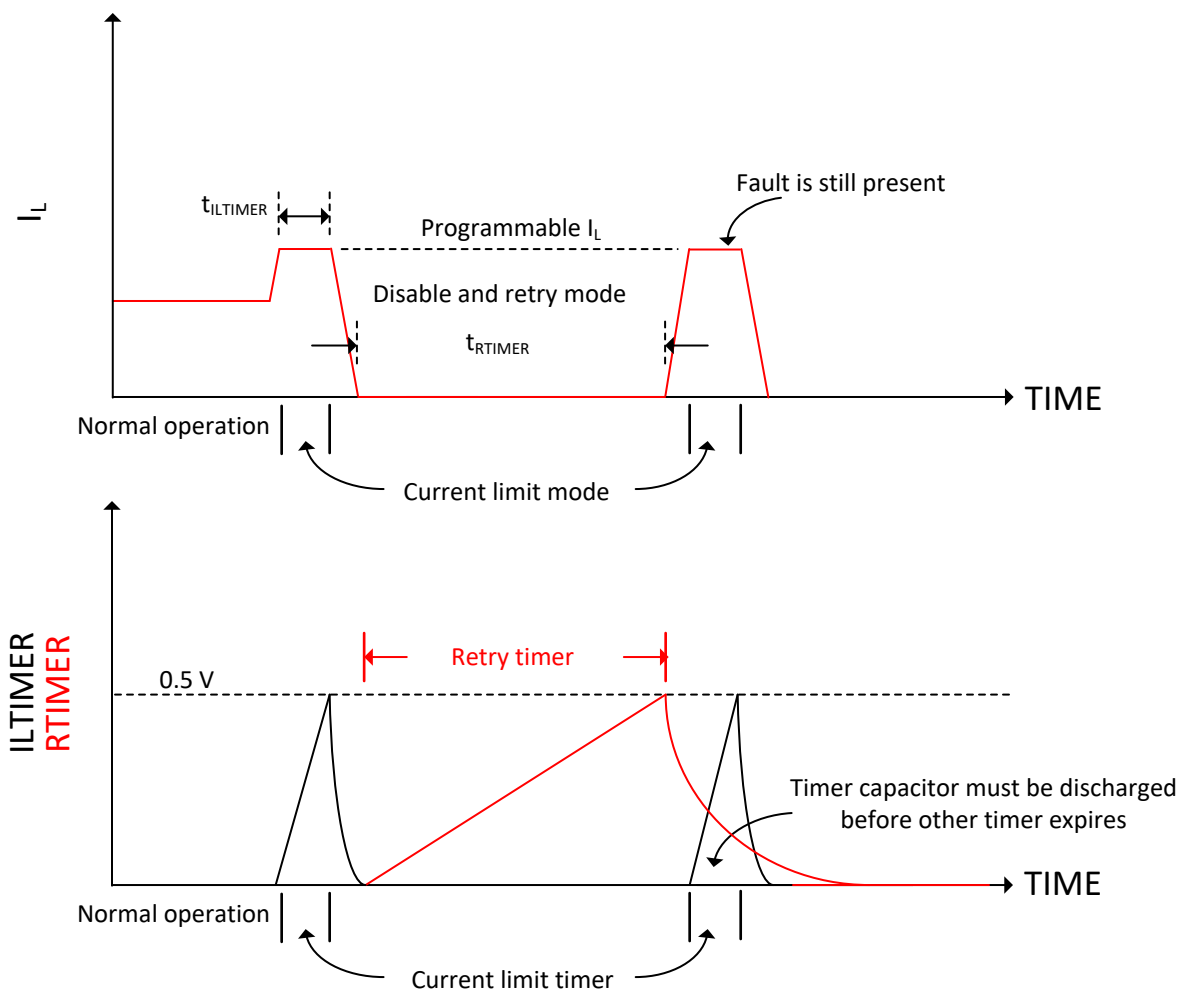


图 27. Programmable Fault Timer Operation Using the Internal Current Limit Timer and Disabling the Retry Mode

## Feature Description (接下页)

The programmable fault timers, ILTIMER and RTIMER, should be set in such a way that the capacitor for one timer is discharged before the other timer expires to ensure proper operation. In the specific case of using the internal ILTIMER, the RTIMER capacitor should be sized such that it is discharged before the internal ILTIMER expires, assuming the fault is still present. 图 28 shows a situation where this constraint is not met as the RTIMER is much larger than the ILTIMER and therefore, the  $C_{RTIMER}$  is not discharged before the  $C_{ILTIMER}$  reaches 0.5 V, which is when the ILTIMER will expire. In order to avoid this situation, the constraint shown in 公式 10 must be met. Using this equation, once a capacitor for a timer has been selected ( $C_1$  in 公式 10), the maximum value for the capacitor of the second timer can be determined. The internal pull-down resistance for each of the timers can be found in the [Electrical Characteristics](#) table. For the situation shown in 图 28,  $C_1$  and  $R_{PD1}$  in 公式 10 correspond to the RTIMER.



**图 28. Programmable Fault Timer Capacitors Constraint**

$$C_1 (\mu\text{F}) < \frac{C_2 (\text{pF})}{8 \times R_{PD1} (\Omega)} \quad (10)$$

## Feature Description (接下页)

### 8.3.5 Current Sense

This pin will output a current proportional to the output current of the switch for current sensing applications. A resistor to GND will convert this current to voltage for current sensing purposes. The output current will be the switch current divided by 41,500. The CS pin will have a valid output 5 ms after the device has been enabled.

### 8.3.6 Parallel Operation

The TPS7H2201-SP can be configured in parallel operation either to increase the current capability, up to 12 A, or to reduce the on-state resistance. In this case, all pins are shared as shown in [图 29](#), except the current limit resistor ( $R_{IL}$ ) for proper operation of the internal current limit loop. The current limiting resistors must be sized as described in the [Programmable Current Limiting](#) section.

Feature Description (接下页)

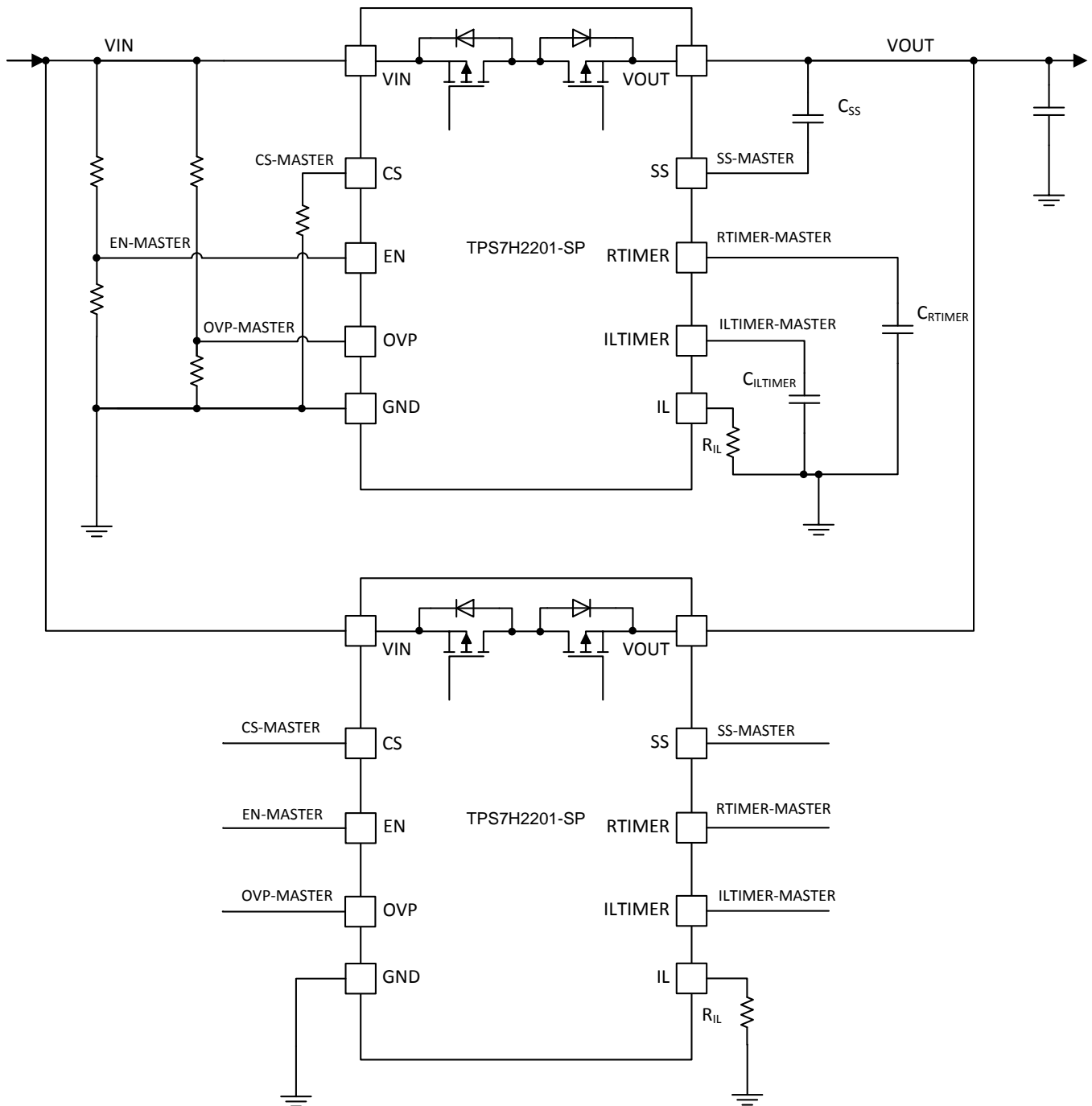


图 29. Parallel Configuration to Reduce Resistance or Increase Current Capability



## 8.4 Device Functional Modes

表 3 lists the VOUT pin states as determined by the EN pin.

**表 3. VOUT Connection**

EN PIN	TPS7H2201-SP
$< V_{ILEN}$	Open
$> V_{IHEN}$	VIN

## 9 Application and Implementation

---

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 9.1 Application Information

The TPS7H2201-SP device is a single channel, 6-A load switch with multiple programmable features such as current limit, undervoltage and overvoltage, current limit and retry timers, and soft start. In addition, the TPS7H2201-SP features a reverse current protection capability for power distribution applications and current sensing for load monitoring purpose. The TPS7H2201-SP user's guide is available on the TI website, [TPS7H2201EVM-CVAL Evaluation Module \(EVM\) User's Guide](#). The guide highlights standard EVM configurations, test results, schematic, and BOM for reference.

### 9.2 Typical Applications

In addition to the standard power management applications where a power switch can be used, there are 2 main applications in which the TPS7H2201-SP can be used in space power applications:

- Redundancy for primary and secondary voltage rails common in satellite applications
- Protection for critical or SEL sensitive loads

#### 9.2.1 Redundancy

In applications where primary and secondary (redundant) power rails are present, the TPS7H2201-SP is ideal to implement redundancy because of its reverse current blocking capability. In this case, since the load switch is placed at the input of the point of load regulator, the on-resistance of the switch is not as critical.

Typical Applications (接下页)

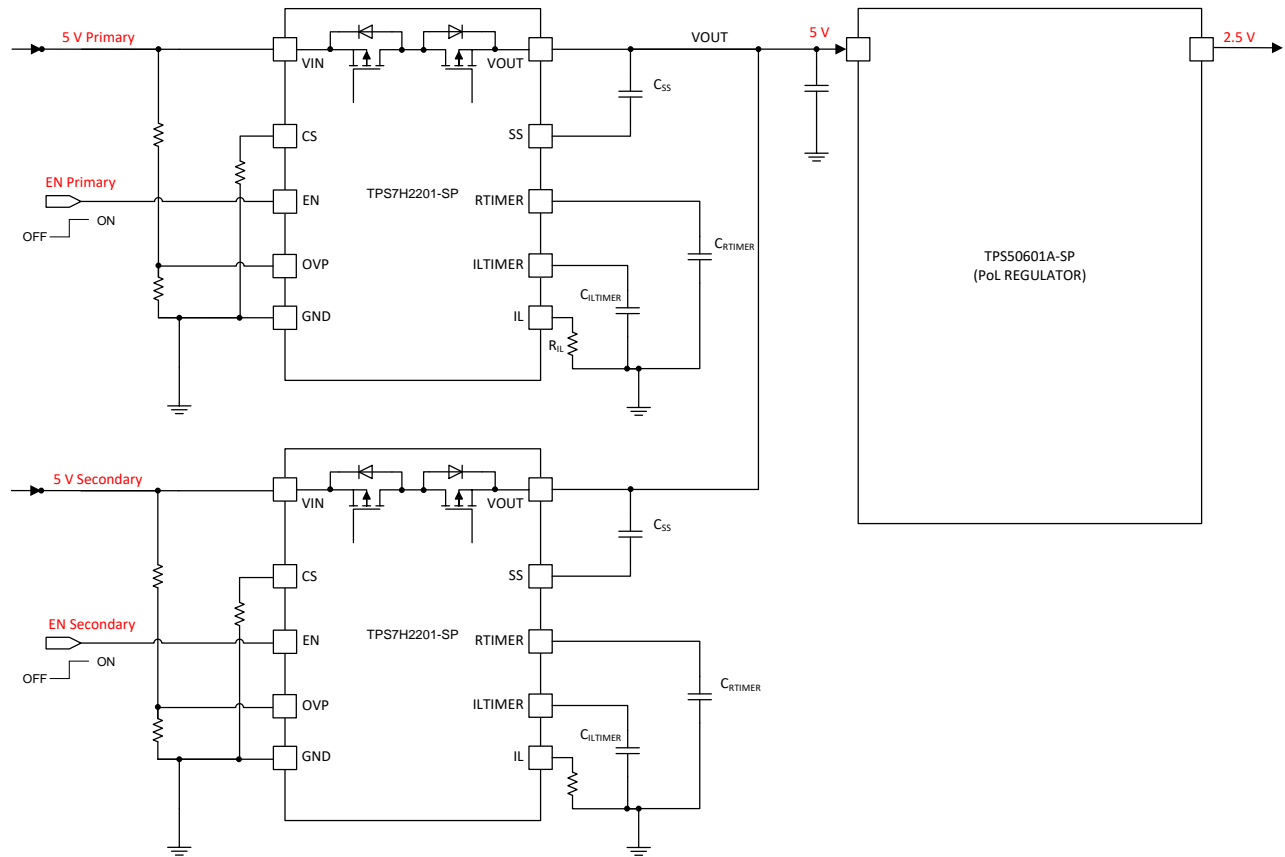


图 30. Redundancy Example Using the TPS7H2201-SP

9.2.2 Protection

The protection features of the TPS7H2201-SP can also be used for SEL sensitive loads. In such case, the on-resistance of the switch might be more relevant as it is placed after the point of load regulator but in such case, two load switches can be placed in parallel to reduce the on-resistance if needed. The main advantages of using the load switch at this location is faster response to SEL events and automatic recovery due to the retry mode of the programmable fault timer.

Typical Applications (接下页)

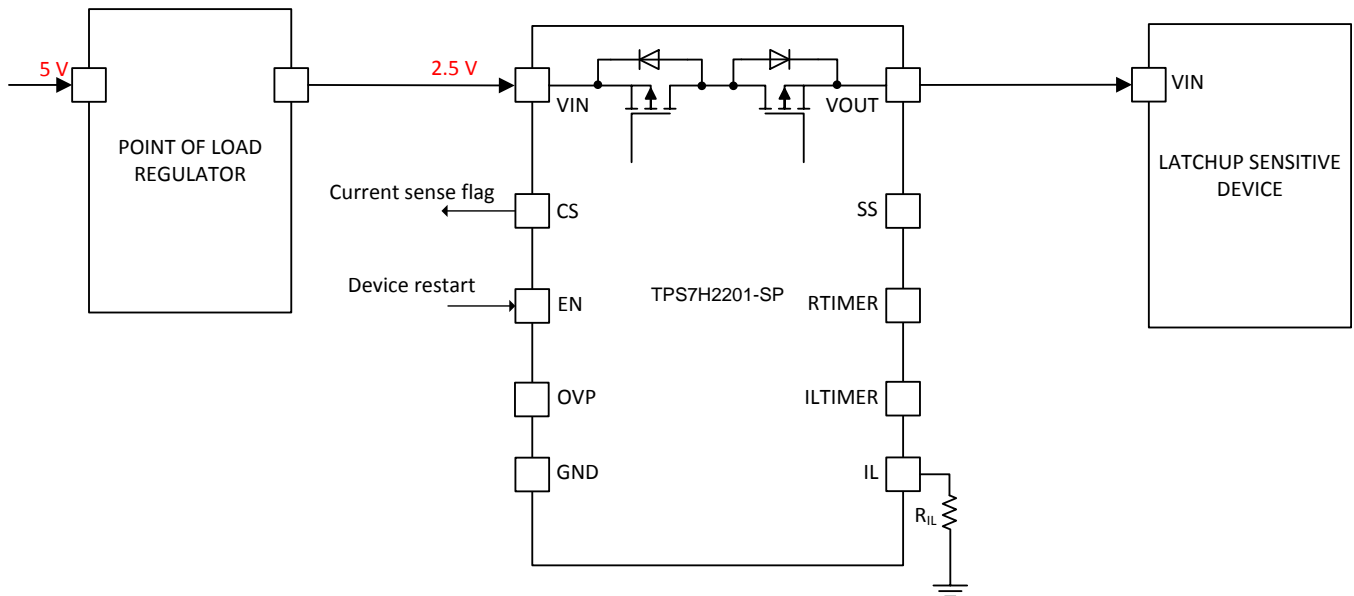


图 31. Protection Example Using the TPS7H2201-SP

9.2.3 Design Requirements

图 32 shows a typical application schematic that is applicable to both the redundancy and the protection applications previously discussed.

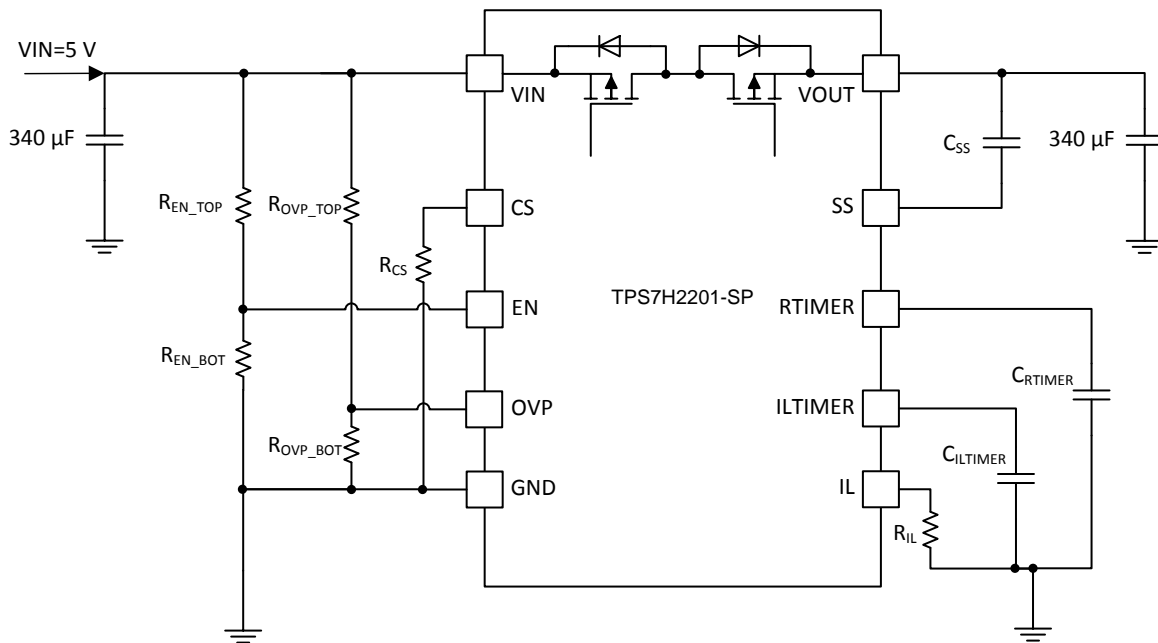


图 32. Typical Application Schematic

表 4 shows the design parameters.

**表 4. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
VIN	5 V
Undervoltage lockout set point	3.5 V
Overvoltage protection set point	6.5 V
Output current	6 A
Current limit	7.5 A
Current limit timer	1 ms
Retry timer	1 ms
Soft start time	9 ms
Input and output capacitors	340 μF

## 9.2.4 Detailed Design Procedure

### 9.2.4.1 Undervoltage Lockout

The undervoltage lockout set point is configured using the resistor divider,  $R_{EN\_TOP}$  and  $R_{EN\_BOT}$  connected to the EN pin. Set the  $R_{EN\_TOP} = 100\text{ k}\Omega$  and, using [公式 1](#), calculate the value for  $R_{EN\_BOT}$ . For an  $UVLO = 3.5\text{ V}$ ,  $R_{EN\_BOT} = 15.5\text{ k}\Omega$ . When choosing the UVLO set point, the resistor divider must ensure that the device will still get enabled for the VIN used in the application. This is achieved by making sure that the  $V_{IHEN}$  requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is smaller than the VIN used in the application. [公式 11](#) shows this VIN and  $V_{IHEN}$  requirement to set the UVLO point. For this particular application, the requirement is met as the result is 4.84 V.

$$V_{IHEN} \times \frac{R_{EN\_TOP} + R_{EN\_BOT}}{R_{EN\_BOT}} \leq VIN \quad (11)$$

### 9.2.4.2 Overvoltage Protection

In a similar way to the UVLO set point, the overvoltage protection set point is configured using the resistor divider,  $R_{OVP\_TOP}$  and  $R_{OVP\_BOT}$  connected to the OVP pin. Set the  $R_{OVP\_TOP} = 100\text{ k}\Omega$  and, using [公式 2](#), calculate the value for  $R_{OVP\_BOT}$ . For an  $OVP = 6.5\text{ V}$ ,  $R_{OVP\_BOT} = 10.7\text{ k}\Omega$ . When choosing the OVP set point, the resistor divider must ensure that the device will still get enabled for the VIN used in the application. This is achieved by making sure that the  $V_{OVPF}$  requirement is still met with the chosen resistor divider and that the VIN needed to meet the requirement is larger than the VIN used in the application. [公式 12](#) shows this VIN and  $V_{OVPF}$  requirement to set the OVP point. For this particular application, the requirement is met as the result is 5.16 V.

$$V_{OVPF} \times \frac{R_{OVP\_TOP} + R_{OVP\_BOT}}{R_{OVP\_BOT}} \geq VIN \quad (12)$$

### 9.2.4.3 Current Limit

The current limit is configured using  $R_{IL}$ . Based on the output current for this design, the minimum current limit that can be programmed is  $I_{OUT} + 1.5\text{ A}$  for a total of 7.5 A. As a result, using [公式 8](#), the resistor value is 6.53 kΩ.

### 9.2.4.4 Programmable Fault Timers

The programmable fault timers are configured using the  $C_{ILTIMER}$  and the  $C_{RTIMER}$  capacitors. For this particular design, both timers are set to 1 ms. Therefore, using [公式 9](#), the value for each capacitor is 2000 pF. These capacitor values meet the requirement in [公式 10](#).

### 9.2.4.5 Soft Start Time

The soft start time is configured using the  $C_{SS}$  capacitor. In order to calculate the value of the capacitor, the VOUT slew rate needs to be calculated using 公式 3 to make sure the maximum VOUT slew rate requirement shown in 公式 4 is satisfied. This requirement is particularly important for space applications where large output capacitance is typically used, which translates to a lower maximum allowable VOUT slew rate. For this particular design, the VOUT slew rate is 555 V/s which is less than the maximum VOUT slew rate of 882 V/s, meeting the requirement from 公式 4. Now, the soft start capacitor value can be calculated as 117 nF using 公式 6, since  $V_{IN} = 5\text{ V}$  for this application.

### 9.2.5 Application Curves

The power-up behavior of this design example is shown in 图 33 and the current limit behavior is shown in 图 34.

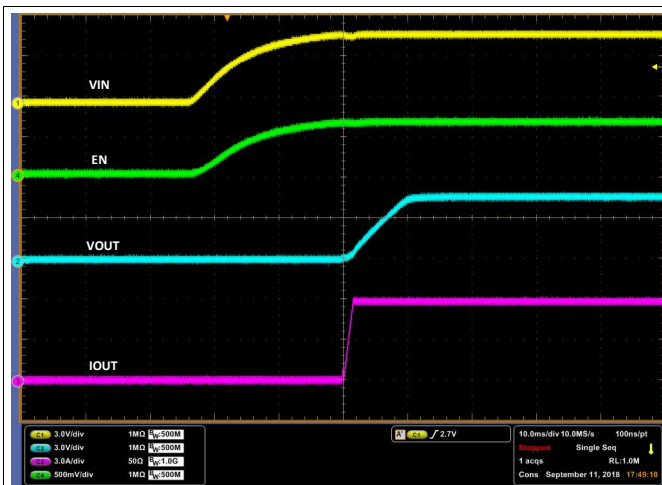


图 33. Power-up Behavior of the TPS7H2201-SP

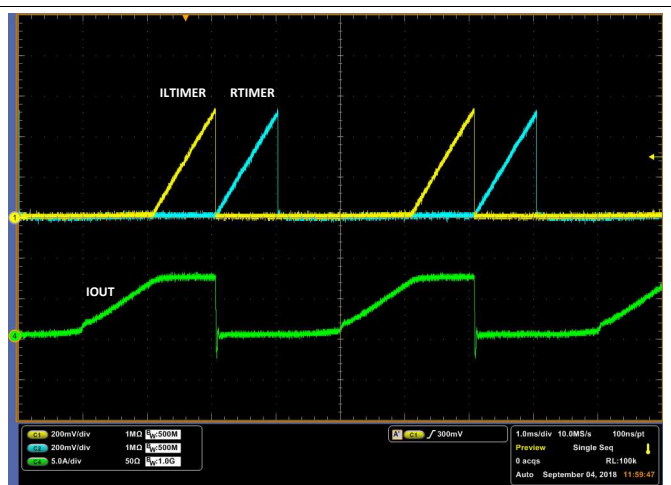


图 34. ILTIMER and RTIMER Waveforms When IL is Set to 7.5 A

## 10 Power Supply Recommendations

The TPS7H2201-SP is designed to operate from an input voltage supply range between 1.5 V to 7 V. This supply voltage must be well regulated and proper local bypass capacitors should be used for proper electrical performance from VIN to GND. Due to stringent requirements for space applications, typically numerous input bypass capacitors are used and the total capacitance is much larger than for commercial applications. The TPS7H2201-SP Evaluation Module uses one 330- $\mu$ F tantalum capacitor in parallel with one 10- $\mu$ F and one 0.1- $\mu$ F ceramic capacitor.

## 11 Layout

### 11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects. In general, the components should be placed close to the device such that traces remain as short as possible to avoid parasitic capacitance. In addition, due to the possibility of large power dissipation in fault conditions (short at VOUT), thermal vias should be placed in the PCB for the thermal pad.

### 11.2 Layout Example

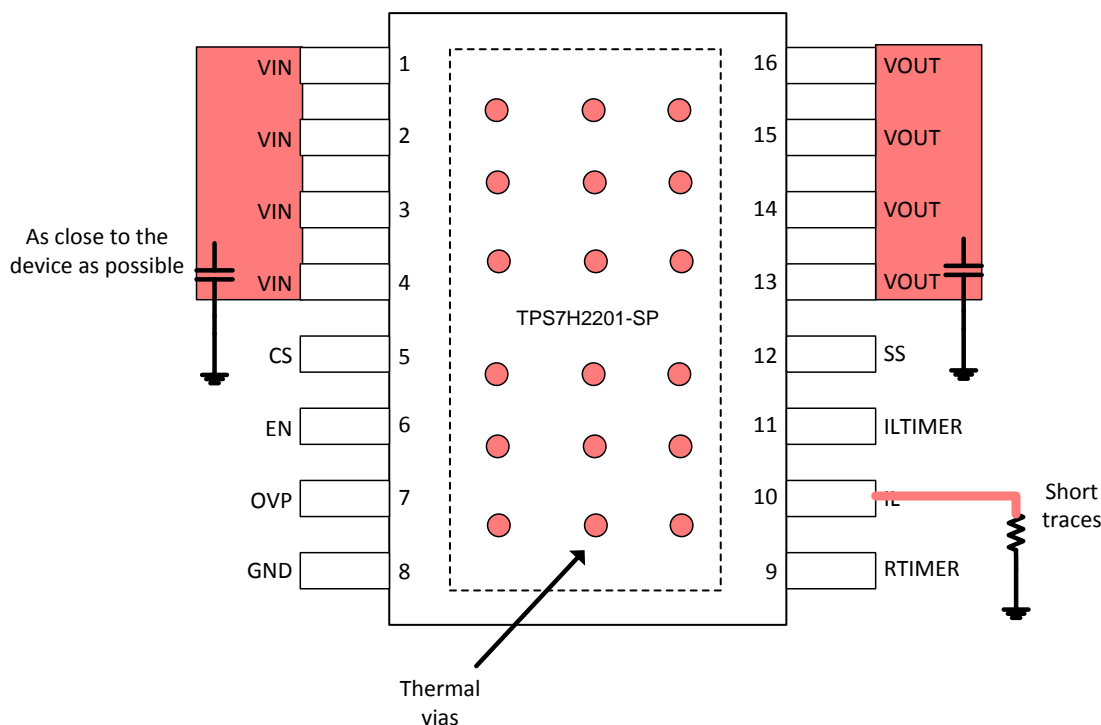


图 35. Layout Recommendation

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，《[TPS7H2201EVM-CVAL 评估模块 \(EVM\) 用户指南](#)》

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.



### 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1722001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962-1722001VXC TPS7H2201MHKRV	<a href="#">Samples</a>
5962R1722001V9A	ACTIVE	XCEPT	KGD	0	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		<a href="#">Samples</a>
5962R1722001VXC	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1722001VXC TPS7H2201MHKRV	<a href="#">Samples</a>
TPS7H2201HKR/EM	ACTIVE	CFP	HKR	16	1	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H2201HKREM	<a href="#">Samples</a>
TPS7H2201Y/EM	ACTIVE	XCEPT	KGD	0	5	RoHS & Green	Call TI	N / A for Pkg Type	25 to 25		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TUBE**


\*All dimensions are nominal

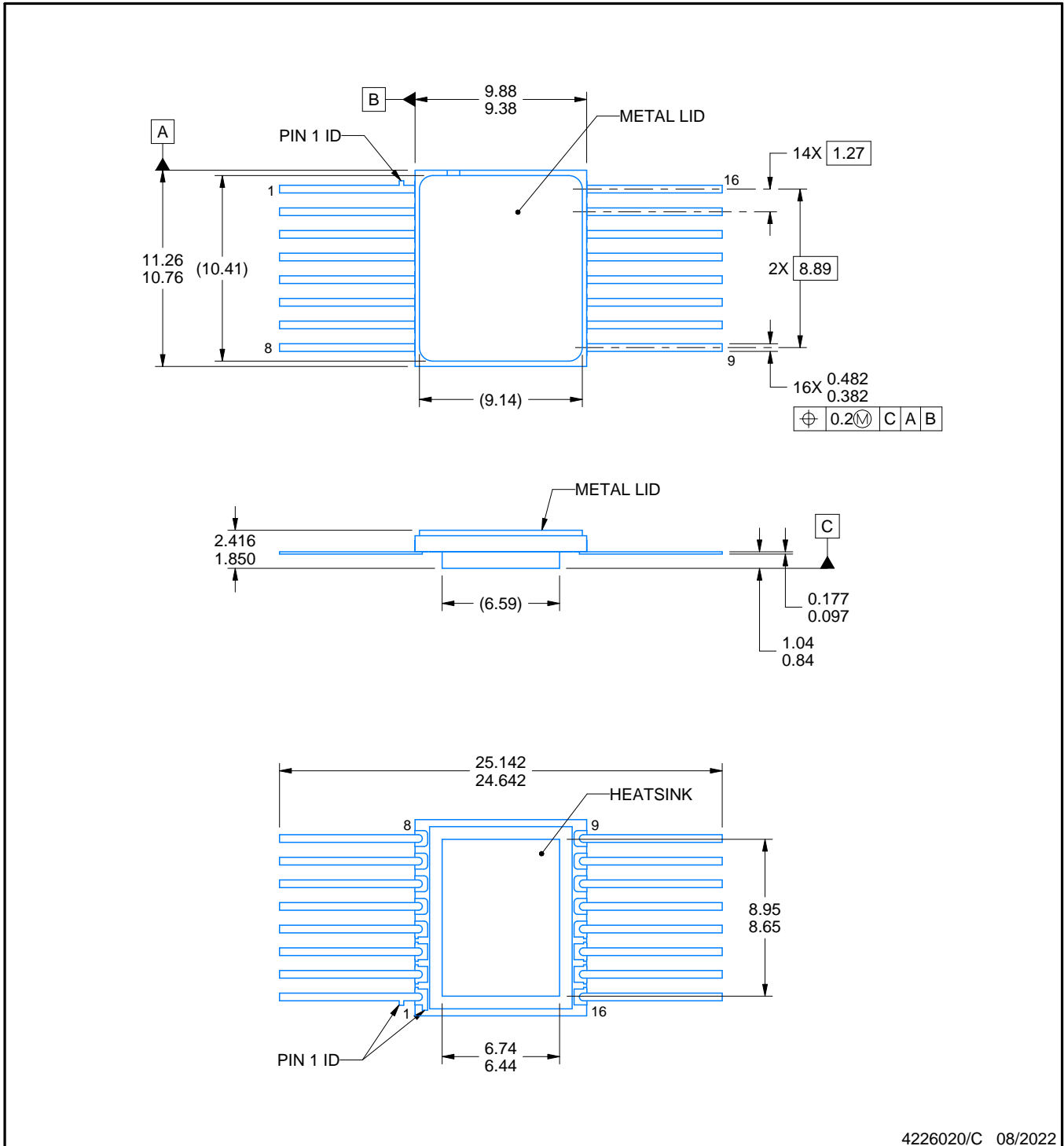
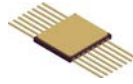
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-1722001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
5962R1722001VXC	HKR	CFP	16	1	506.98	26.16	6220	NA
TPS7H2201HKR/EM	HKR	CFP	16	1	506.98	26.16	6220	NA

**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPS7H2201Y/EM	KGD	XCEPT	0	5	5 x 5	70	6.35	3.81	610	1.3	8.89	8.13



4226020/C 08/2022

NOTES:

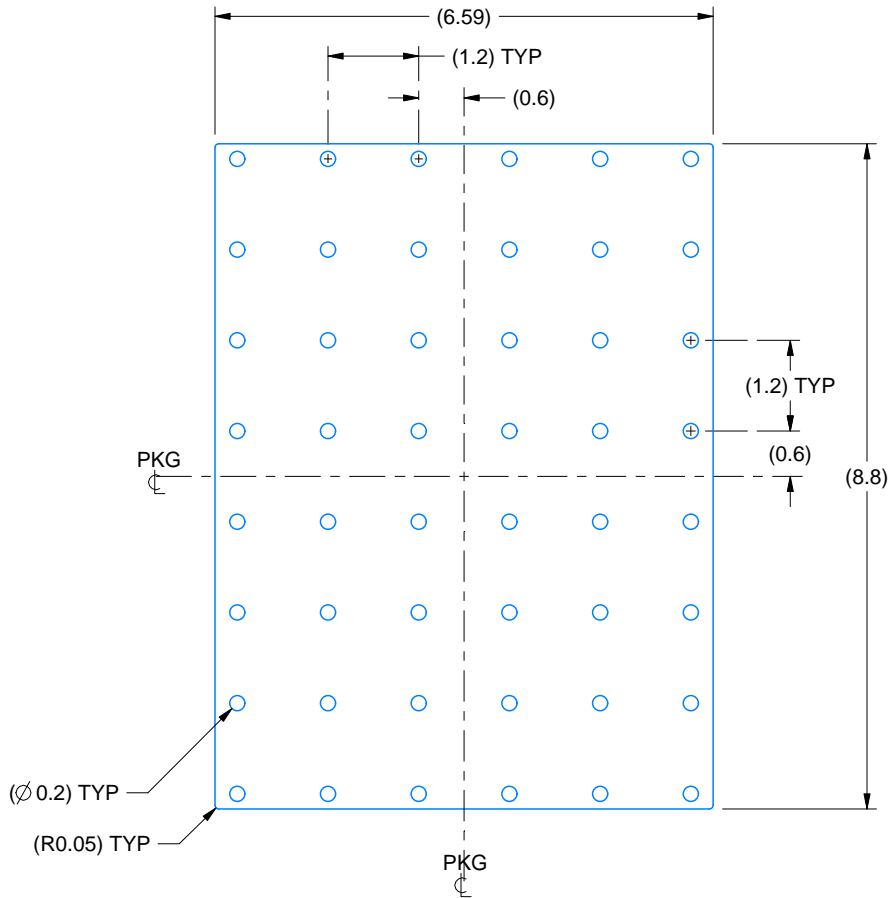
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

# EXAMPLE BOARD LAYOUT

HKR0016A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



**HEATSINK LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:10X

4226020/C 08/2022

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司