TEXAS INSTRUMENTS

TS5A3166-Q1
ZHCSE31A –JULY 2014–REVISED DECEMBER 2014

TS5A3166-Q1 0.9Ω SPST 模拟开关

1 特性

- 符合汽车应用要求
- 断电模式下的隔离，$V_+ = 0$
- 低导通状态电阻 (0.9Ω)
- 控制输入为 5.5V 耐压
- 低电荷注入
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 性能测试符合 JESD 22 标准
  - 2000V 人体放电模式（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 远程信息处理
- 汽车雷达系统
- 信息娱乐系统
- 车身控制模块
- 引擎控制单元
- 锁相环 (PLL) 应用

3 说明

TS5A3166-Q1 是一款单刀单掷 (SPST) 模拟开关，工作电压范围为 1.65V 至 5.5V。该器件具有较低的导通状态电阻。 该器件的总谐波失真 (THD) 性能出色，并且功耗超低。 这些特性使得这款器件适合于便携式音频应用。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TS5A3166-Q	SC70 (5)	2.00mm × 1.25mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图

English Data Sheet: SCDS357

目录

5 修订历史记录

Changes from Original (July 2014) to Revision A	**Page**

6 Pin Configuration and Functions

SOT-23 OR SC-70 PACKAGE
(TOP VIEW)

YZP PACKAGE
(BOTTOM VIEW)
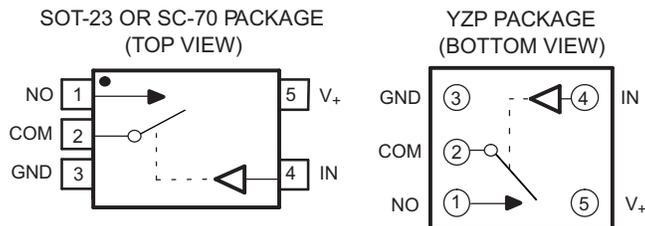
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NO	1	IO	Normally closed
COM	2	IO	Common
GND	3	GND	Digital ground
IN	4	Input	Digital control pin to connect COM to NO
V_+	5	Power	Power Supply

7 Specifications

7.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range[3]		−0.5	6.5	V
V_{NO} V_{COM}	Analog voltage range[3][4][5]		−0.5	$V_+ + 0.5$	V
I_K	Analog port diode current	$V_{NO}, V_{COM} < 0$	−50		mA
I_{NO} I_{COM}	On-state switch current	$V_{NO}, V_{COM} = 0$ to V_+	−200	200	mA
	On-state peak switch current[6]		−400	400	
V_I	Digital input voltage range[3][4]		−0.5	6.5	V
I_{IK}	Digital clamp current	$V_I < 0$	−50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		−100		mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5.5	V
V_+	Supply voltage	0	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	−40	125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TS5A3166-Q1	UNIT
		DCK	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	283.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	60.8	
ψ_{JT}	Junction-to-top characterization parameter	1.7	
ψ_{JB}	Junction-to-board characterization parameter	60.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics for 5-V Supply[1]

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch												
Analog signal range	V_{COM}, V_{NO}					0		V_+	0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100$ mA,	Switch ON, See Figure 13	25°C	4.5 V		0.8	1.1		0.8	1.1	Ω
				Full				1.2			1.44	
ON-state resistance	r_{on}	$V_{NO} = 2.5$ V, $I_{COM} = -100$ mA,	Switch ON, See Figure 13	25°C	4.5 V		0.7	0.9		0.7	0.9	Ω
				Full				1			1.2	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, $I_{COM} = -100$ mA,	Switch ON, See Figure 13	25°C	4.5 V		0.15			0.15		Ω
		$V_{NO} = 1$ V, 1.5 V, 2.5 V, $I_{COM} = -100$ mA,		25°C			0.09	0.15		0.09	0.15	
				Full				0.15			0.18	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 1$ V, $V_{COM} = 4.5$ V, or $V_{NO} = 4.5$ V, $V_{COM} = 1$ V,	Switch OFF, See Figure 14	25°C	5.5 V	–20	4	20	–80	4	80	nA
				Full		–100		100	–400		400	
	$I_{NO(PWROFF)}$	$V_{NO} = 0$ to 5.5 V, $V_{COM} = 5.5$ V to 0,		25°C	0 V	–5	0.4	5	–5	0.4	5	µA
				Full		–15		15	–30		30	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 1$ V, $V_{NO} = 4.5$ V, or $V_{COM} = 4.5$ V, $V_{NO} = 1$ V,	Switch OFF, See Figure 14	25°C	5.5 V	–20	4	20	–80	4	80	nA
				Full		–100		100	–400		400	
	$I_{COM(PWROFF)}$	$V_{COM} = 5.5$ V to 0, $V_{NO} = 0$ to 5.5 V,		25°C	0 V	–5	0.4	5	–5	0.4	5	µA
				Full		–15		15	–30		30	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 1$ V, $V_{COM} = $ Open, or $V_{NO} = 4.5$ V, $V_{COM} = $ Open,	Switch ON, See Figure 15	25°C	5.5 V	–2	0.3	2	–80	0.3	80	nA
				Full		–20		20	–400		400	
COM ON leakage current	$I_{COM(ON)}$	$V_{COM} = 1$ V, $V_{NO} = $ Open, or $V_{COM} = 4.5$ V, $V_{NO} = $ Open,	Switch ON, See Figure 15	25°C	5.5 V	–2	0.3	2	–80	0.3	80	nA
				Full		–20		20	–400		400	
Digital Control Inputs (IN)												
Input logic high	V_{IH}			Full		2.4		5.5	2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	$V_I = 5.5$ V or 0		25°C	5.5 V	–2	0.3	2				nA
				Full		–20		20	–400		400	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 5-V Supply[(1)] (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	5 V	2.5	4.5	7	2.5	4.5	7	ns
				Full	4.5 V to 5.5 V	1.5		7.5	1.5		7.5	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	5 V	6	9	11.5	6	9	11.5	ns
				Full	4.5 V to 5.5 V	4		12.5	4		12.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1$ nF, See Figure 20	25°C	5 V		1			1		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		19			19		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	5 V		18			18		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5			35.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	5 V		35.5			35.5		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	5 V		2			2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	5 V		200			200		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 19	25°C	5 V		–64			–64		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50$ pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	5 V		0.005			0.005		%
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1		0.01	0.1	µA
				Full				0.5			0.8	

7.6 Electrical Characteristics for 3.3-V Supply[(1)]

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch												
Analog signal range	V_{COM}, V_{NO}					0		V_+	0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.1	1.5		1.1	1.5	Ω
				Full				1.7			2.07	
ON-state resistance	r_{on}	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1	1.4		1	1.4	Ω
				Full				1.5			1.8	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		0.3			0.3		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.09	0.15		0.09	0.15	
				Full				0.15			0.18	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–2	0.5	2	–2	0.5	2	nA
				Full		–20		20	–360		360	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–1	0.1	1	–1	0.1	1	µA
				Full		–5		5	–27		27	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–2	0.5	2	–72	0.5	72	nA
				Full		–20		20	–360		360	
	$I_{COM(PWROFF)}$	V_{COM} = 3.6 V to 0, V_{NO} = 0 to 3.6 V,		25°C	0 V	–1	0.1	1	–2	0.1	2	µA
				Full		–5		5	–27		27	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.2	2	–72		72	nA
				Full		–20		20	–360		360	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.2	2	–72		72	nA
				Full		–20		20	–360		360	
Digital Control Inputs (IN)												
Input logic high	V_{IH}			Full		2		5.5	2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2				nA
				Full		–20		20	–360		360	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 3.3-V Supply[(1)] (continued)

$V_+ = 3$ V to 3.6 V, $T_A = -40°C$ to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	3.3 V	2	5	10	2	5	10	ns
				Full	3 V to 3.6 V	1.5		11	1.5		11	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	3.3 V	6.5	9	12	6.5	9	12	ns
				Full	3 V to 3.6 V	4		13	4		13	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1$ nF, See Figure 21	25°C	3.3 V		1			1		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		19			19		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	3.3 V		18			18		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36			36		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	3.3 V		36			36		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	3.3 V		2			2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	3.3 V		200			200		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1$ MHz,	Switch OFF, See Figure 19	25°C	3.3 V		−64			−64		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50$ pF,	$f = 20$ Hz to 20 kHz, See Figure 21	25°C	3.3 V		0.01			0.01		%
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	3.6 V		0.01	0.1		0.01	0.1	μA
				Full				0.25			0.7	

7.7 Electrical Characteristics for 2.5-V Supply[(1)]

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch												
Analog signal range	V_{COM}, V_{NO}				2.3 V	0		V_+	0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.8	2.4		1.8	2.4	Ω
				Full				2.6			3.1	
ON-state resistance	r_{on}	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.2	2.1		1.2	2.1	Ω
				Full				2.4			2.88	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.7			0.7		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.4	0.6		0.4	0.6	
				Full				0.6			0.72	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	–64	0.3	64	nA
				Full		–50		50	–320		320	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2	0.05	2	–2	0.05	2	µA
				Full		–15		15	–24		24	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	–64	0.3	64	nA
				Full		–50		50	–320		320	
	$I_{COM(PWROFF)}$	V_{COM} = 3.6 V to 0, V_{NO} = 0 to 3.6 V,		25°C	0 V	–2	0.05	2	–2	0.05	2	µA
				Full		–15		15	–24		24	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	–64		64	nA
				Full		–20		20	–320		320	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	–64	0.3	64	nA
				Full		–20		20	–320		320	
Digital Control Inputs (IN1, IN2)												
Input logic high	V_{IH}			Full		1.8		5.5	1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2				nA
				Full		–20		20	–320		320	

(1)   The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply[(1)] (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	2.5 V	2	6	10	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	1		12	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	2.5 V	4.5	8	10.5	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	3		15	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1$ nF, See Figure 21	25°C	2.5 V		4			4		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		19.5			19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	2.5 V		18.5			18.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5			36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	2.5 V		36.5			36.5		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	2.5 V		2			2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	2.5 V		150			150		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		–62			–62		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50$ pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	2.5 V		0.02			0.02		%
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02		0.001	0.02	μA
				Full				0.25			0.6	

7.8 Electrical Characteristics for 1.8-V Supply[(1)]

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Analog Switch												
Analog signal range	V_{COM}, V_{NO}					0		V_+	0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq V_{NO} \leq V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		4.2	25		4.2	25	Ω
				Full				30			36	
ON-state resistance	r_{on}	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		1.6	3.9		1.6	3.9	Ω
				Full				4.0			4.8	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq V_{NO} \leq V_+$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		2.8			2.8		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			4.1	22		4.1	22	
				Full				27			32.4	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	–58		58	nA
				Full		–50		50	–320		320	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2		2	–2		2	µA
				Full		–10		10	–22		22	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	–58		58	nA
				Full		–50		50	–320		320	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NO} = 3.6 V to 0,		25°C	0 V	–2		2	–2		2	µA
				Full		–10		10	–22		22	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	–58		58	nA
				Full		–20		20	–320		320	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	–58		58	nA
				Full		–20		20	–320		320	
Digital Control Inputs (IN1, IN2)												
Input logic high	V_{IH}			Full		1.5		5.5	1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2				nA
				Full		–20		20	–320		320	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply[1] (continued)

$V_+ = 1.65$ V to 1.95 V, $T_A = -40°C$ to 85°C (unless otherwise noted))

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	85°C			125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic												
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	1.8 V	3	9	18	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	1		20	
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$,	$C_L = 35$ pF, See Figure 17	25°C	1.8 V	5	10	15.5	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	4		18.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	$C_L = 1$ nF, See Figure 21	25°C	1.8 V		2			2		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		19.5			19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_+$ or GND, Switch OFF,	See Figure 16	25°C	1.8 V		18.5			18.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5			36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See Figure 16	25°C	1.8 V		36.5			36.5		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND,	See Figure 16	25°C	1.8 V		2			2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON,	See Figure 18	25°C	1.8 V		150			150		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		−62			−62		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50$ pF,	f = 20 Hz to 20 kHz See Figure 21	25°C	1.8 V		0.055			0.055		%
Supply												
Positive supply current	I_+	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01		0.001	0.01	µA
				Full				0.15			0.6	

7.9 Typical Characteristics
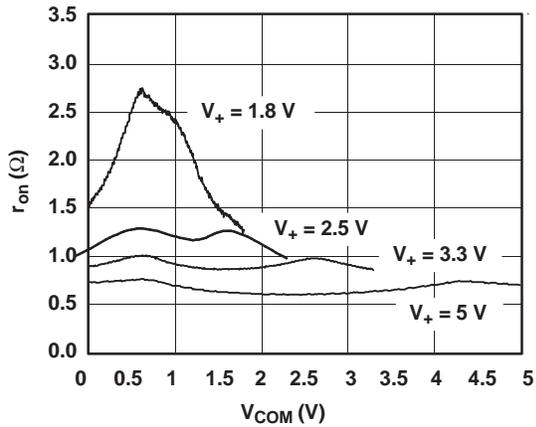
Figure 1. r_{on} vs V_{COM}
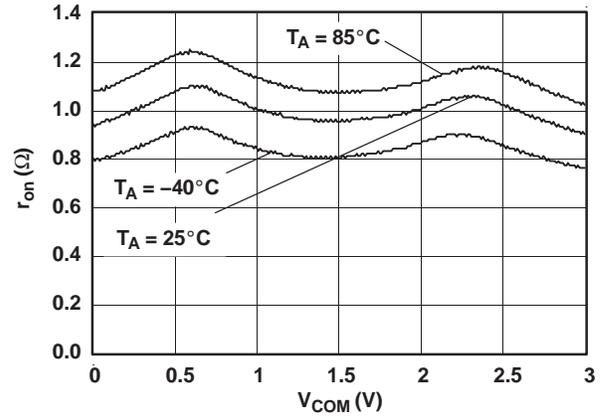
Figure 2. r_{on} vs V_{COM} ($V_+ = 3$ V)
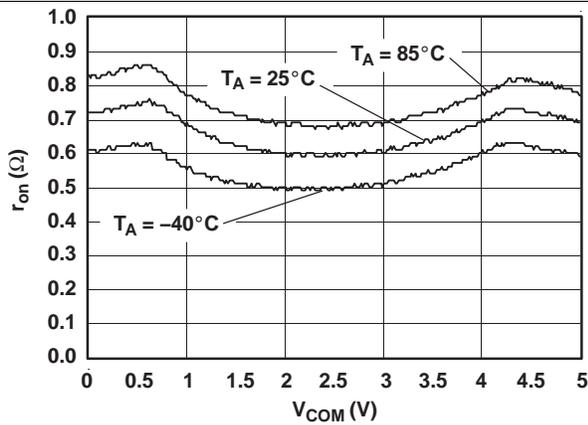
Figure 3. r_{on} vs V_{COM} ($V_+ = 5$ V)
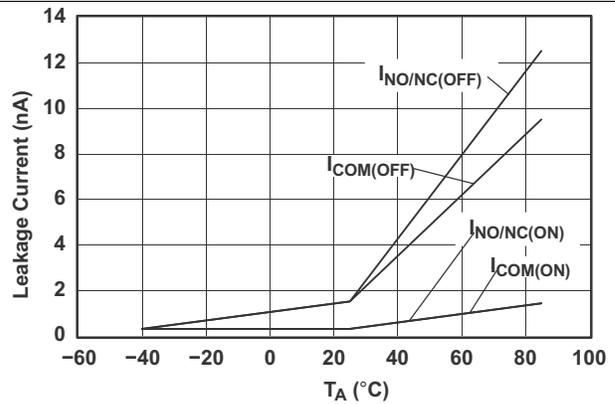
Figure 4. Leakage Current vs Temperature ($V_+ = 5.5$ V)
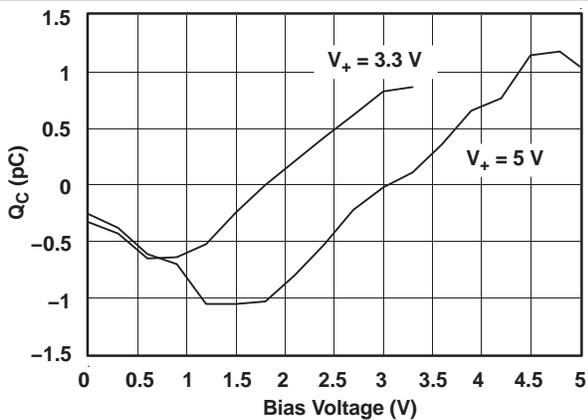

Figure 5. Charge Injection (Q_C) vs V_{COM}
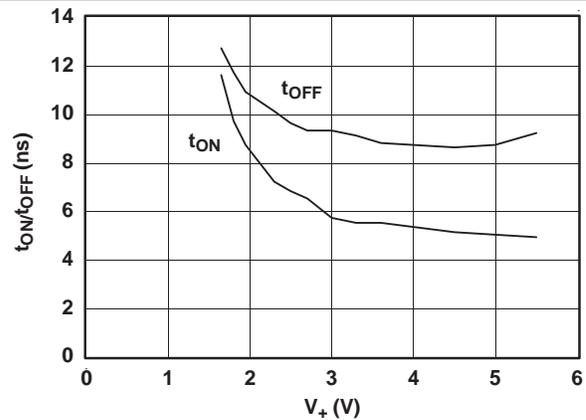
Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)
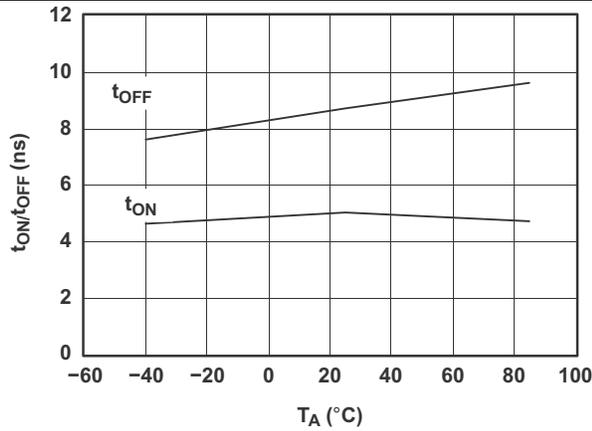

Figure 7. t_ON and t_OFF vs Temperature (V_+ = 5 V)
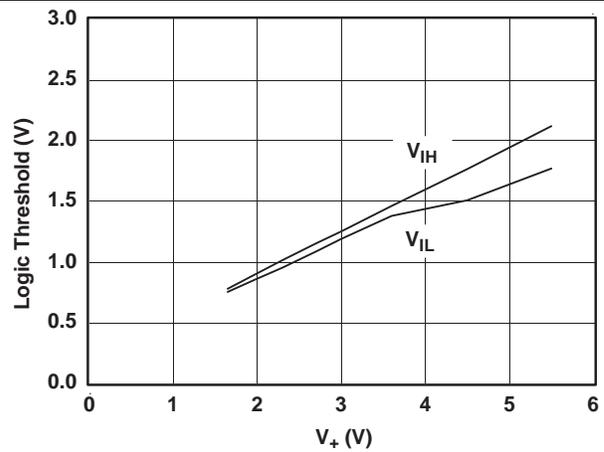

Figure 8. Logic Threshold vs V_+
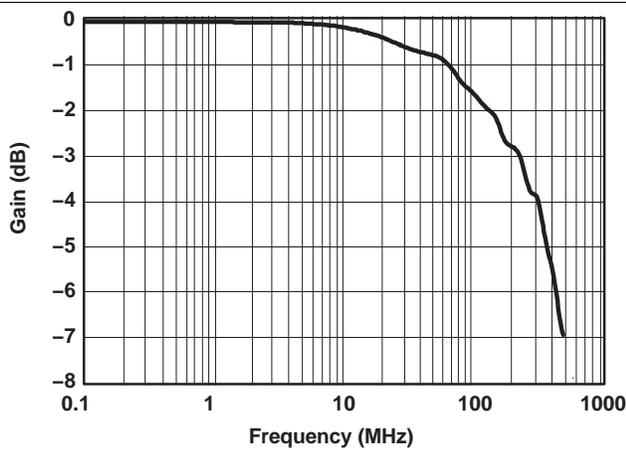
Figure 9. Gain vs Frequency (V_+ = 5 V)
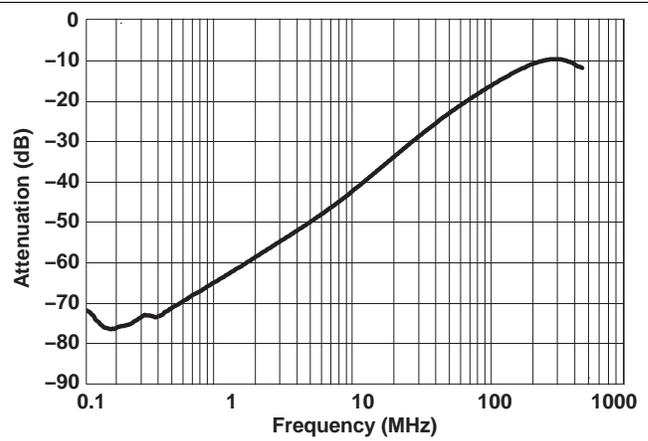
Figure 10. OFF Isolation vs Frequency (V_+ = 5 V)
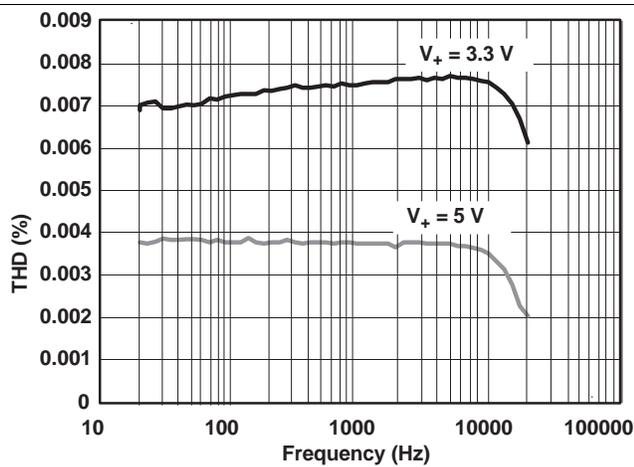
Figure 11. Total Harmonic Distortion vs Frequency
(V_+ = 5 V)
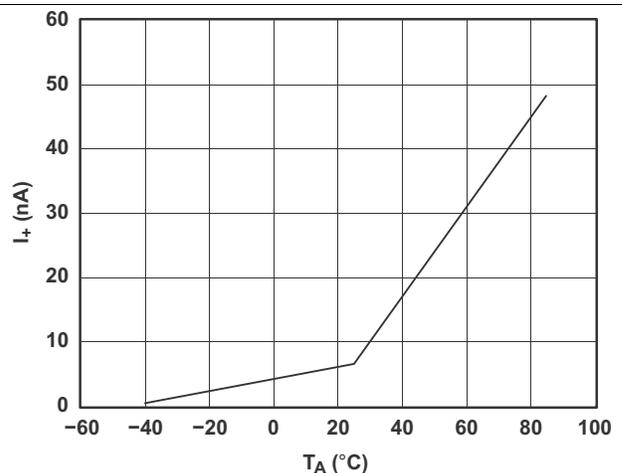
Figure 12. Power-Supply Current vs Temperature
(V_+ = 5 V)

8 Parameter Measurement Information
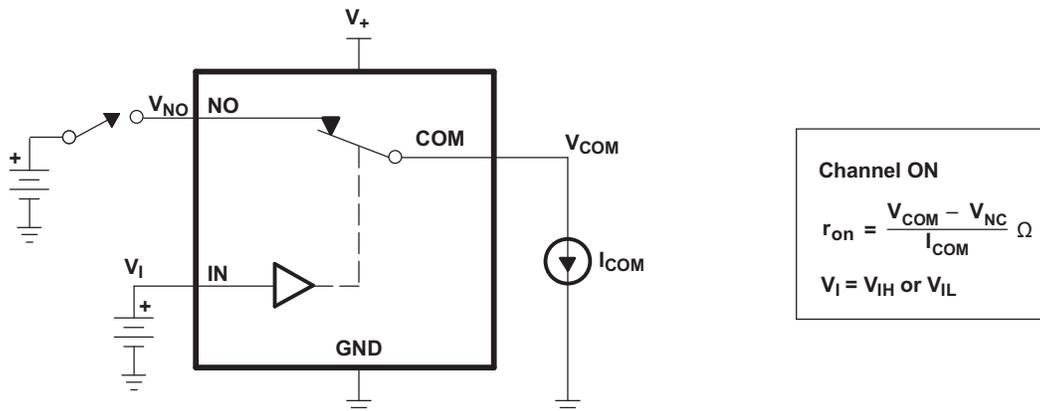
Figure 13. ON-State Resistance (r$_{on}$)

$$r_{on} = \frac{V_{COM} - V_{NC}}{I_{COM}} \; \Omega$$

Channel ON

$V_I = V_{IH}$ or V_{IL}
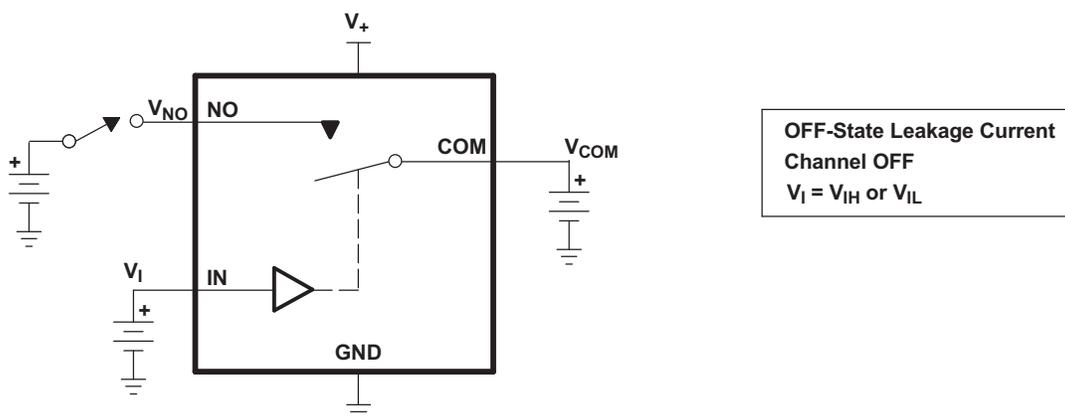
Figure 14. OFF-State Leakage Current (I$_{COM(OFF)}$, I$_{NO(OFF)}$, I$_{COM(PWROFF)}$, I$_{NO(PWR(FF))}$)

OFF-State Leakage Current
Channel OFF
$V_I = V_{IH}$ or V_{IL}
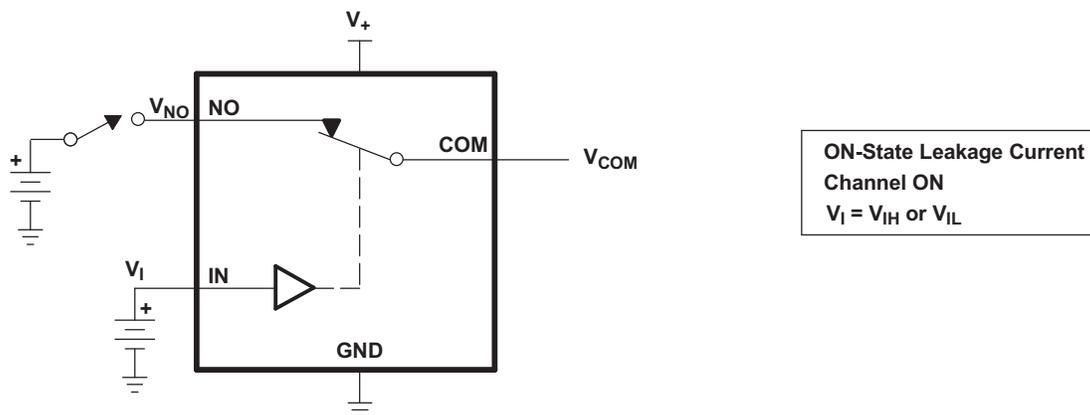
Figure 15. ON-State Leakage Current (I$_{COM(ON)}$, I$_{NO(ON)}$)

ON-State Leakage Current
Channel ON
$V_I = V_{IH}$ or V_{IL}

Parameter Measurement Information (continued)

V_BIAS = V_+ or GND

V_I = V_IH or V_IL

Capacitance is measured at NO, COM, and IN inputs during ON and OFF conditions.
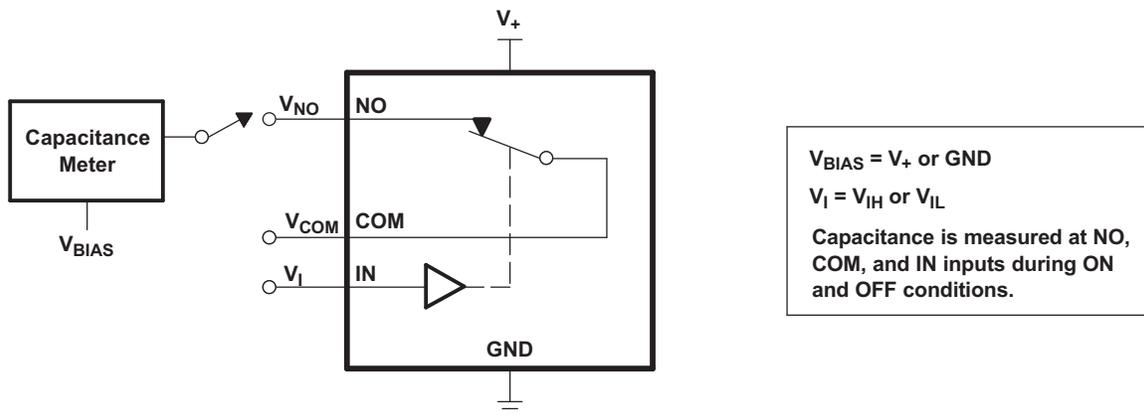
Figure 16. Capacitance (C_I, C_COM(OFF), C_COM(ON), C_NO(OFF), C_NO(ON))

TEST	R_L	C_L	V_COM
t_ON	50 Ω	35 pF	V_+
t_OFF	50 Ω	35 pF	V_+
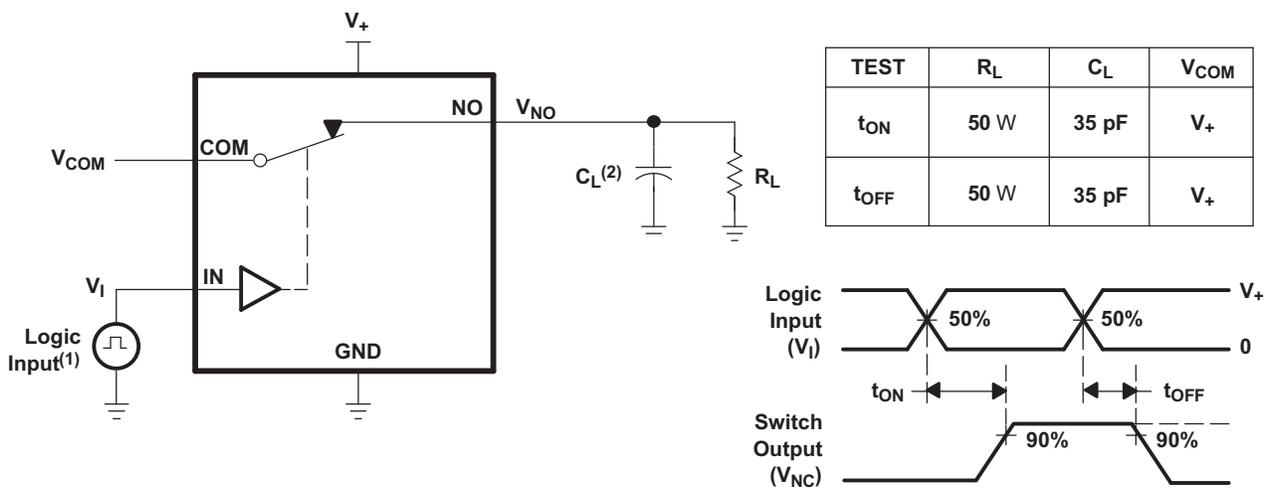
(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_ON) and Turn-Off Time (t_OFF)

Channel ON: NO to COM

V_I = V_+ or GND

Network Analyzer Setup

Source Power = 0 dBm (632-mV P-P at 50-Ω load)

DC Bias = 350 mV
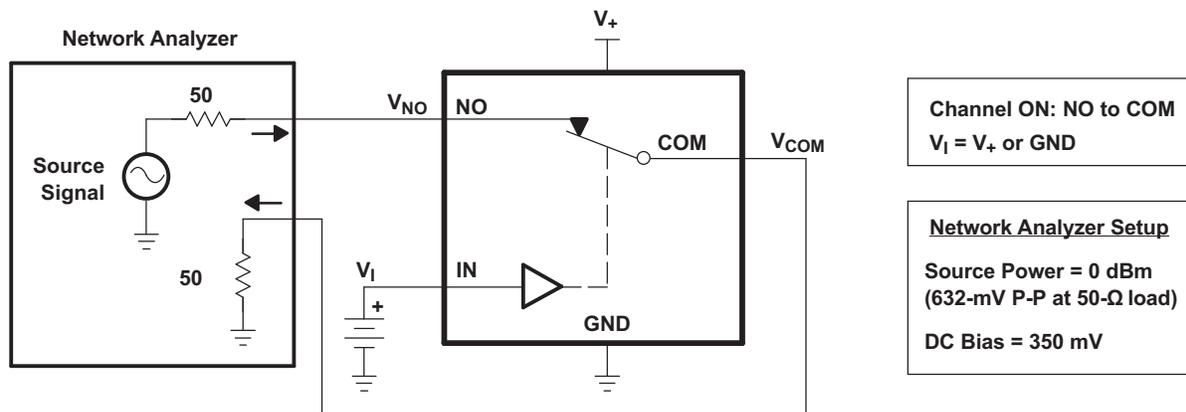
Figure 18. Bandwidth (BW)

Parameter Measurement Information (continued)
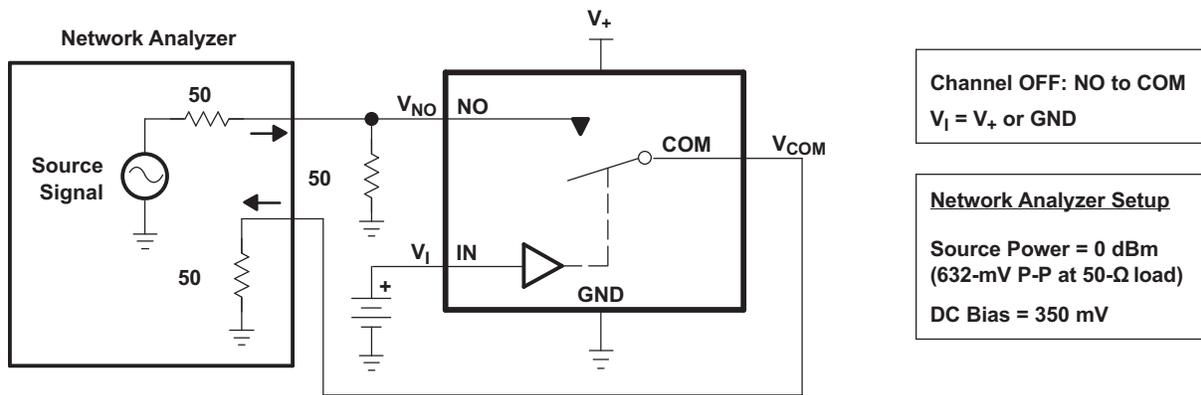

Figure 19. OFF Isolation (O_{ISO})
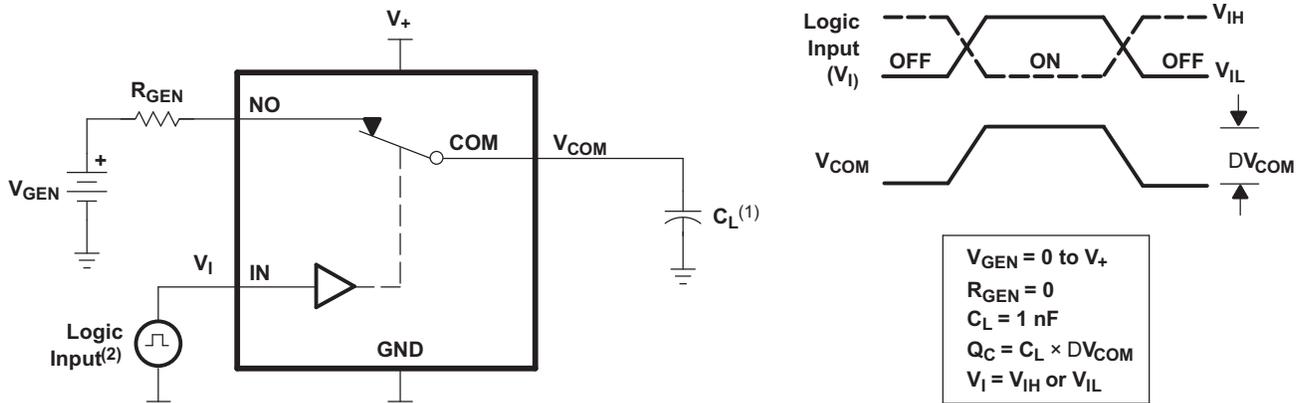
(1) C_L includes probe and jig capacitance.

(2)   All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 20. Charge Injection (Q_C)
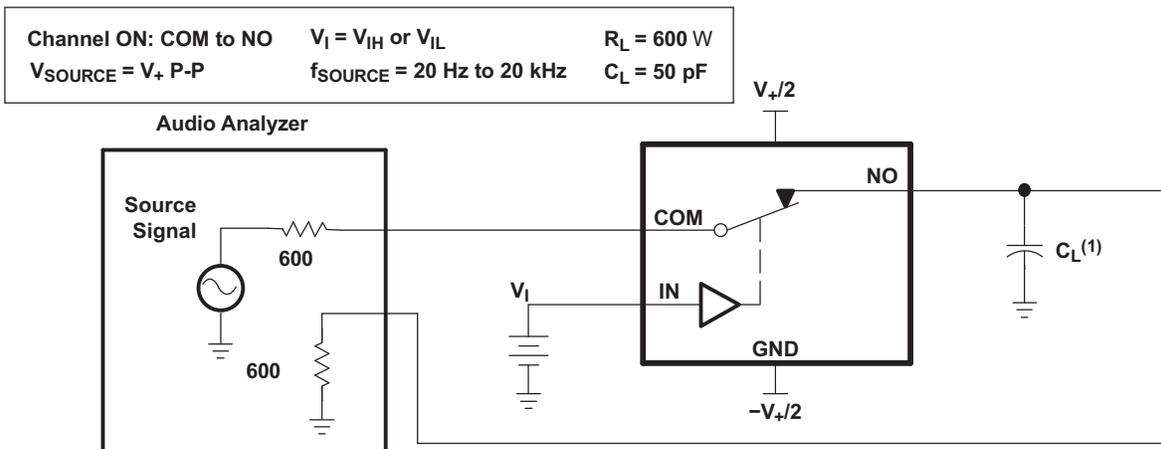
(1) C_L includes probe and jig capacitance.

Figure 21. Total Harmonic Distortion (THD)

9 Detailed Description

9.1 Overview

Table 1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

9.2 Functional Block Diagram
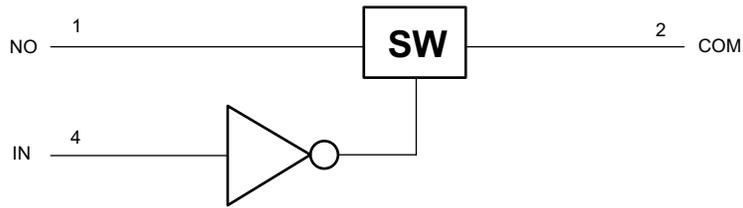
9.3 Feature Description

Table 2. Summary Of Characteristics[1]

Configuration	Single Pole Single Throw (SPST)
Number of channels	1
ON-state resistance (r_{on})	0.9 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	7.5 ns/12.5 ns
Charge injection (Q_C)	1 pC
Bandwidth (BW)	200 MHz
OFF isolation (O_{ISO})	–64 dB at 1 MHz
Total harmonic distortion (THD)	0.005%
Leakage current ($I_{COM(OFF)}$)	±4 nA
Power-supply current (I_+)	0.5 µA
Package option	5-pin DSBGA, SOT-23, or SC-70

(1) V_+ = 5 V, T_A = 25°C

9.4 Device Functional Modes

Table 3. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

10 Application and Implementation

10.1 Application Information

SPST analog switch is a basic component that could be used in any electrical system design. The following are some basic applications that utilize the TS5A3166, more detailed applications may be found in the *Typical Application* section.

1. Gain-control circuit for amplifier
   (a) Additional details are available in the *Typical Application* section.
2. Improve lock time of a PLL by changing the time constant
   (a) Example Diagram:
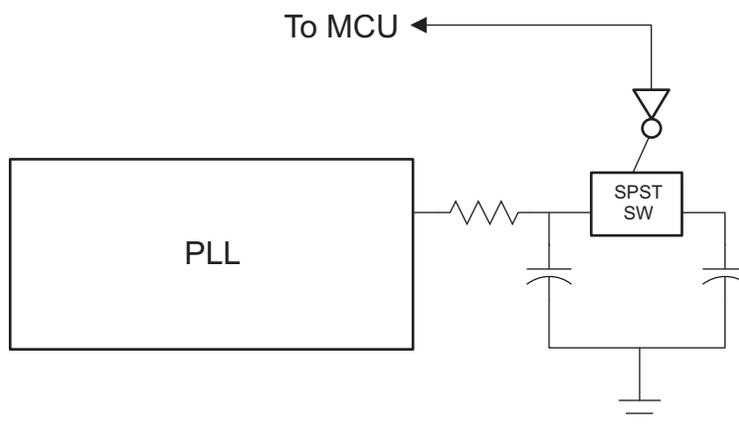
Figure 22. Improved Lock Time Circuit Simplified Block Diagram

1. Improve power consumption for PLL
   (a) Example Diagram:
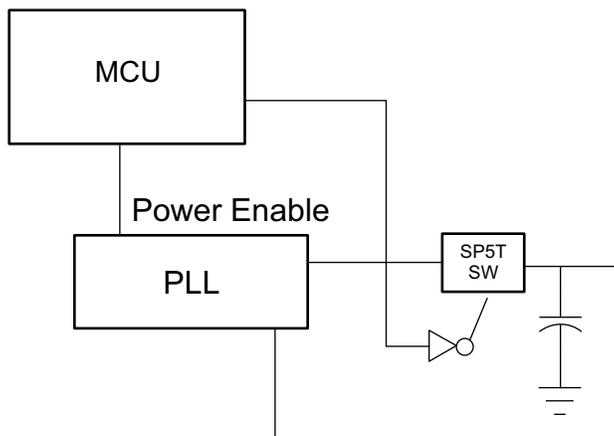
Figure 23. PLL Improved Power Consumption Simplified Block Diagram

10.2 Typical Application
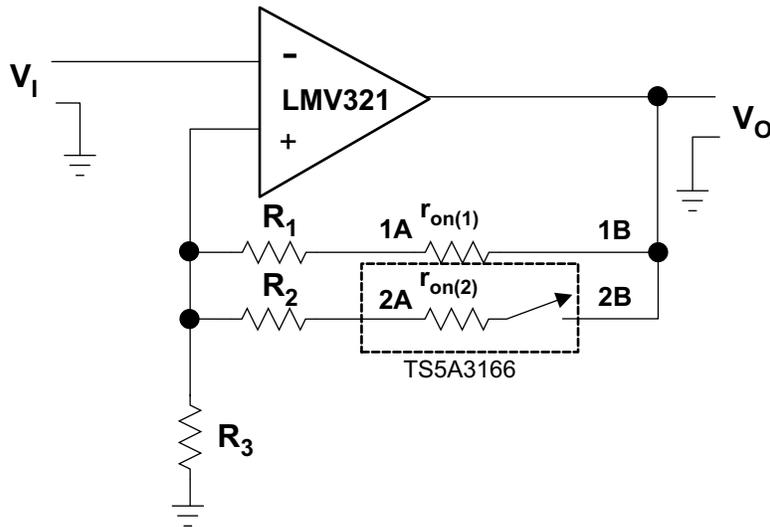
Figure 24. Gain-Control Circuit for OP Amplifier

10.2.1 Design Requirements

Place a switch in series with the input of the op amp. Since the op amp input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

### 10.2.2 Detailed Design Procedure

By choosing values of R1 and R2, such that $Rx >> r_{on(x)}$, r_{on} of TS5A3166 can be ignored. The gain of op amp can be calculated as follow:

$$Vo / VI = 1 + R|| / R3 \tag{1}$$

$$R|| = (R1 + r_{on(1)}) \,||\, (R2 + r_{on(2)}) \tag{2}$$

10.2.3 Application Curves
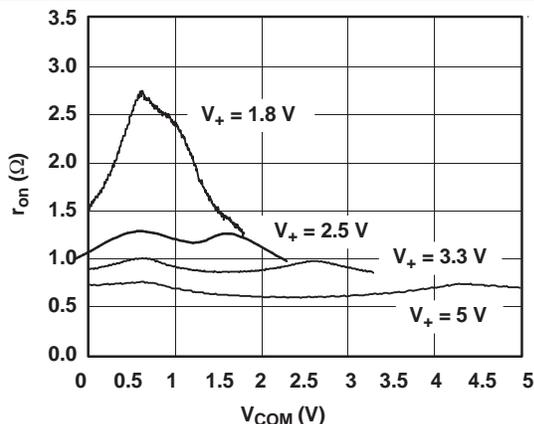
Figure 25. r_{on} vs V_{COM}
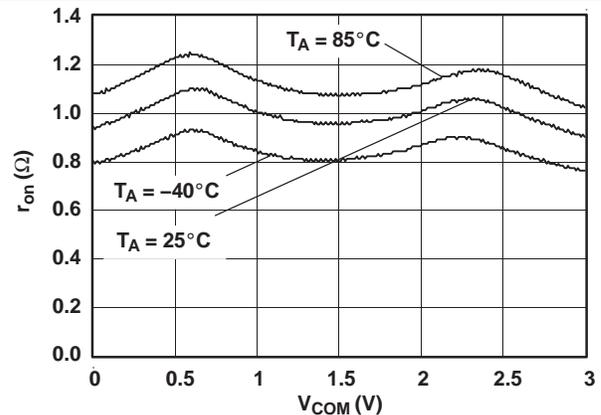
Figure 26. r_{on} vs V_{COM} (V_+ = 3 V)

21

Typical Application (continued)
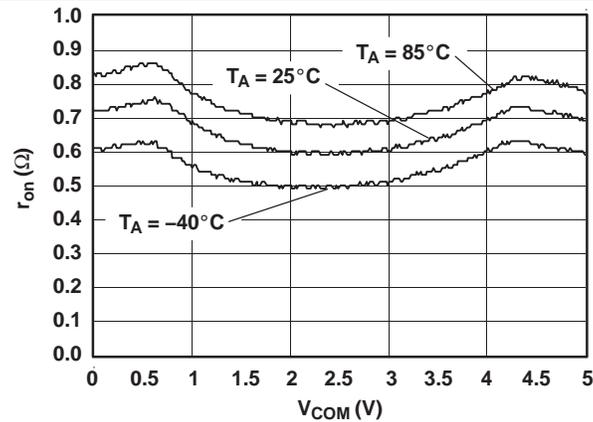
Figure 27. r_on vs V_COM (V_+ = 5 V)

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each Vcc terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF bypass capacitor is recommended. If there are multiple Vcc terminals then a 0.01 µF or 0.022 µF capacitor is recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 µF and 1 µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. Below figure shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

12.2 Layout Example
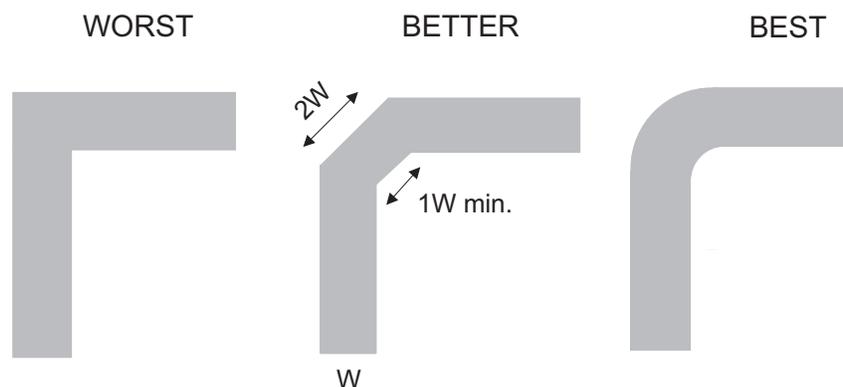
Figure 28. Trace Example

## 13 器件和文档支持

13.1 商标

All trademarks are the property of their respective owners.

13.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

产品		应用	
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3166QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
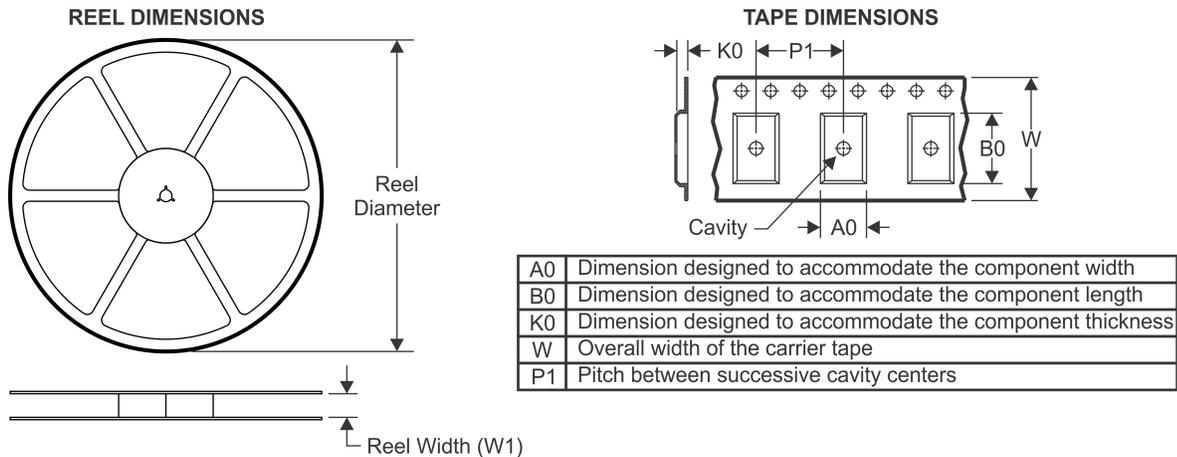
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
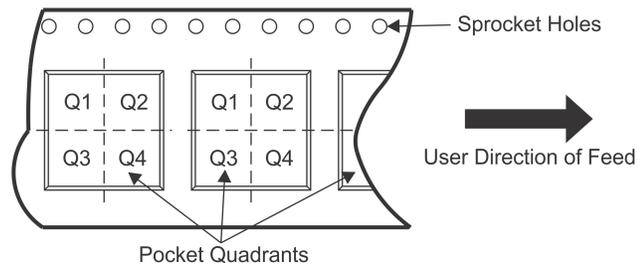
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3166QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS
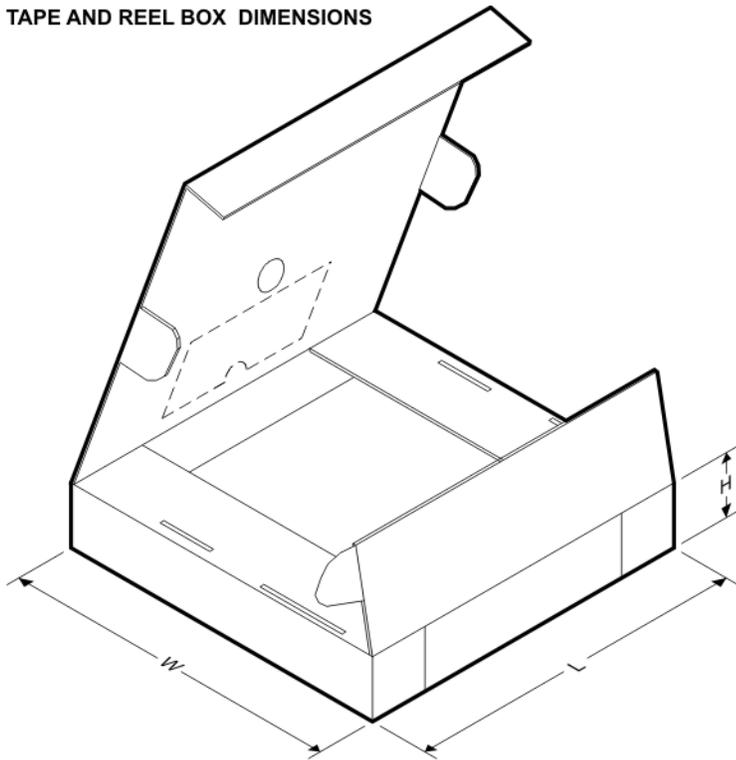
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3166QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0

DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE
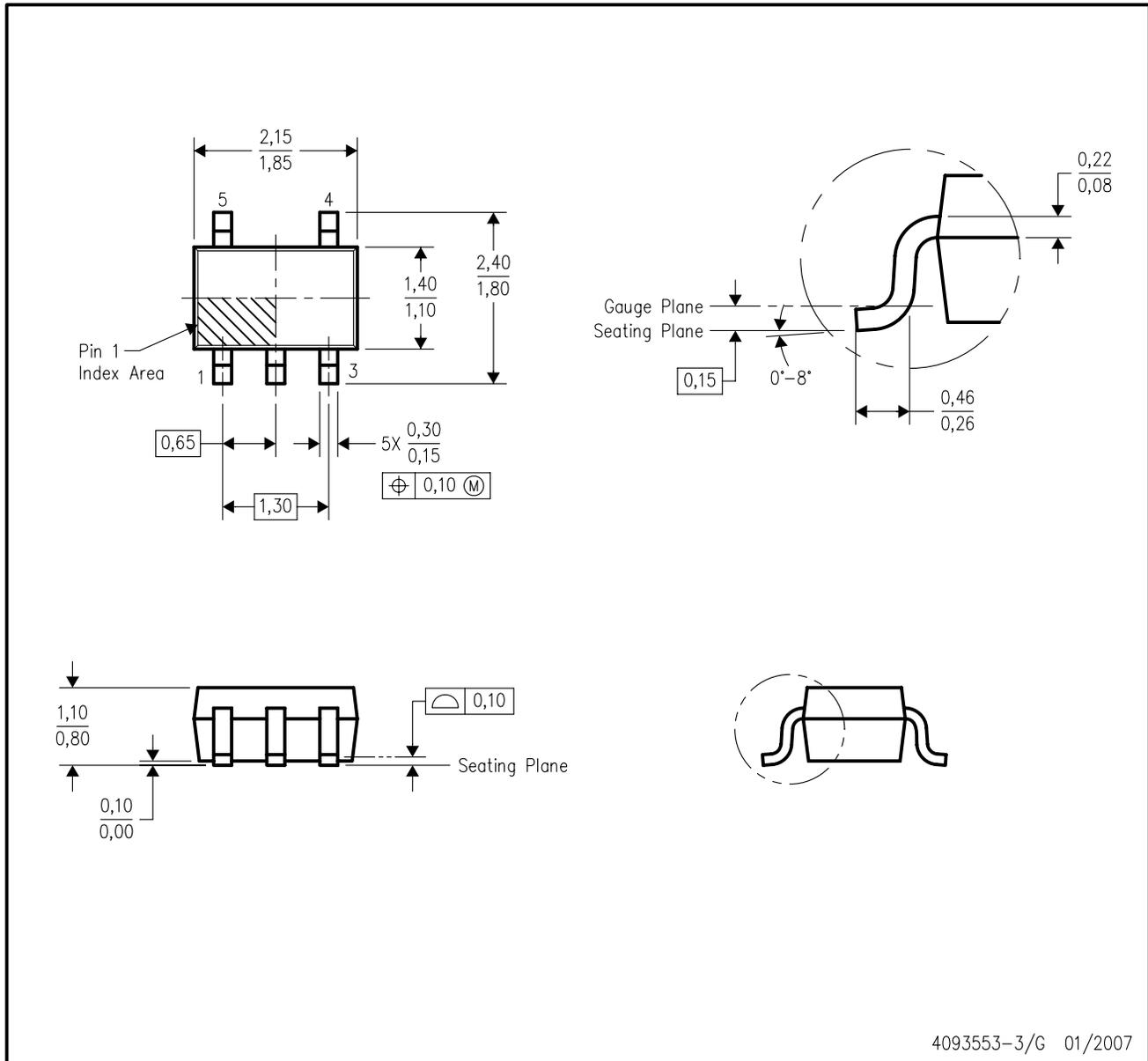
2,15
1,85

5   4

1,40
1,10

2,40
1,80

Pin 1
Index Area   1   2   3

0,65

5X 0,30
0,15

⊕ 0,10 Ⓜ

1,30

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
0,80

⌓ 0,10

Seating Plane

0,10
0,00

4093553−3/G 01/2007

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
        D. Falls within JEDEC MO−203 variation AA.

DCK (R-PDSO-G5)   PLASTIC SMALL OUTLINE
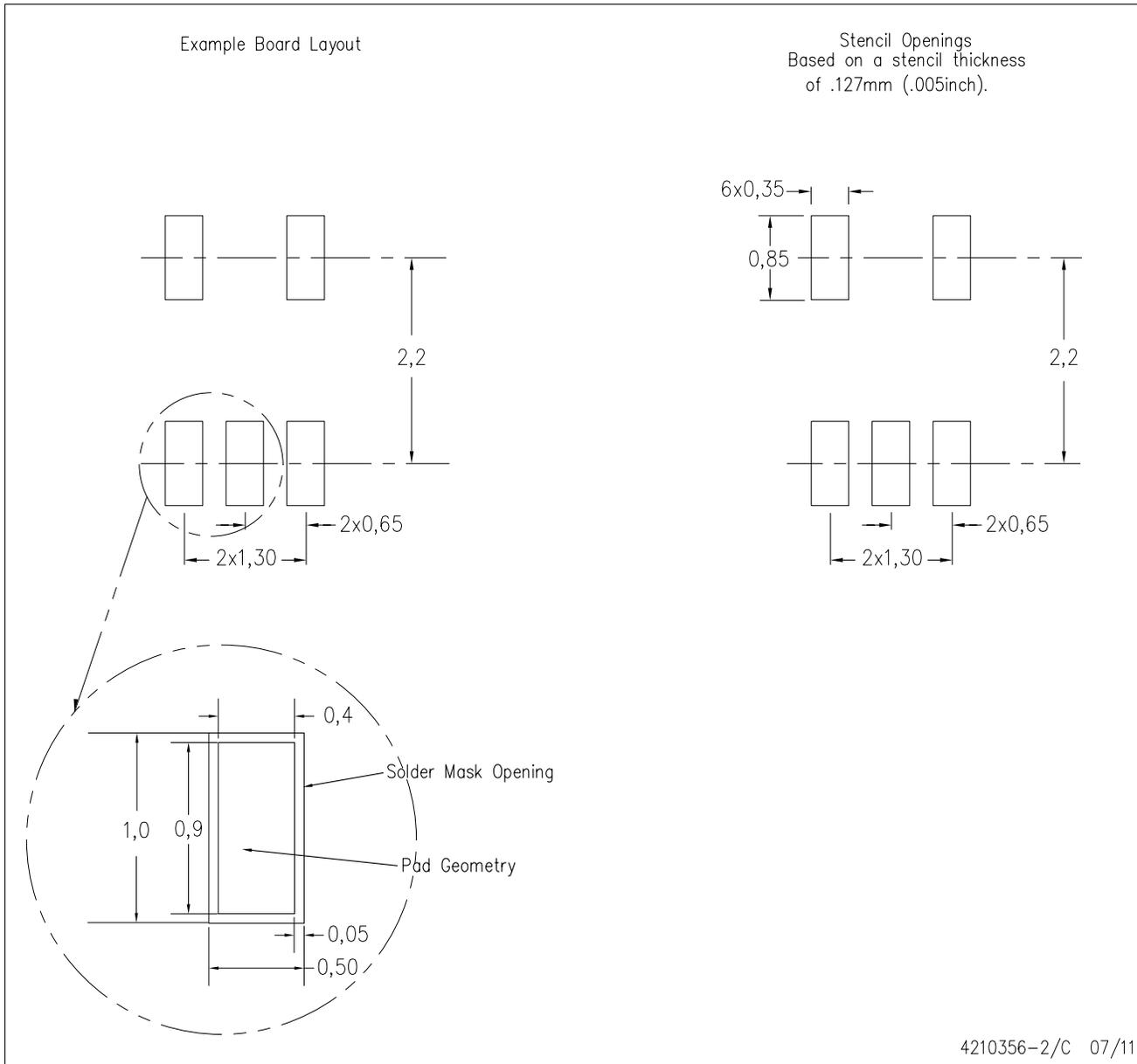
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

2x0,65

2x0,65

2x1,30

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356-2/C 07/11

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
          D. Publication IPC-7351 is recommended for alternate designs.
          E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

重要声明和免责声明