IEEE 1394-1995 and P1394a Compliant General-Purpose Link-Layer Controller for Computer Peripherals and Consumer Audio/Video Electronics

FEATURES

- **Compliant With IEEE 1394-1995 Standards and 1394a-2000 Supplement for High Performance Serial Bus[1]**
- **Supports Transfer Rates of 400, 200, or 100 Mbps**
- **Compatible With Texas Instruments Physical Layer Controllers (Phys)**
- **Supports the Texas Instruments Bus Holder Galvanic Isolation Barrier**
- **Glueless Interface to 68000 and ColdFire Microcontrollers/Microprocessors**
- **Supports ColdFire Burst Transfers**
- **2-Kbyte General Receive FIFO (GRF) Accessed Through Microcontroller Interface Supports Asynchronous and Isochronous Receive.**
- **2-Kbyte Asynchronous Transmit FIFO (ATF) Accessed Through Microcontroller Interface Supports Asynchronous Transmissions.**
- **Programmable Microcontroller Interface With 8-Bit or 16-Bit Data Bus, Multiple Modes of Operation Including Burst Mode, and Clock Frequency to 60 MHz**
- **8-Bit or 16-Bit Data-Mover Port (DM Port) Supports Isochronous, Asynchronous, and Asynchronous Streaming Transmit/Receive From an Unbuffered Port at a Clock Frequency of 25 MHz.**
- **Backward Compatible With All TSB12LV31(GPLynx) Microcontroller and Data-Mover Functionality in Hardware**
- **Two-Channel Support for Isochronous Receive to Unbuffered 8/16 Data-Mover Port**
- **Four-Channel Support for Isochronous Transmit From Unbufferred 8/16 Bit Data-Mover Port**
- **Single 3.3-V Supply Operation With 5-V Tolerance Using 5-V Bias Terminals**
- **High Performance 100-Pin PZ Package**

NOTE: Implements technology covered by one or more patents of Apple Computer, Incorporated and SGS Thomson, Limited.

DESCRIPTION

The TSB12LV32 (GP2Lynx) is a high-performance general-purpose IEEE 1394a-2000 link-layer controller (LLC) with the capability of transferring data between the 1394 Phy-link interface, an external host controller, and an external device connected to the data-mover port (local bus interface). The 1394 Phy-link interface provides the connection to a 1394 physical layer device and is supported by the LLC. The LLC provides the control for transmitting and receiving 1394 packet data between the microcontroller interface and the Phy-link interface via internal 2-Kbyte FIFOs at rates up to 400 Mbps. The TSB12LV32 transmits and receives correctly formatted 1394 packets, generates and detects the 1394 cycle start packets, communicates transaction layer transmit requests to the Phy, and generates and inspects the 32-bit cyclic redundancy check (CRC).

The TSB12LV32 is capable of being 1394 cycle master (CM), 1394 bus manager, 1394 isochronous resource manager (IRM) if additional control status registers (CSRs) are added via the external host controller, and supports reception of 1394 isochronous data on two channels and transmission of 1394 isochronous data on four channels.

The TSB12LV32 supports a direct interface to many microprocessors/microcontrollers by including programmable endian swapping. TSB12LV32 has a generic 16-/8-bit host bus interface which includes support for a ColdFireE microcontroller mode at rates up to 60 MHz. The microcontroller interface can operate in byte or word (16 bit) accesses.

The data-mover block in GP2Lynx handles the external memory interface of large data blocks. This local bus interface can be configured either to transmit or receive data packets. The packets can be either asynchronous, isochronous, or asynchronous streaming data packets. The data-mover (DM) port can receive any type of packet, but it can only transmit one type of packet at a time: isochronous data packets, asynchronous data packets, or asynchronous stream data packets.

The internal FIFO is separated into an asynchronous transmit FIFO (ATF) and a general receive FIFO (GRF), each of 520 quadlets (2 Kbytes). Asynchronous and/or isochronous receive packets can be routed to either the DM port or the GRF via the receiver routing control logic. Asynchronous data packets or asynchronous stream data packets can be transmitted from the DM port or the internal FIFO: ATF. If there is contention the ATF has priority and is transmitted first. Isochronous packets can only be transmitted by the data-mover port.

The LLC also provides the capability to receive status information from the physical layer device and to access the physical layer control and status registers by the application software.

NOTE:

This product is for high-volume applications only. For a complere datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSB12LV32PZ	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TSB12LV32 F711538A	Samples
TSB12LV32PZG4	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TSB12LV32 F711538A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

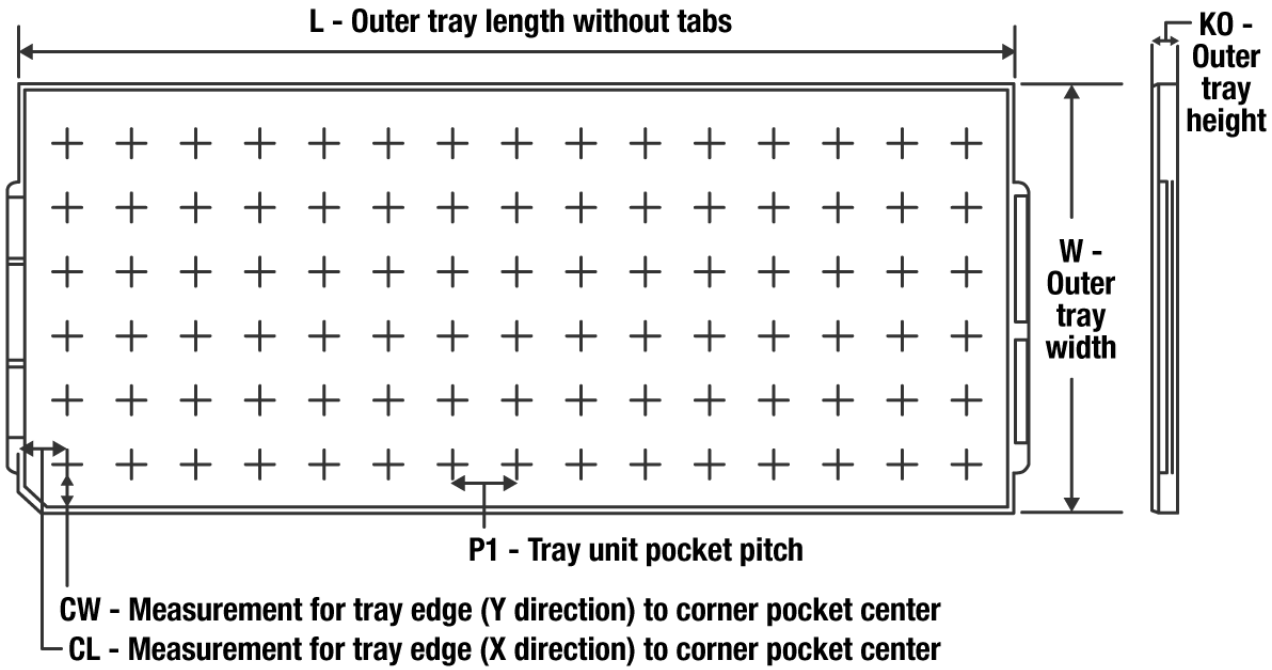
OTHER QUALIFIED VERSIONS OF TSB12LV32 :

- Enhanced Product: TSB12LV32-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TSB12LV32PZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TSB12LV32PZG4	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4

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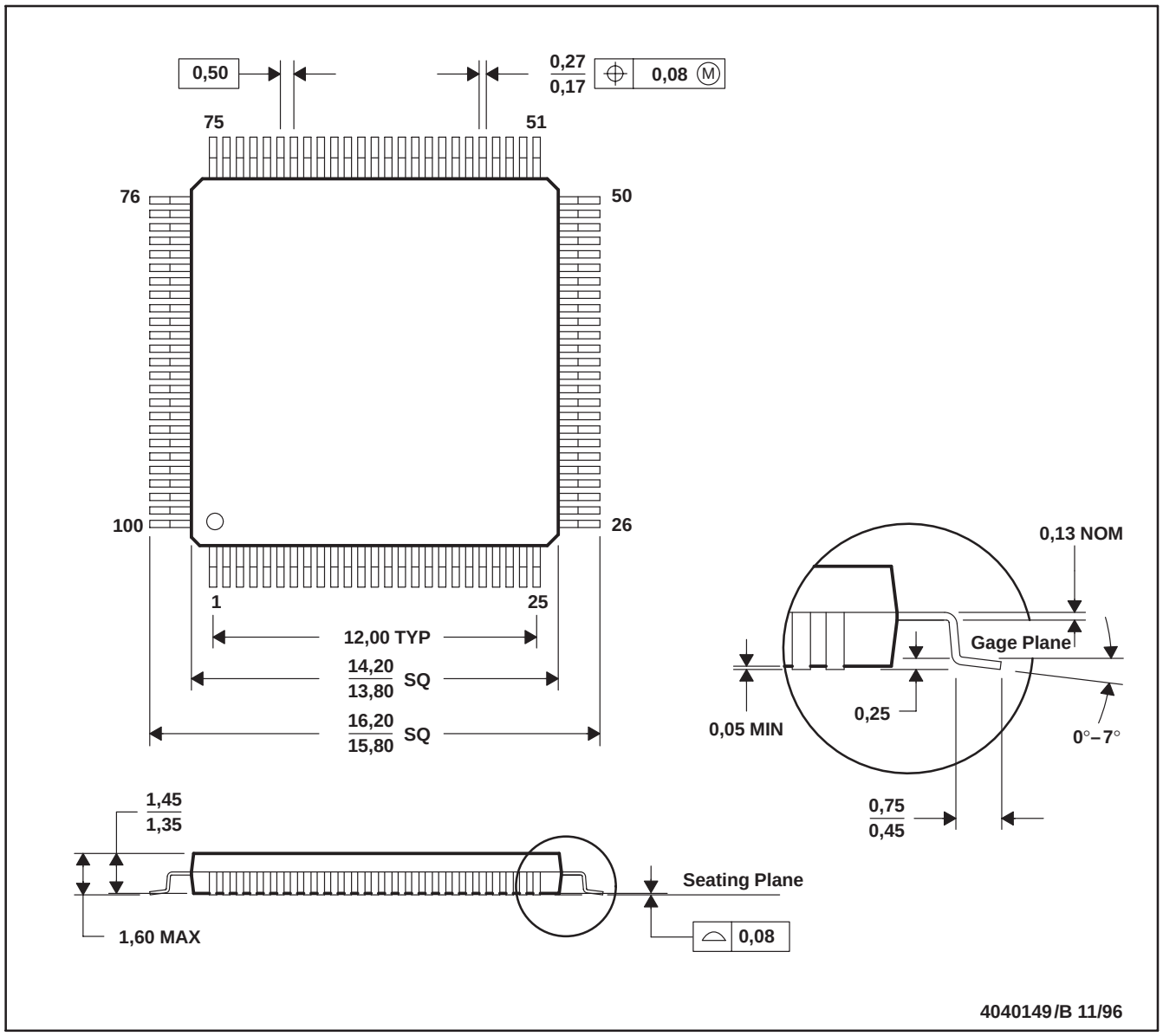
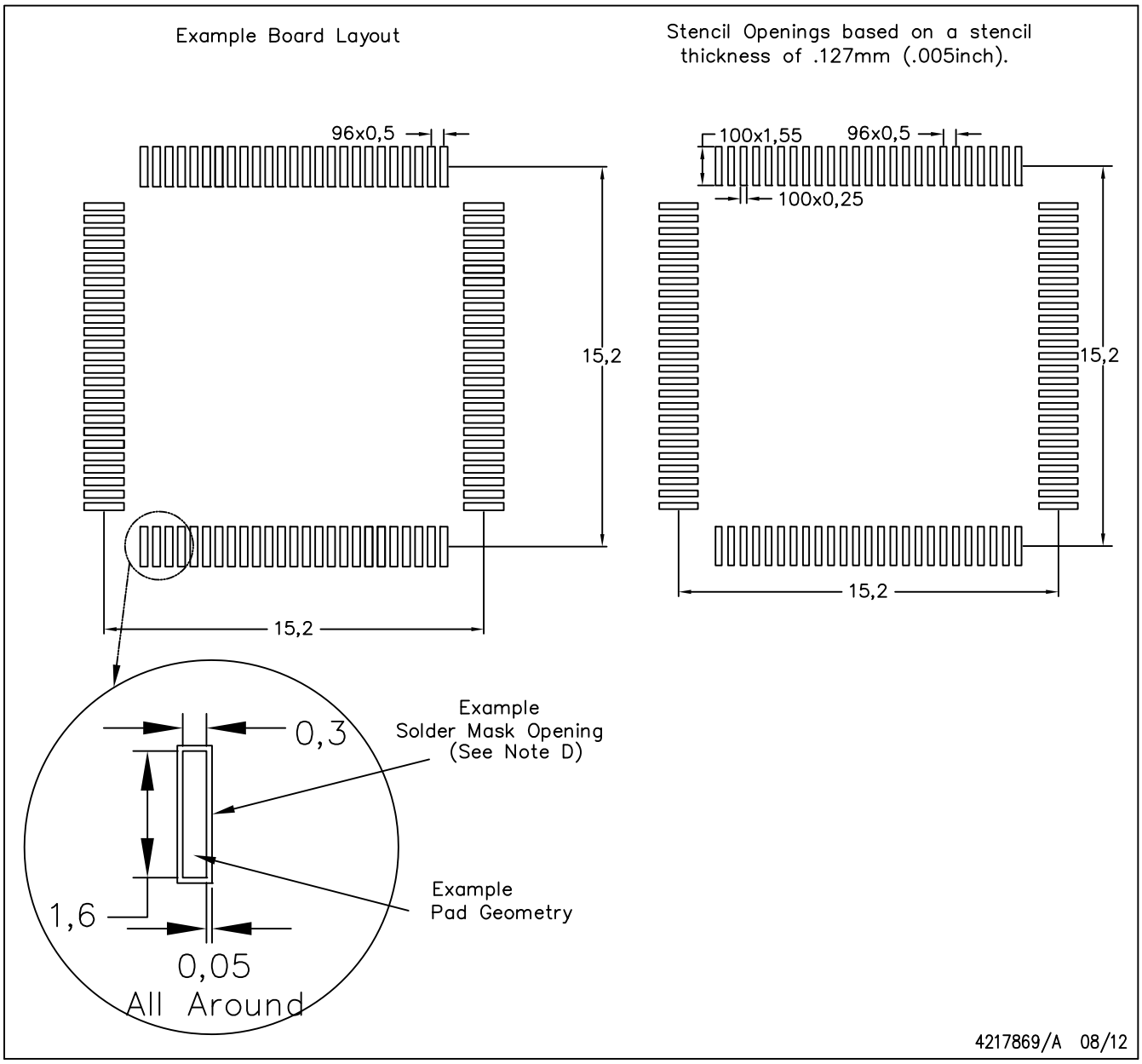
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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