# 同步降压功率级

查询样片: **UCD74106**

## 特性

- 具有单相位与多相位同步降压转换器驱动器的全集成电源开关
- 与 **TI Fusion** 数字电源控制器完全兼容，（**UCD91xx** 和 **UCD92xx** 系列）
- 与模拟域控制器兼容
- 宽泛的输入电压：
  - **4.5V** 至 **18V**
  - 支持外部偏置电源，低至 **2.2V** 的工作输入电压
- 高达 **6A** 的输出电流
- 工作开关频率 **2MHz**
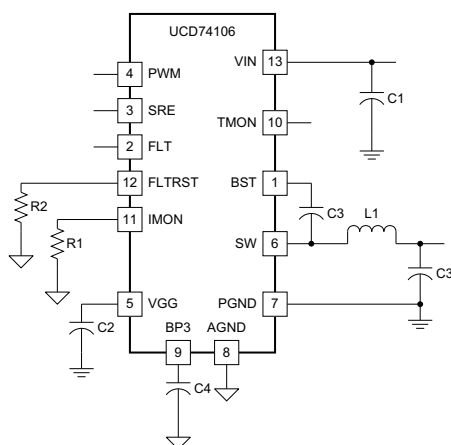- 具有电流限制标记的电流限值
- **VIN** 提供板载经稳压 **6V** 驱动器电源
- 热保护及监控

## 应用范围

- 单相位与多相位应用的数控同步降压功率级
- 台式机、服务器、电信以及笔记本应用的小型高效稳压器
- 同步降压功率级

## 描述

UCD74106 是一款可驱动降压电源的完整电源系统 (Figure 1)。 在一个单片解决方案中全面集成高侧 MOSFET，低侧金属氧化物半导体场效应晶体管 (MOSFET)，驱动器，电流感测电路以及必要的保护功能，以有助于实现最小尺寸与最高效率。 驱动器电路可在同步降压电路中为高侧 NMOS 开关和低侧 NMOS 同步整流器提供高充电及放电电流。 MOSFET 栅极由内部已稳压 $V_{GG}$ 电源驱动至 6.25V。 可禁用内部 $V_{GG}$ 稳压器，以允许用户提供一个独立的栅极驱动电压。 这种高灵活性支持 2.2V 至 18V 的宽功率转换输入电压。内部欠压闭锁 (UVLO) 逻辑可在允许芯片工作之前确保 $V_{GG}$ 正常。

驱动逻辑模块可支持两个工作模式中的一个。 在同步模式下，该逻辑模块可使用 PWM 信号来控制高侧与低侧栅极驱动信号。 已优化死区时间以防止交叉传导。 同步整流器使能 (SRE) 引脚在 PWM 信号为低电平时控制低侧 MOSFET 是否打开。

### 简化应用示意图

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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English Data Sheet: SLUSAJ5

## DESCRIPTION (CONT.)

On-board current sense amplifiers monitor the current to safeguard the power stage from sudden high current loads. In the event of an over-current fault, the output power stage is turned off and the Fault Flag (FLT) is asserted to alert the controller.

Output current is measured and monitored by a precision integrated current sense element. This method provides an accuracy of ±5%. The amplified signal is available for use by the controller on the IMON pin. The IMON pin has a positive offset so that both positive (sourcing) and negative (sinking) current can be sensed.

If the die temperature exceeds 150°C, the temperature sensor initiates a thermal shutdown that halts output switching and sets the FLT flag. Normal operation resumes when the die temperature falls below the thermal hysteresis band and the Fault Flag is re-set by the controller.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### Table 1. ORDERING INFORMATION

| OPERATING TEMPERATURE RANGE, $T_A$ | PIN COUNT | ORDERABLE PART NUMBER | SUPPLY | PACKAGE | TOP SIDE MARKING |
|---|---|---|---|---|---|
| −40°C to 125°C | 13-pin | UCD74106RGMR | Reel of 2500 | QFN | UCD74106 |
| | | UCD74106RGMT | Reel of 250 | | |

## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, VIN | | -0.3 | 20 | V |
| Boot voltage, BST | DC | -0.3 | SW + 7 | |
| | AC [2] | | 34 | |
| Gate supply voltage, VGG | | -0.3 | 7 | |
| Switch voltage, SW | DC | -2 | VIN + 1 | |
| | AC [2] | | 34 | |
| Analog outputs, TMON, IMON | | -0.3 | 3.6 | |
| Digital I/O's, PWM, SRE, FLT, FLTRST | | -0.3 | 5.5 | V |
| Junction temperature, $T_J$ | | -55 | 150 | °C |
| Storage temperature, $T_{stg}$ | | -65 | 150 | |
| ESD rating, Human Body Model (HBM) | | | 2000 | V |
| ESD rating, Charged Device Model (CDM) | | | 500 | |
| Lead temperature | Reflow soldering, 10 sec | | 300 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult company packaging information for thermal limitations and considerations of packages.

(2) AC levels are limited to within 5 ns.

## THERMAL INFORMATION

| THERMAL METRIC[1] | | UCD74106 RGM 13 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance[2] | 70.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance[3] | 47.3 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance[4] | 11.0 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter[5] | 0.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter[6] | 11.0 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance[7] | 0.9 | |

(1) 有关传统和新的热 度量的更多信息，请参阅IC 封装热度量应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， $\psi_{JT}$，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 $\theta_{JA}$。
(6) 结至电路板特征参数， $\psi_{JB}$，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 $\theta_{JA}$。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Power input voltage | Internally generated VGG | 4.5 | 12 | 18 | V |
| | | Externally supplied VGG | 2.2 | 12 | 18 | |
| $V_{GG}$ | Externally supplied gate drive voltage | | 4.5 | 6.2 | | |
| $T_J$ | Operating junction temperature range | | -40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 12 V; 1 μF from BP3 to GND, 0.22 μF from BST to SW, 4.7 μF from VGG to PGND, $T_A$ = $T_J$ = -40°C to 125°C (unless otherwise noted).

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| | Supply current | Outputs not switching, $V_{IN}$ = 2.2 V, $V_{GG}$ = 5 V | | 4 | | mA |
| | Supply current | Outputs not switching, $V_{IN}$ = 12 V, | | 4 | | |
| **Gate Drive Under Voltage Lockout** | | | | | | |
| | VGG UVLO ON | BP3 rising | | 4.0 | | V |
| | VGG UVLO OFF | BP3 falling | | 3.8 | | |
| | VGG UVLO hysteresis | | | 200 | | mV |
| **VGG Supply Generator** | | | | | | |
| | VGG | $V_{IN}$ = 7 to 14 V | 5.2 | 6.25 | 6.8 | V |
| | VGG drop out | $V_{IN}$ = 4.5 to 7 V, $I_{VGG}$ < 20 mA | | | 200 | mV |
| **BP3 Supply Voltage** | | | | | | |
| | BP3 | $I_{DD}$ = 0 to 10 mA | 3.15 | 3.3 | 3.45 | V |
| **Input Signal (PWM, SRE)** | | | | | | |
| $V_{IH}$ | Positive-going input threshold voltage | | | | 2.3 | |
| $V_{IL}$ | Negative-going input threshold voltage | | 1 | | | V |
| | Tristate condition | | 1.4 | | 1.9 | |
| $t_{HLD\_R}$ | 3-state hold-off time | $V_{PWM}$ = 1.65 V | | | 200 | ns |
| | $I_{PWM}$ input current | $V_{PWM}$ = 5.0 V | | 250 | | |
| | | $V_{PWM}$ = 3.3 V | | 165 | | |
| | | $V_{PWM}$ = 0 V | | -165 | | |
| | $I_{SRE}$ input current | $V_{SRE}$ = 5.0 V | | 1 | | μA |
| | | $V_{SRE}$ = 3.3 V | | 1 | | |
| | | $V_{SRE}$ = 0 V | | 1 | | |

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 12 V; 1 µF from BP3 to GND, 0.22 µF from BST to SW, 4.7 µF from VGG to PGND, $T_A$ = $T_J$ = -40°C to 125°C (unless otherwise noted).

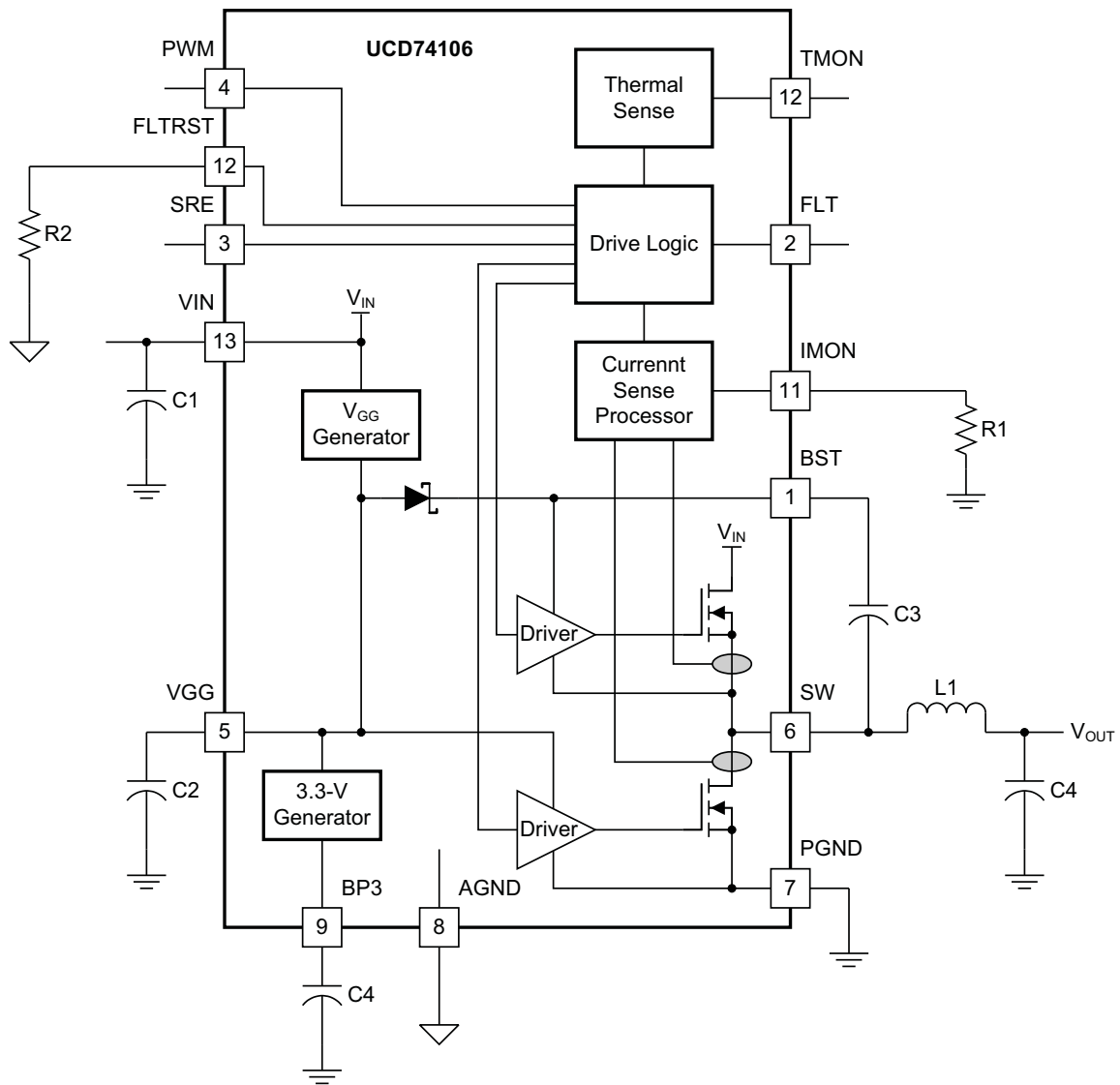| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **FAULT Flag (FLT)** | | | | | | |
| FLT | Output high level | $I_{OH}$ = 500 µA | 2.7 | | | V |
| | Output low level | $I_{OL}$ = 500 µA | | | 0.6 | |
| **Current Limit** | | | | | | |
| | Over current threshold | PWM frequency = 1 MHz, $V_{IN}$ = 12 V, $V_{OUT}$ = 1.2 V | 6.7 | 7.5 | 8.2 | A |
| **Current Sense Amplifier** | | | | | | |
| | Gain[1] | $I_{MON}/I_{SW}$, 0.3 ≤ $V(I_{MON})$ ≤ 1.3 V | 4.106 | 4.322 | 4.538 | µA/A |
| | Zero amp load offset | 0 ≤ $V(I_{MON})$ ≤ 3.1 V, $R_{IMON}$ = 22.6 kΩ | | 22.1 | | µA |
| | **Thermal Sense** | | | | | |
| | Thermal shutdown[1] | | | 155 | | °C |
| | Thermal shutdown hysteresis[1] | | | 30 | | |
| | Temperature sense T[1] | Gain | | 10 | | mV/°C |
| | Temperature sense T offset | $T_J$ = 25 °C, -100 µA ≤ $I_{TMON}$ ≤ 100 µA | | 750 | | mV |
| | **POWER Drive Train** | | | | | |
| | Propagation delay from PWM to switch node going high[1] | | | 20 | | ns |
| | High-side MOSFET turn on – dead Time[1] | | 3 | 5 | 15 | |
| | Low-side MOSFET turn on – dead time[1] | | 3 | 7 | 15 | |
| | Min PWM pulse width[1] | | | 20[2] | | |

(1) As designed and characterized, not fully tested in production.
(2) There is no inherent limit on the minimum pulse width. Depending on the board layout, partial enhancement of the high-side FET may be observed for shorter pulse widths.

## DEVICE INFORMATION

**RGM Package**
**(Top View)**

| | |
|---|---|
| BST 1 | 13 VIN / 12 FLTRST |
| FLT 2 | 11 IMON |
| SRE 3 | SW 6 / 10 TMON |
| PWM 4 | 7 PGND / 9 Bp3 |
| VGG 5 | 8 AGND |
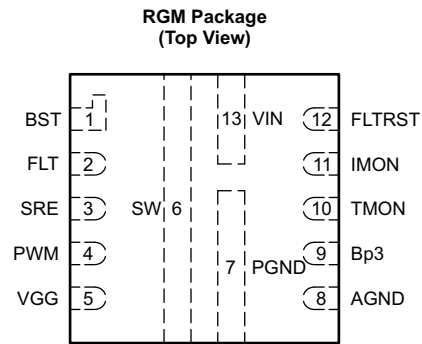
## BLOCK DIAGRAM



**Figure 1. Typical Block Diagram**

## TERMINAL FUNCTIONS

| TERMINAL | | I/O | FUNCTION |
|---|---|---|---|
| NAME | NO. | | |
| PWM | 4 | I | 20-kΩ input capable of accepting 3.3-V or 5-V logic level signals up to 2 MHz. A Schmitt trigger input comparator desensitizes this pin from external noise. This pin controls the state of the high-side MOSFET and the low-side MOSFET when SRE is high. When PWM is in HiZ state the output power stage is turned off within 200 ns. |
| SRE | 3 | I | Synchronous rectifier enable input. High impedance digital input capable of accepting 3.3-V or 5-V logic level signals used to control the synchronous rectifier switch. An appropriate anti-cross-conduction delay is used during synchronous mode. |
| BST | 1 | I | Charge pump capacitor connection. It provides a floating supply for the high-side driver. Connect a 0.22-µF ceramic capacitor from this pin to SW. |
| VGG | 5 | I/O | Gate drive voltage for the power MOSFETs. For $V_{IN}$ > 4.5 V, the internal $V_{GG}$ generator can be used. For $V_{IN}$ < 4.5 V, this pin should be driven from an external bias supply. In all cases, bypass this pin with a 4.7-µF (min), 10-V (min) ceramic capacitor to PGND. |
| BP3 | 9 | O | Output of internal 3.3-V LDO regulator for powering internal logic circuits. Bypass this pin with 1 µF (min) to AGND . This LDO is supplied by the VGG pin. |
| IMON | 11 | O | Current sense monitor output. Provides a current source output that is proportional to the current flowing in the low-side MOSFET. The gain on this pin is equal to 4.32 µA/A. The IMON pin should be connected to a 22.6-kΩ resistor to AGND to produce a voltage proportional to the power-stage load current. The IMON pin sources 22.1 µA at no load. This provides a pedestal that permits the reporting of negative (sinking) current. |
| TMON | 10 | O | Temperature sense pin. The voltage on this pin is proportional to the die temperature. The gain is 10 mV/°C . At $T_J$ = 25°C, the output voltage has an offset of 0.75 V. When the die temperature reaches the thermal shutdown threshold, this pin is pulled to BP3 and power FETs are switched off. Normal operation resumes when the die temperature falls below the thermal hysteresis band. |
| FLT | 2 | O | Fault flag. This signal is a 3.3-V digital output which is latched high when the load current exceeds the current limit trip point. When tripped both high side and low side are latched off. See FLT clear protocol as defined by FLTRST. Additionally, if the die temperature exceeds 150°C, $V_{IN}$ and/or $V_{GG}$ is outside of UVLO limits, the output switching will be halted and FLT flag is set. Normal operation resumes after fault clear sequence is complete. |
| FLTRST | 12 | I | Fault reset mode. |
| PGND | 7 | - | Shared power ground return for the buck power stage |
| SW | 6 | - | Switching node of the buck power stage and square wave input to the buck inductor. Electrically this is the connection of the high-side MOSFET source to the low-side MOSFET drain. |
| VIN | 13 | - | Input voltage to the buck power stage and driver circuit |

# TYPICAL CHARACTERISTICS
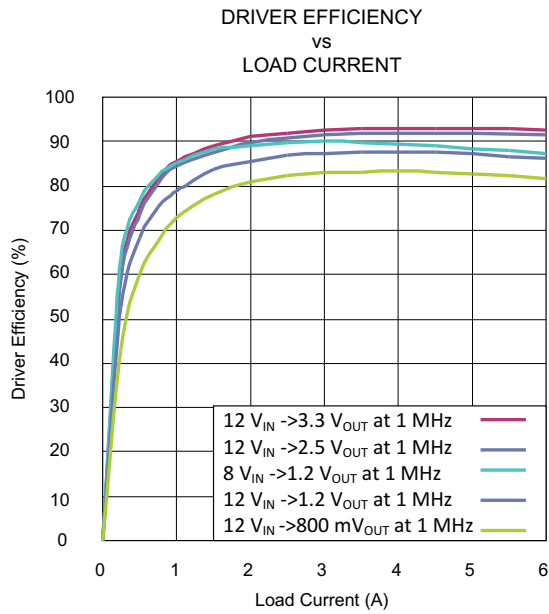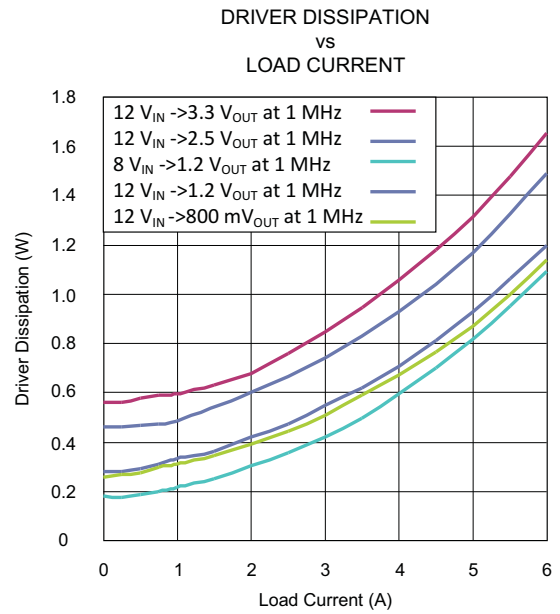
## Typical Efficiency



**Figure 2.**



**Figure 3.**

## PWM and SRE Behavior

The PWM and SRE (Synchronous Rectifier Enable) pins control the high-side and low-side drivers, as described in Table 2.

**Table 2. PWM and SRE Behavior**

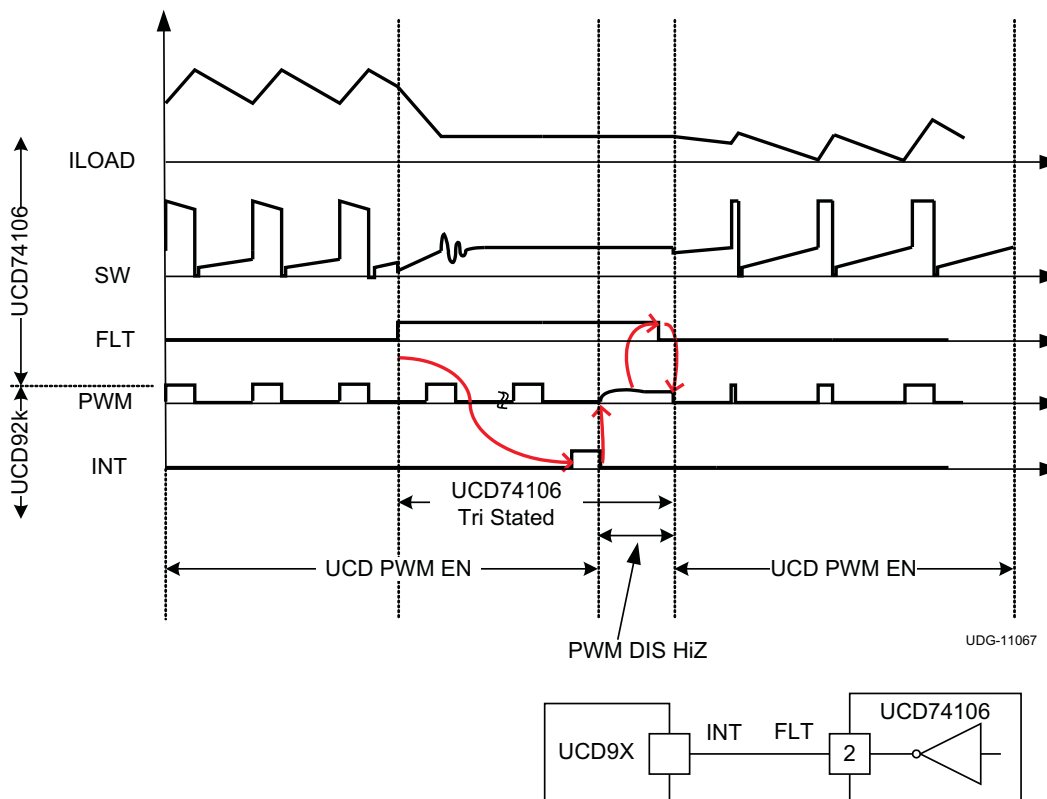|  | PWM = High | PWM = Low | PWM = HiZ |
|---|---|---|---|
| **SRE = High** | HS = ON, LS = OFF | HS = OFF, LS = ON | HS = OFF, LS = OFF |
| **SRE = Low** | HS = ON, LS = OFF | HS = OFF, LS = OFF | HS = OFF, LS = OFF |

## Fault Modes

### Fault Reset Mode

The Fault Reset Mode can be programmed with the FLTRST pin, as described in Table 3

**Table 3.**

| Mode | FLTRST | FLT Clear |
|---|---|---|
| 1 | GND | PWM = HiZ |
| 2 | BP3 | PWM = 0, SRE = 0 |
| 3 | Open | PWM = 1 pulse |

### MODE 1



**Figure 4.  Fault Handshake Protocol, (PWM HiZ)**

**NOTE**

Handshake Sequence:

1.  UCD74106 detects fault condition – FLT flag is set

2.  FLT flag generates UCD interrupt

3.  UCD releases PWM -HiZ state

4.  UCD74106 detects (HiZ) as FLT clear; if fault condition is no longer present then flag is cleared

5.  If FLT clears UCD responds to the Start command, Else PWM stays in HiZ state

**MODE 2**
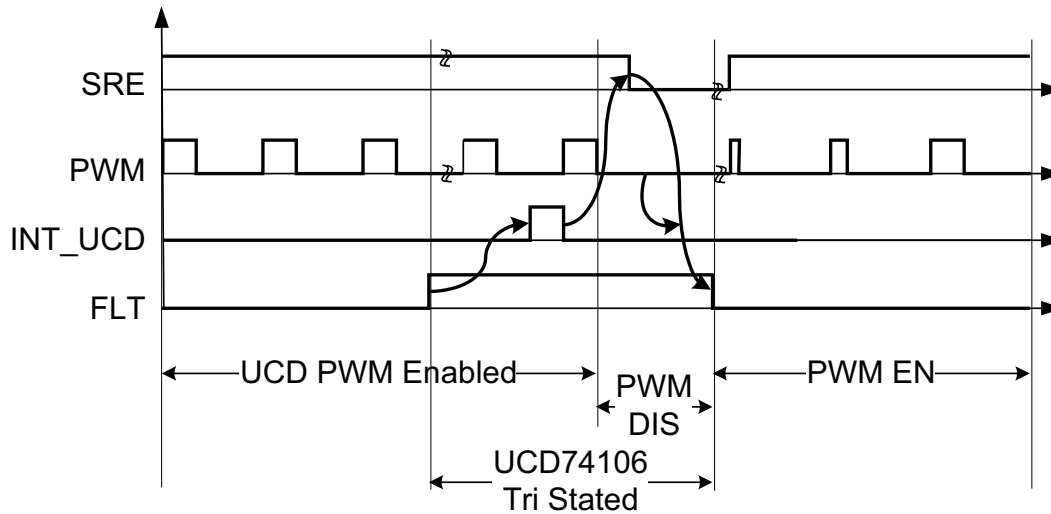


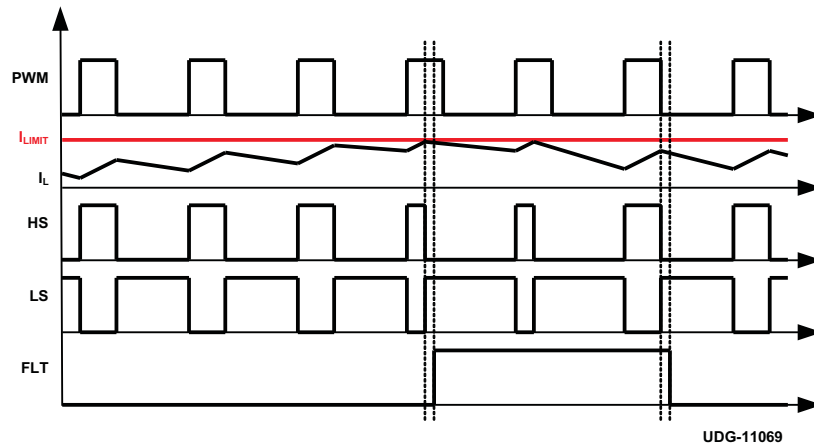**Figure 5. Fault Handshake Protocol, (PWM SRE)**

**NOTE**

Handshake Sequence:

1. UCD74106 detects fault condition – FLT is set

2. FLT flag generates interrupt

3. UCD sets SRE low AND stops PWM

4. UCD74106 reads (SRE and PWM) = low as FLT clear; if fault condition is no longer present then flag is cleared.

5. If FLT clears UCD responds to the Start command, Else (PWM and SRE) = low

**MODE 3**



**Figure 6. Fault Handshake Protocol, (PWM pulses)**

**NOTE**

No Handshake Re-Set:

1. UCD74106 detects fault condition – FL_FLAG is set
2. No action on UCD side.
3. UCD74106 reads one complete PWM pulse without FLT being present and re-sets FLT_FLAG signal on the falling edge of PWM.
4. Within the area of uncertainty: FLT rising edge to FLT_FLAG rising edge delay is zero (gate delay only).
5. PWM falling edge to FLT_FLAG falling edge delay is zero (gate delay only).

The high-side current limit fault behavior shown in Figure 7.



**Figure 7.**

In general, FLT is always cleared by the first complete PWM pulse (a rising and a falling edge) without a fault present. This is true for all faults including UV and OT. The only exception to this occurs during start up where FLT will self clear once UVLO is disabled, as shown in Figure 8. However, if a subsequent under voltage condition occurs the fault must be cleared by one complete PWM pulse without a fault, as shown in Figure 7.
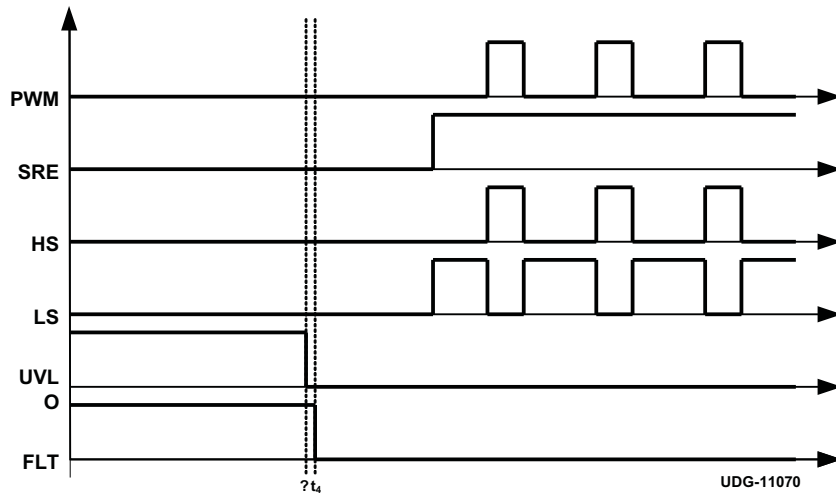


**Figure 8.**

## IMON Behavior

The plot in Figure 9 shows how the voltage on the IMON pin will behave with a 22.6-kΩ resistor. The solid dark line represents the typical behavior and the shaded region represents the tolerance band due too gain.
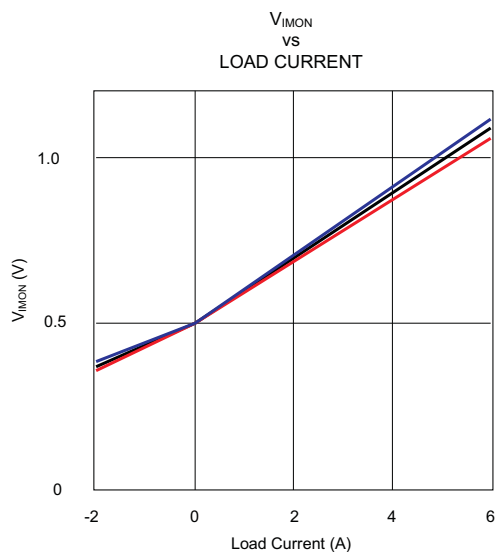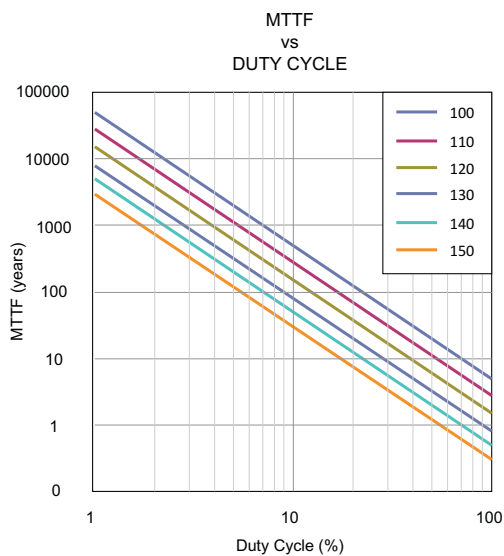
$V_{IMON}$
vs
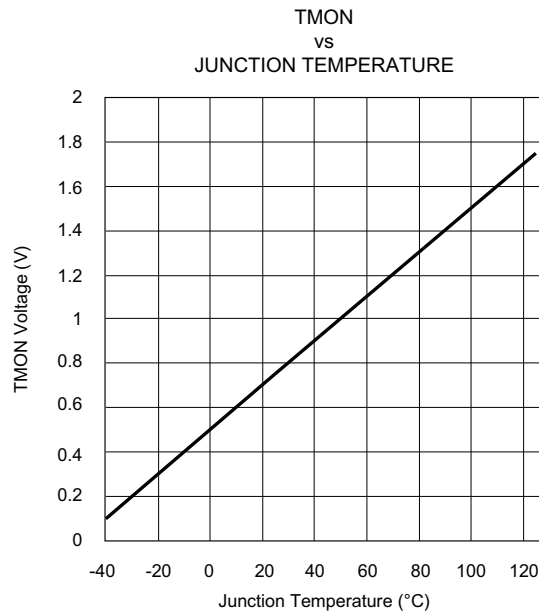LOAD CURRENT



**Figure 9.**

MTTF
vs
DUTY CYCLE



**Figure 10.**

## TMON Behavior

The voltage on this pin is proportional to the die temperature:

$$T_{MON} = T_{OFFSET} + T_{GAIN} \times T_J$$

(1)

**Table 4. Temperature Sense Definitions**

| NAME | DESCRIPTION |
|---|---|
| $T_{MON}$ | Voltage from TMON pin to GND |
| $T_{OFFSET}$ | Thermal sense T offset |
| $T_{GAIN}$ | Thermal sense T gain |
| $T_J$ | Device internal junction temperature |



**Figure 11.**

If the junction temperature exceeds approximately 155°C, the device will enter thermal shutdown. This will assert the FLT pin, both MOSFETs will be turned off and the switch node will become high impedance. When the junction temperature cools by approximately 30°C, the device will exit thermal shutdown and resume switching as directed by the PWM and SRE pins.

## APPLICATION INFORMATION

### Operating Frequency

Switching frequency is a key place to start the design of any DC/DC converter. This will set performance limits on things such as: maximum efficiency, minimum size, and achievable closed loop bandwidth. A higher switching frequency is, generally, going to yield a smaller design at the expense of a lower efficiency. The size benefit is principally a result of the smaller inductor and capacitor energy storage elements needed to maintain ripple and transient response requirements. The additional losses result from a variety of factors, however, one of the largest contributors is the loss incurred by switching the MOSFETs on and off. The integrated nature of the UCD74106 makes these losses drastically smaller and subsequently enables excellent efficiency from a few hundred kHz up to the low MHz. For a reasonable trade off of size versus efficiency, 750 kHz is a good place to start.

### VGG

If 4.5 V < $V_{IN}$ ≤ 6 V then a simple efficiency enhancement can be achieved by connecting $V_{GG}$ directly to $V_{IN}$. This allows the solution to bypass the drop-out voltage of the internal $V_{GG}$ linear regulator, subsequently improving the enhancement of the MOSFETs. When doing this it is critical to make sure that $V_{GG}$ never exceeds the absolute maximum rating of 7 V.

### Inductor selection

There are three main considerations in the selection of an inductor once the switching frequency has been determined. Any real world design is an iterative trade off of each of these factors.

1. The electrical value which in turn is driven by:
    (a) RMS current
    (b) The maximum desired output ripple voltage
    (c) The desired transient response of the converter
2. Losses
    (a) Copper (PCu)
    (b) Core (Pfe)
3. Saturation characteristics of the core

### Inductance Value

The principle equation used to determine the inductance is:

$$v_L(t) = L\frac{di_L(t)}{dt}$$

(2)

During the on time of the converter the inductance can be solved to be:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I}\frac{D}{f_S}$$

(3)

**Table 5. Definitions**

| | |
|---|---|
| $V_{IN}$ | Input voltage |
| $V_{OUT}$ | Output voltage |
| $f_S$ | Switching frequency |
| D | Duty cycle ($V_{OUT}/V_{IN}$ for a buck converter) |
| ΔI | The target peak-to-peak inductor current |

In general, it is desirable to make ΔI large to improve transient response and small to reduce output ripple voltage and RMS current. A number of considerations go into this however, ΔI = 0.4 $I_{OUT}$ results in a small $I_{LRMS}$ without an unnecessary penalty on transient response. It also creates a reasonable ripple current that most practical capacitor banks can handle. Here $I_{OUT}$ is defined as the maximum expected steady state current.

Plugging these assumptions into the above inductance equation results in:

$$L = 5\frac{V_{IN} - V_{OUT}}{2 \times I_{OUT}}\frac{D}{f_S}$$

(4)

For example, plotting this result as a function of $V_{IN}$ and $V_{OUT}$ results in:

- $I_{OUT}$ = 6.0 A
- $f_S$ = 1.0 MHz
- $N_{CRIT}$ = 5
- $ΔI/I_{OUT}$ = 40%
- $ΔI$ = 2.4 A
- $V_{OUT}$ (V)



**Figure 12. $V_{IN}$ and $V_{OUT}$**
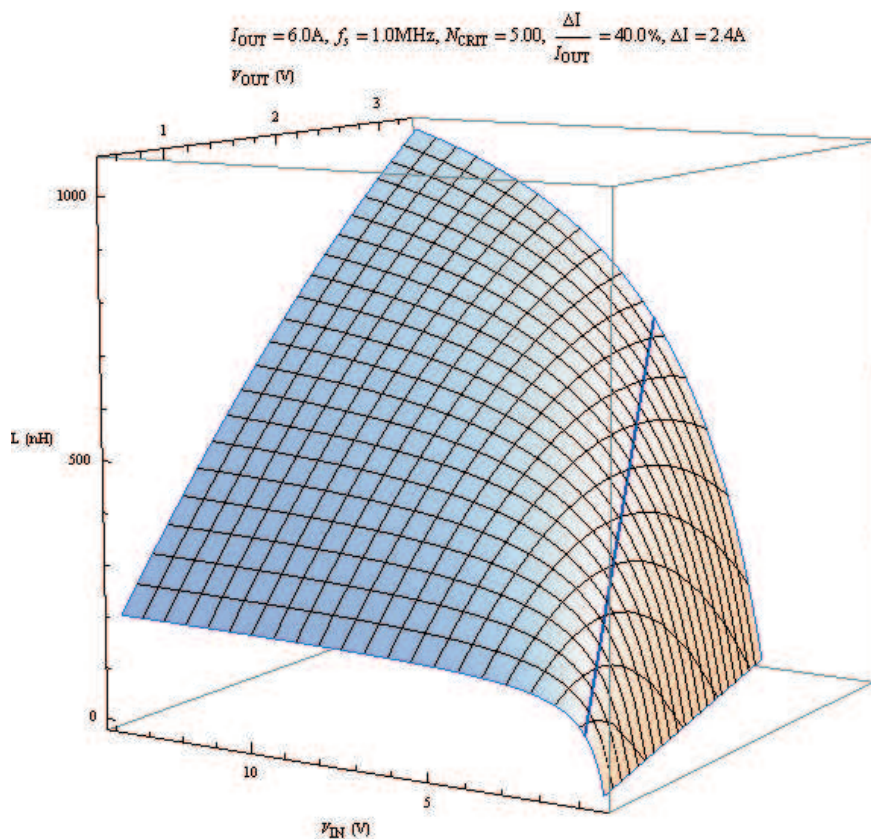
**NOTE**
The maximum inductance occurs at the maximum $V_{IN}$ and $V_{OUT}$ shown in Figure 12. In general, this inductance value should be used in order to keep the inductor ripple current from becoming too large over the range of supported $V_{IN}$ and $V_{OUT}$.

## Inductor Losses and Saturation

The current rating of an inductor is based on two things, the current necessary to raise the component temperature by 40°C and the current level necessary to reduce the inductance to 80% of its initial value (saturation current ). The current rating is the lower of these two numbers. Both of these factors are influenced by the choice of core material. Popular materials currently in use are: ferrite, powdered alloy and powdered iron.

Ferrite is regarded as the highest performance material and as such is the lowest loss and the highest cost. Solid ferrite all by itself will saturate with a relatively small amount of current. This can be addressed by inserting a gap into the core. This, in effect, makes the inductor behave in a linear manner over a wide DC current range. However, once the inductance begins to roll off, these gapped materials exhibit a "sharp" saturation characteristic. In other words the inductance value reduces rapidly with increases in current above the saturation level. This can be dangerous if not carefully considered, in that the current can rise to dangerous levels.

Powdered iron has the advantage of lower cost and a soft saturation characteristic; however, its losses can be very large as switching frequencies increase. This can make it undesirable for a UCD74106 based application where higher switching frequency may be desired. It's also worth noting that many powdered iron cores exhibit an aging characteristic where the core losses increase over time. This is a wear out mechanism that needs to be considered when using these materials.

The powdered alloy cores bring the soft saturation characteristics of powered iron with considerable improvements in loss without the wear-out mechanism observed in powered iron. These benefits come at a cost premium.

In general the following relative figure of merits can be made:

**Table 6. Core Material Choices**

|  | FERRITE | POWDERED ALLOY | POWDERED IRON |
|---|---|---|---|
| COST | High | Medium | Low |
| LOSS | Low | Medium | High |
| SATURATION | Rapid | Soft | Soft |

When selecting an inductor with an appropriate core it's important to have in mind the following:

- $I_{LRMS}$, maximum RMS current
- $\Delta I$, maximum peak-to-peak current
- $I_{MAX}$, maximum peak current

The RMS current can be determined by the following equation:

$$I_{LRMS} = \sqrt{I_{OUT}{}^2 + \frac{\Delta I^2}{12}}$$

(5)

When the 40% ripple constraint is used at maximum load current, this equation simplifies to: $I_{LRMS} \approx I_{OUT}$.

It is widely recognized that the Steinmetz equation ($P_{fe}$) is a good representation of core losses for sinusoidal stimulation. It is important to recognize that this approximation applies to sinusoidal excitation only. This is a reasonable assumption when working with converters whose duty cycles are near 50%, however, when the duty cycle becomes narrow this estimate may no longer be valid and considerably more loss may result.

$$P_{fe} = k \times f^{\alpha} \times B_{AC}^{\beta}$$

(6)

The principle drivers in this equation are the material and its respective geometry (k, α, β), the peak AC flux density ($B_{AC}$) and the excitation frequency (f). The frequency is simply the switching frequency of the converter while the constant k, can be computed based on the effective core volume ($V_e$) and a specific material constant ($k_{fe}$).

$$k = k_{fe} \times V_e$$

(7)

The AC flux density ($B_{AC}$) is related to the conventional inductance specifications by the following relationship:

$$B_{AC} = \frac{L}{A_e \times N} \frac{\Delta I}{2}$$

(8)

Where L is the inductance, $A_e$, is the effective cross sectional area that the flux takes through the core and N is the number of turns.

Some inductor manufactures use the inductor ΔI as a figure of merit for this loss, since all of the other terms are a constant for a given component. They may provide a plot of core loss versus ΔI for various frequencies where ΔI can be calculated as:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \frac{D}{f_S}$$

(9)

$I_{MAX}$ has a direct impact on the saturation level. A good rule of thumb is to add 15% of head room to the maximum steady state peak value to provide some room for transients.

$$I_{MAX} = 1.15 \times \left( I_{OUT} + \frac{\Delta I}{2} \right)$$

(10)

For example for a 6-A design has the following:

**Table 7. 6-A Design: Inductor Current Requirements**

| $I_{OUT}$ | 6 A |
|---|---|
| $I_{LRMS}$ | 6 A |
| ΔI | 2.4 A |
| $I_{MAX}$ | 9.6 A |

Armed with this data one can now approach the inductor datasheet to select a part with a saturation limit above 9 A and current heating limit above 6 A. Furthermore total losses can be estimated based on the datasheet DCR value ($I_{LRMS}^2$ x DCR) and the core loss curves for a given frequency and ΔI.

## Input Capacitance

Due to the non-zero impedance of the power planes of the input voltage rail, it is necessary to add some local capacitance near the UCD74106 to ensure that the voltage at this node is quiet and stable. The primary things to consider are:

• The radiated fields generated by the di/dt and dv/dt from this node
• RMS currents capability needed in the capacitors
• The AC voltage present and respective susceptibility of any device connected to this node

$$I_{CINRMS} = \sqrt{I_{OUT}^2 \times D \times (1-D) + \frac{\Delta I^2}{12} \times D}$$

(11)

As a point of reference if $\Delta I = 0.4 \ I_{OUT}$ this places the worst case $I_{CINRMS}$ at approximately 3 A. This corresponds to a duty cycle of approximately 50%. Other duty cycles can result in a significantly lower RMS current.

A good input capacitor would be a 22-µF X5R ceramic capacitor. Equally important as selecting the proper capacitor is placing and routing that capacitor. It is crucial that the decoupling be placed as close as possible to both the power pin (VIN) and ground (PGND). It is important to recognize that each power stage should have its own local decoupling. One 22-µF capacitor should be placed across each VIN and PGND pair. The proximity of the capacitance to these pins will reduce the radiated fields mentioned above.

## Output Capacitance

The goal of the output capacitor bank is to keep the output voltage within regulation limits during steady state and transient conditions.

The total AC RMS current flowing through the capacitor bank can be calculated as:

$$I_{COUTRMS} = \frac{\Delta I}{\sqrt{12}}$$

(12)

For a single type of output capacitor the output ripple voltage wave form can be approximated by the following equation:

$$V_{OUT}(t) = I_C(t) \times esr + \frac{1}{C}\int_0^t I_C(\tau) \times d\tau$$

(13)

Where:

$$I_C(t) = \begin{cases} \dfrac{\Delta I \times f_S}{D} \times t - \dfrac{\Delta I}{2} & t < \dfrac{D}{f_S} \\[3mm] \dfrac{\Delta I \times f_S}{1-D} \times \left(t - \dfrac{D}{f_S}\right) + \dfrac{\Delta I}{2} & \text{otherwise} \end{cases}$$

(14)

After substitution and simplification yields:

$$V_{OUT}(t) = \begin{cases} esr \times \left(\dfrac{\Delta I \times f_S}{D} \times t - \dfrac{\Delta I}{2}\right) + \dfrac{1}{C} \times \left(\dfrac{t \times \Delta I \times (f_S \times t - D)}{2 \times D} - \dfrac{\Delta I \times (1 - 2 \times D)}{12 \times f_S}\right) & t < \dfrac{D}{f_S} \\[4mm] esr \times \left(\dfrac{\Delta I \times f_S}{1-D} \times \left(t - \dfrac{D}{f_S}\right) + \dfrac{\Delta I}{2}\right) + \dfrac{1}{C} \times \left(\dfrac{\Delta I \times (f_S \times t - 1) \times (D - f_S \times t)}{2 \times (1-D) \times f_S} - \dfrac{\Delta I \times (1 - 2 \times D)}{12 \times f_S}\right) & \text{otherwise} \end{cases}$$

(15)

The term in this equation multiplied by the esr gives the ripple voltage component due to esr and the term multiplied by 1/C gives the ripple voltage component due to the change in charge on the capacitor plates. In the case were the esr component dominates the peak-to-peak output voltage can be approximated as:

$$V_{PPesr} \approx \Delta I \times esr$$

(16)

When the charge term dominates the peak-to-peak voltage ripple becomes:

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_S}$$

(17)

It's tempting to simply add these two results together for the case where the voltage ripple is significantly influenced by both the capacitance and the esr. However, this will yield an overly pessimistic result, in that it does not account for the phase difference between these terms.

Using the ripple voltage equations and the RMS current equation should give a design that safely meets the steady state output requirements. However, additional capacitance is often needed to meet transient requirements and the specific local decoupling requirements of any device that is being powered off of this voltage. This is not just a function of the capacitor bank but also the dynamics of the control loop. See the UCD9240 Compensation Cookbook for additional details (TI Literature Number SLUA497).

## Decoupling

It is necessary that $V_{GG}$ and BP3 have their own local capacitance as physically close as possible to these pins. The $V_{GG}$ capacitor should be connected as close as possible to the VGG pin and PGND with a 4.7-µF ceramic capacitor. The BP3 capacitor should be connected as close as possible to BP3 pin and AGND with a 1-µF ceramic capacitor.

The UCD74106 also supports the ability to operate from input voltages down to 2.2 V. In these cases an additional supply rail must be connected to $V_{GG}$. Potential external bias supply generators for low VIN operation: TPS63000, TPS61220.

## Current Sense

An appropriate resistor must be connected to the current sense output pins to convert the IMON current to a voltage. In the case of the UCD92xx digital controllers, these parts have a full scale current monitor range of 0 V to 2 V. This range can be maximized to make full use of the current monitoring resolution inside the controller.

$$\frac{V_{MON(min)}}{I_{OFFSET} + I_{MIN} \times I_{GAIN}} \leq R_{MON} \leq \frac{V_{MON(max)}}{I_{OFFSET} + I_{MAX} \times I_{GAIN}}$$

(18)

**Table 8. Current Sense Definitions**

| NAME | DESCRIPTION |
|------|-------------|
| $R_{MON}$ | Resistor from IMON pin to GND |
| $V_{MON(min)}$ | Minimum voltage for IMON (typically, 0.2 V) |
| $V_{MON(max)}$ | Maximum voltage for IMON (typically, 1.8 V) |
| $I_{MIN}$ | Minimum load current to sense |
| $I_{MAX}$ | Maximum load current to sense |
| $I_{OFFSET}$ | Current sense amplifier zero amp load offset |
| $I_{GAIN}$ | Current sense amplifier gain |

The recommended 22.6-kΩ resistor can be used to keep IMON within range for sensing load currents below -2 A to above 6 A.

In some applications it may be necessary to filter the IMON signal. The UCD74106 IMON pin is a current source output, so a capacitor to ground in parallel with the current-to-voltage conversion resistor is all that is required. As a rule of thumb, placing the corner frequency of the filter at 20% of the switching frequency should be sufficient.

For example, if the switching frequency is 500 kHz or higher, the ripple frequency will be easily rejected with a corner frequency of approximately 100 kHz. With a 100-kHz pole point, the filter time constant is 1.6 µs. A fast current transient should be detected within 4.8 µs.

$$C_{MON} = \frac{1}{2 \times \pi \times R_{MON} \times 20\% \times f_S}$$

(19)

## Layout Recommendations

The primary thermal cooling path is from the VIN, GND, and the SW stripes on the bottom of the package. Wide copper traces should connect to these nodes. 1-ounce copper should be the minimum thickness of the top layer; however, 2 ounce is better. Multiple thermal vias should be placed near the GND stripes which connect to a PCB ground plane. There is room to place multiple 10 mil (0.25 mm) diameter vias next to the VIN and GND stripes under the package.

For input bypassing, the 22-µF input ceramic caps should be connected as close as possible to the VIN and GND stripes. If possible, the input caps should be placed directly under the UCD74106 using multiple 10-mil vias to bring the VIN and GND connections to the back side of the board. Minimizing trace inductance in the bypass path is extremely important to reduce the amplitude of ringing on the switching node.

## REVISION HISTORY

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCD74106RGMR | ACTIVE | VQFN-HR | RGM | 13 | 3000 | RoHS-Exempt & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74106 | Samples |
| UCD74106RGMT | ACTIVE | VQFN-HR | RGM | 13 | 250 | RoHS-Exempt & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74106 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UCD74106RGMR | VQFN-HR | RGM | 13 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| UCD74106RGMT | VQFN-HR | RGM | 13 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|-------------|-----------------|------|-----|-------------|------------|-------------|
| UCD74106RGMR | VQFN-HR | RGM | 13 | 3000 | 356.0 | 356.0 | 35.0 |
| UCD74106RGMT | VQFN-HR | RGM | 13 | 250 | 210.0 | 185.0 | 35.0 |

RGM (S−PVQFN−N13)           PLASTIC QUAD FLATPACK NO−LEAD

$\frac{3,10}{2,90}$

$\frac{3,10}{2,90}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

$\frac{0,05}{0,00}$

0,08

0,23 Ref.

0,50

0,25 Ref.

1

5

EXPOSED POWER BUSSES

D

6

13

7

$\frac{0,50}{0,30}$

12

8

2,00

10X $\frac{0,30}{0,20}$   ⊕ | 0,10 | M

Bottom View

4210353/A 07/09
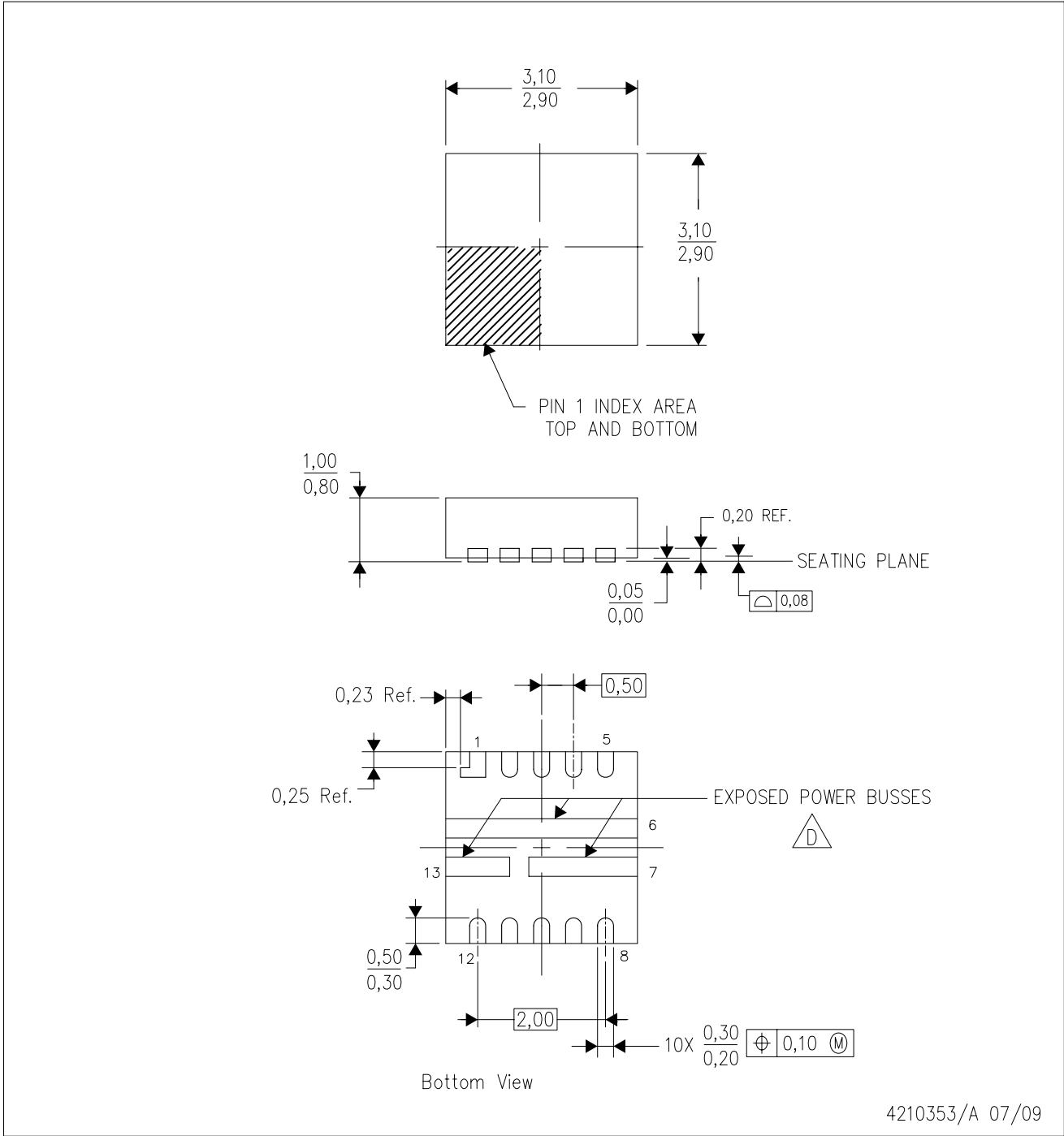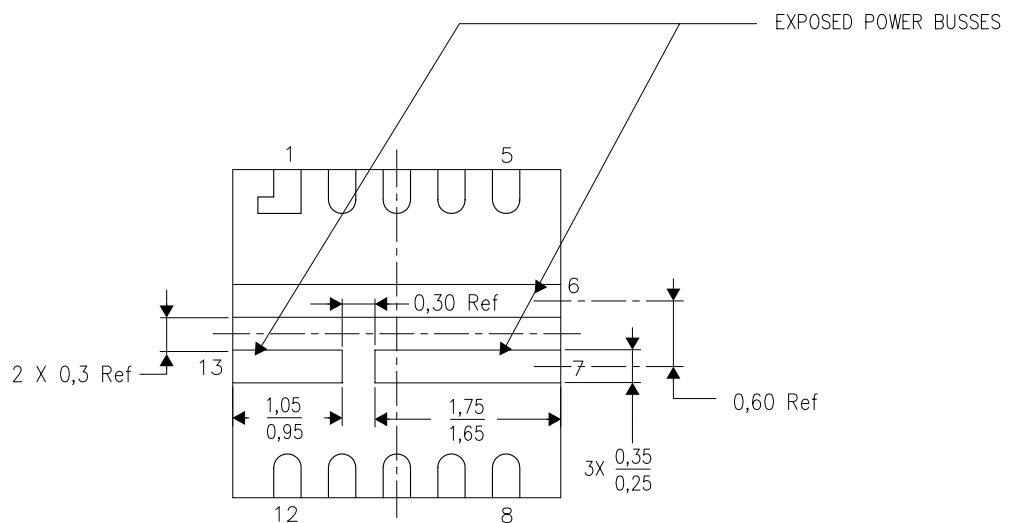
NOTES:   A.  All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.  This drawing is subject to change without notice.
          C.  Quad Flatpack, No−leads (QFN) package configuration.
          D.  See the Product Data Sheet for details regarding the exposed power buss dimensions.
          E.  RoHS exempt flip chip application. Internal solder joints may contain Pb.
          F.  Exposed terminals are Pb−free

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## THERMAL INFORMATION

This package incorporates an exposed and partitioned thermal pad that functions electrically as distinct power busses. The power busses must be soldered directly to the printed circuit board (PCB). After soldering, the PCB electrically connects the power busses. In addition, the PCB can be used as a heatsink that can be enhanced with the use of thermal vias.

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed power buss dimensions for this package are shown in the following illustration.

EXPOSED POWER BUSSES

1    5

6

0,30 Ref

2 X 0,3 Ref — 13

7

1,05
0,95
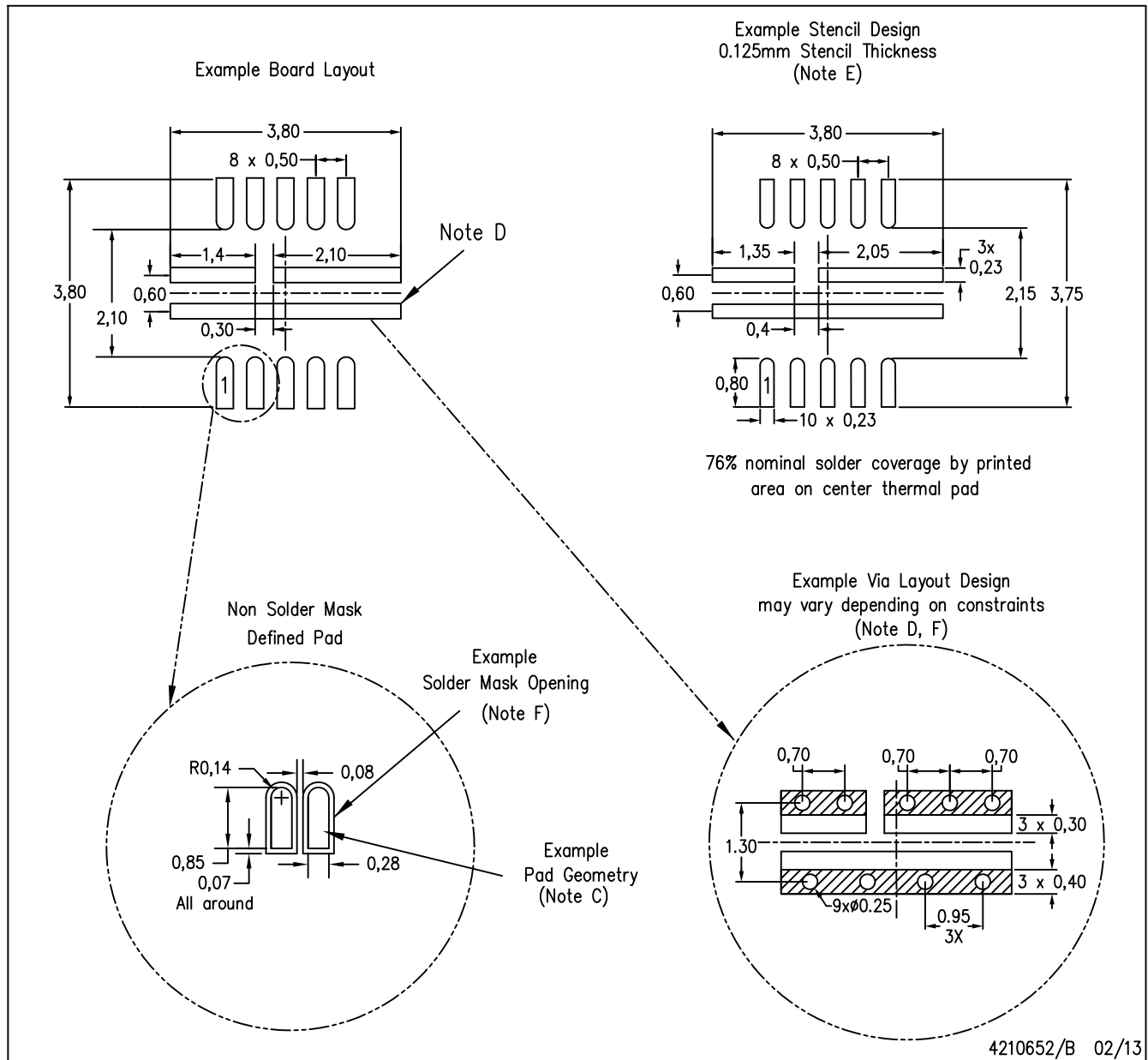
1,75
1,65

0,60 Ref

3X $\frac{0,35}{0,25}$

12    8

Bottom View

NOTE:   All linear dimensions are in millimeters

Exposed Power Buss Dimensions

RGM (R-PVQFN-N13)          PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

3,80
8 x 0,50
1,4    2,10
3,80
0,60
2,10
0,30

Note D

1

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

3,80
8 x 0,50
1,35    2,05
3x
0,23
0,60
0,4
2,15  3,75

0,80   1
10 x 0,23

76% nominal solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

R0,14        0,08

0,85         0,28
0,07
All around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

0,70      0,70      0,70

1.30
3 x 0,30

3 x 0,40
9xØ0.25   0.95
3X

4210652/B  02/13

NOTES:  A.  All linear dimensions are in millimeters.
        B.  This drawing is subject to change without notice.
        C.  Publication IPC-7351 is recommended for alternate designs.
        D.  This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat-Pack
            Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.  These documents are available at
            www.ti.com <http://www.ti.com>.
        E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
            contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
        F.  Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.